Phase Noise and Jitter in Digital Electronics

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Outline

- Basics
- FPGAs — Mechanisms / Examples / Facts
- ADCs — Basics / Examples
- DDSs — Basics / Advanced / Examples
- Dividers — Π and Λ / Microwave

home page http://rubiola.org

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…and myself

Caveat

Only a fraction of this can be taught at a 1–2 H session

1 – Basics

Jitter

$$v(t) = V_0 \left[1 + \alpha(t)\right] \cos\left[2\pi\nu_0 t + \varphi(t)\right] \qquad x(t) = \frac{\varphi(t)}{2\pi\nu_0}$$

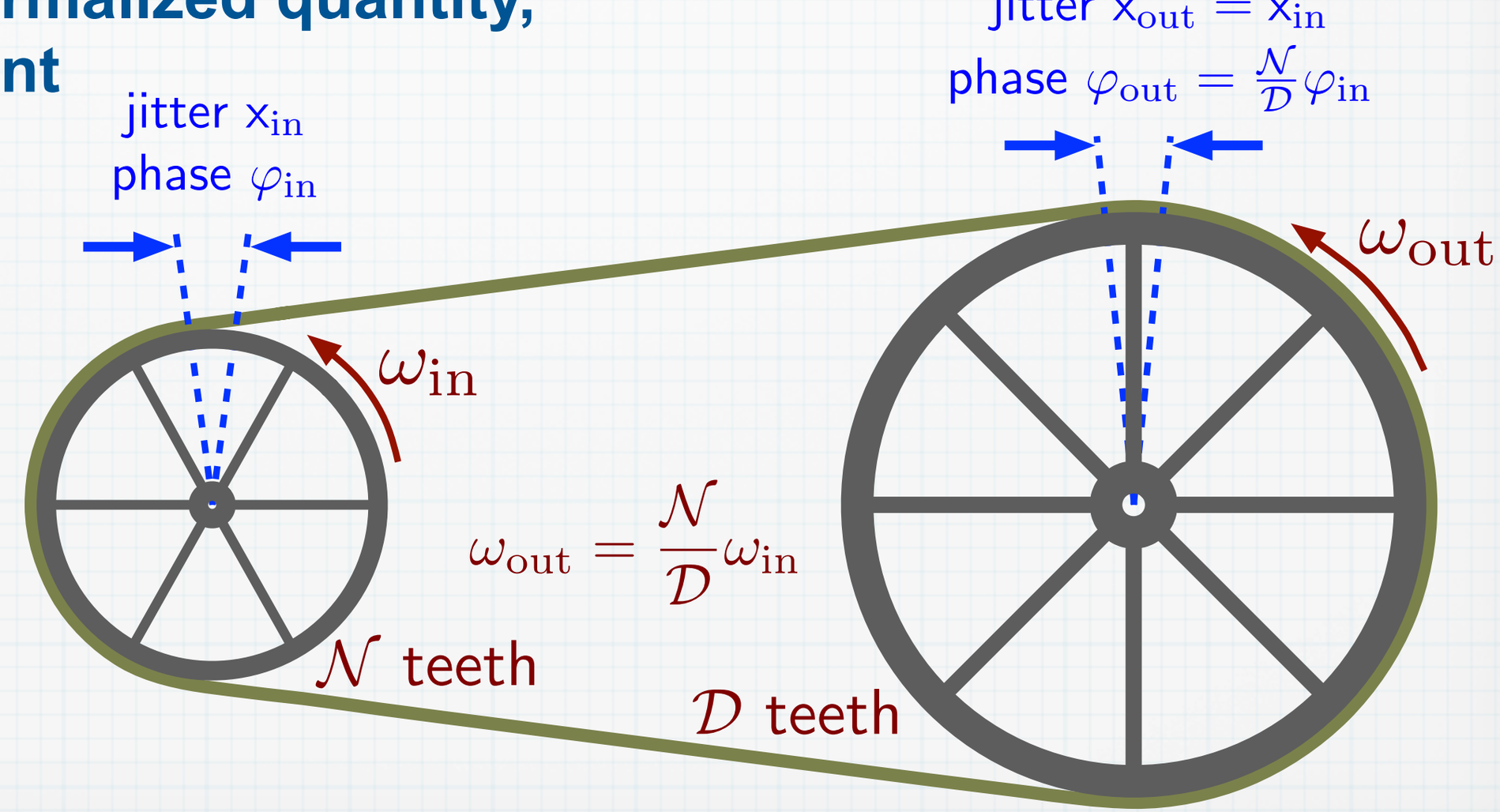
- ITU defines jitter as the variations in the significant instants of a clock or data signal, vs a “perfect” clock
- Jitter —> Usually fast phase changes *f* > a few tens of Hz
- Wander —> Usually slower phase changes (due to temperature, voltage, etc)
- Designers first care about consistency of logic functions,
  - First, maximum timing error
  - Sometimes RMS value and probability distribution
- Time and Frequency community focuses on
  - PM noise spectra
  - Delay spectra
  - Two-sample variances (ADEV, TDEV, etc.)

Phase Time x(t) — or Jitter

- Let's allow φ(t) to exceed ±π, and count the no of turns
- This is easily seen by scaling ω down (up) to ω = 1 rad/s using a noise-free gear work
- The phase-time fluctuation associated to φ(t) is

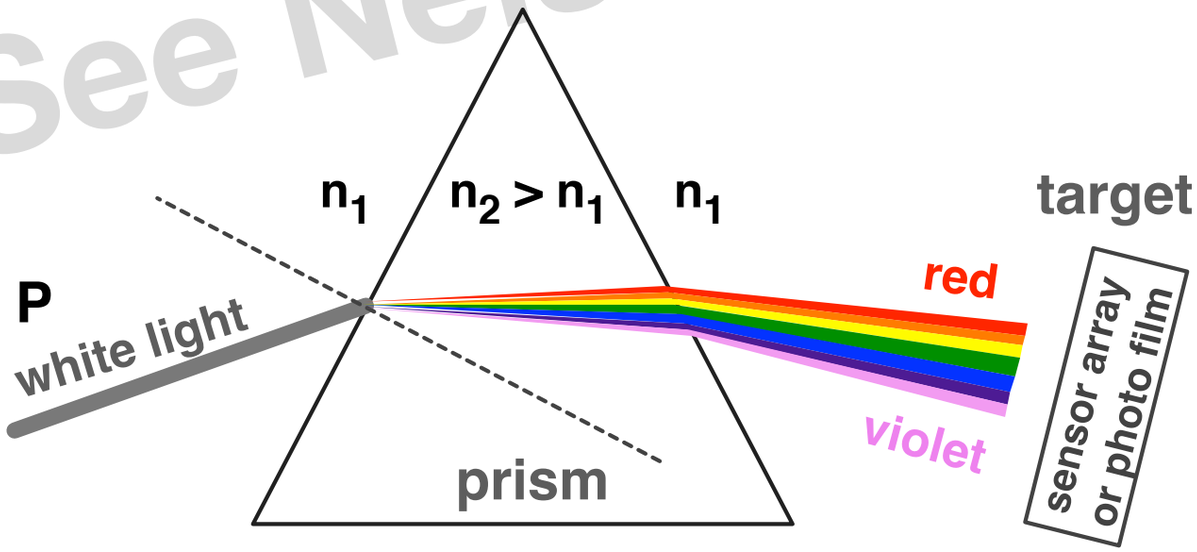
$$x(t) = \varphi(t) / \omega_0$$

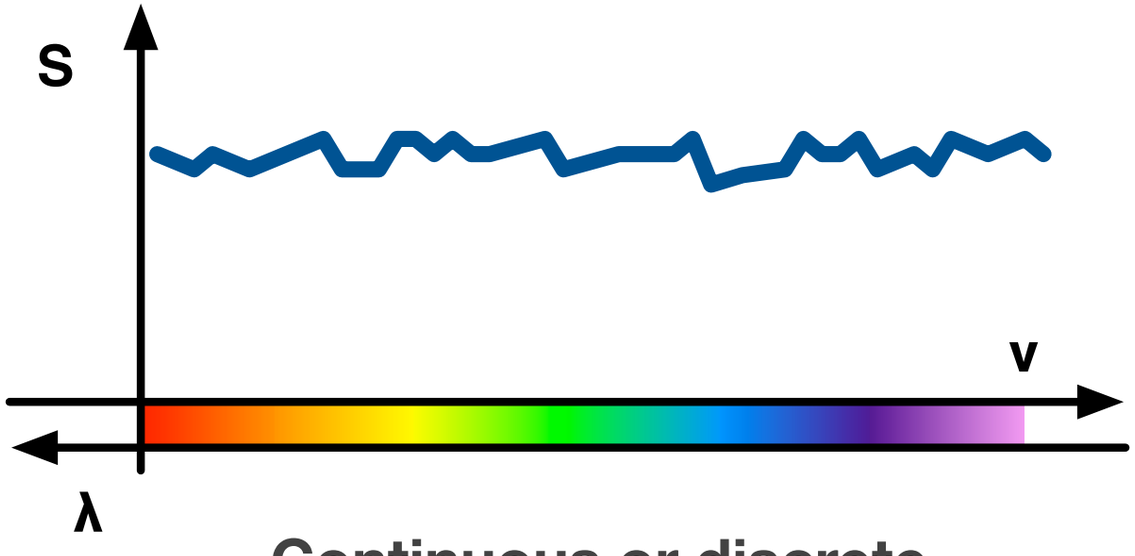
- x(t) is a normalized quantity, independent of ω_0.



Physical Concept of PSD S(*f*)

Power Spectral Density



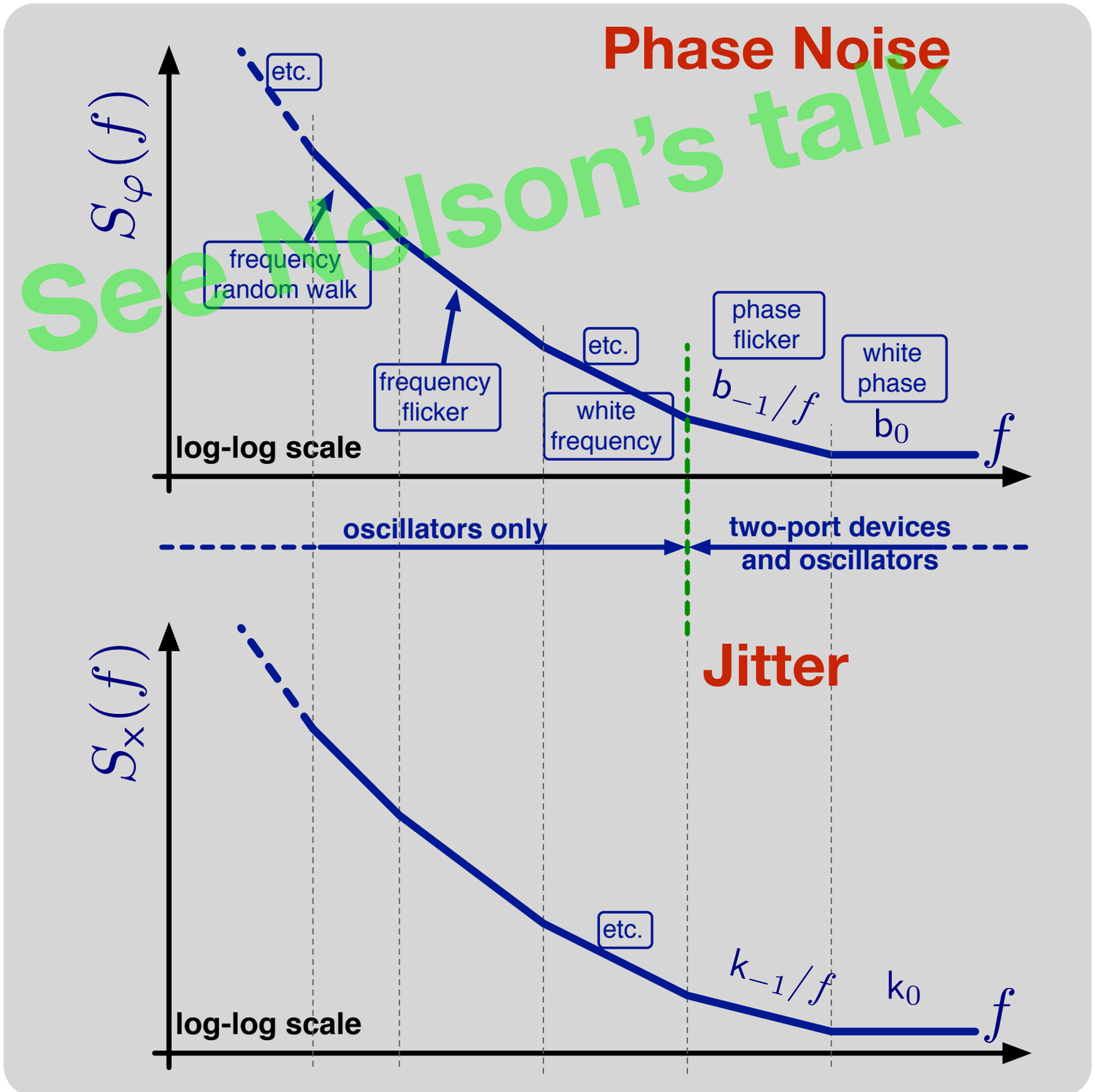


Continuous or discrete

- The PSD is the distribution of power vs. frequency (power in 1-Hz bandwidth)
- The PS is the distribution of energy vs. frequency (energy in 1-Hz bandwidth)
- Frequency can be continuous or discrete (histogram),
- In mathematics,
  - the power is a square quantity
  - the energy is power integrated in time
- Power (energy) in physics is a square (integrated) quantity
  - PSD –> W/Hz (or V^2/Hz, A^2/Hz, etc.)
  - PS –> J/Hz

The Polynomial Law

$$v(t) = V_0 \left[1 + \alpha(t)\right] \cos\left[2\pi\nu_0 t + \varphi(t)\right]$$



Phase Noise PSD

$$S_\varphi(f) = \sum_{i \le -4}^{0} b_i f^i$$

Jitter (phase-time) PSD

$$x(t) = \frac{\varphi(t)}{2\pi\nu_0}$$

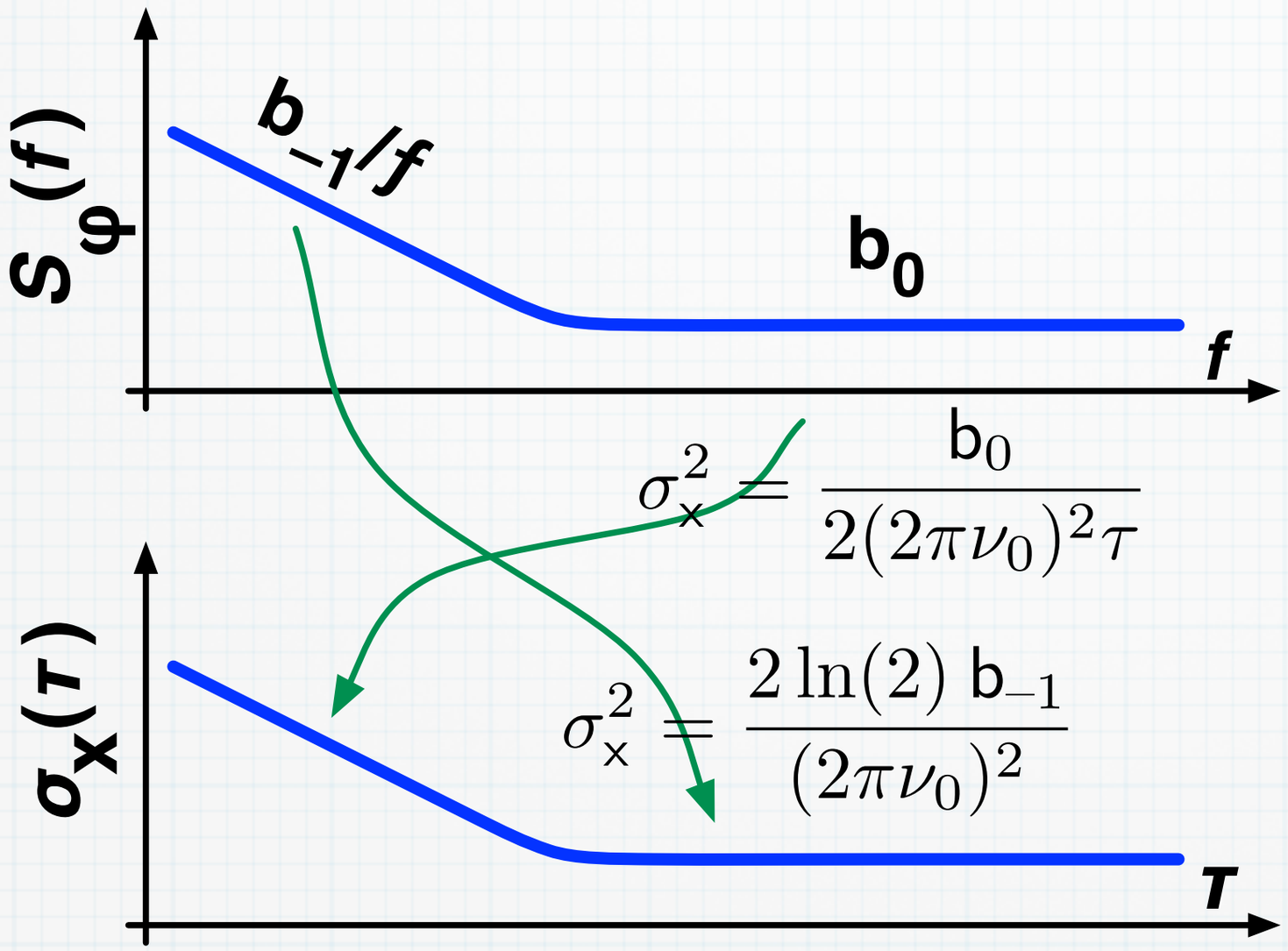
$$S_x(f) = \sum_{i \le -4}^{0} k_i f^i$$

Fractional Frequency PSD

$$y(t) = \dot{x}(t) = \frac{\dot{\varphi}(t)}{2\pi\nu_0}$$

$$S_y(f) = \sum_{i \le -2}^{2} h_i f^i$$

Converting PM noise to TDEV



random phase

$$\varphi(t)$$

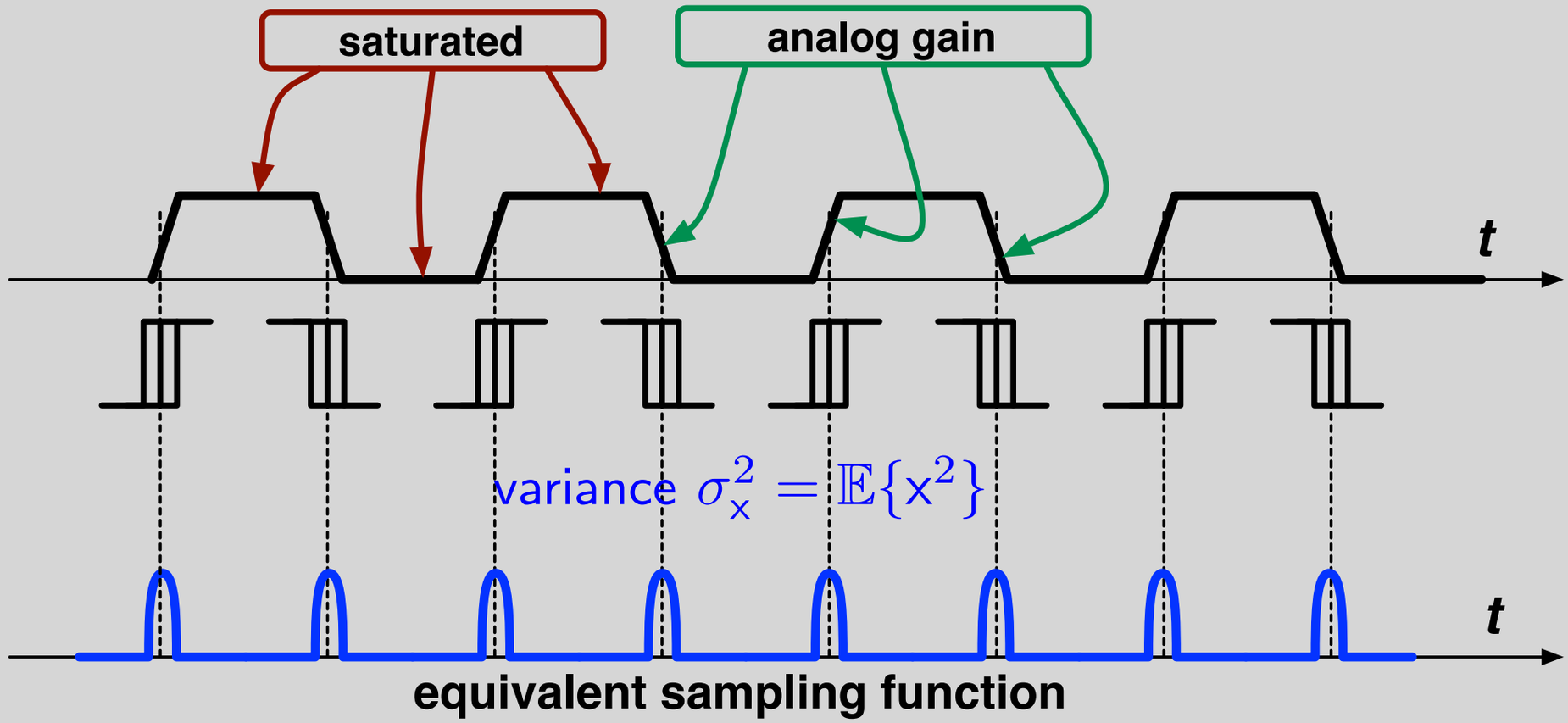
phase-time (fluctuation)

$$x(t) = \frac{\varphi(t)}{2\pi\nu_0}$$

TDEV $\sigma_x(\tau)$ same as ADEV, but we use x(t) instead of y(t)

You may be more familiar to $\sigma_y^2(\tau) = h_0/2\tau + 2\ln(2)h_{-1}$

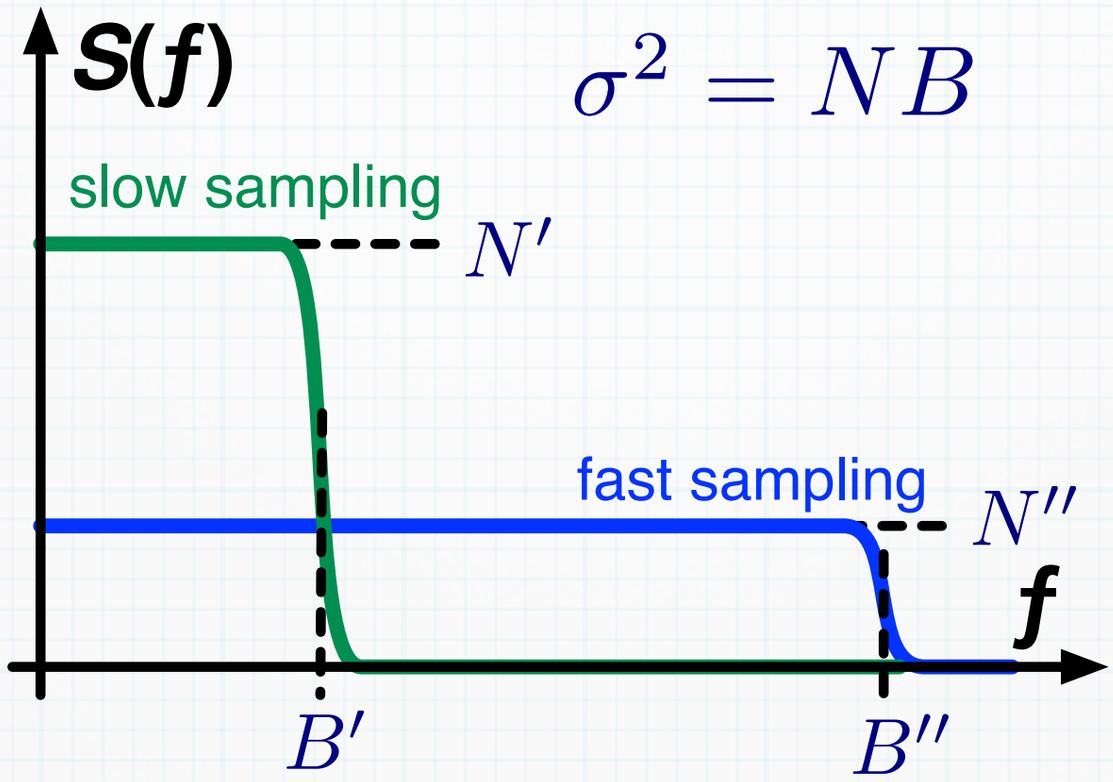
Phase Noise Sampling



input sampling frequency $2\nu_0 \longrightarrow$ noise bandwidth $B = \nu_0$

- **Sampling occurs at the edges**
  - (in some cases, only at rising or falling edges)
- **Square wave signals need analog bandwidth at least 3 v_{max} ... 4 v_{max}**
- **Aliasing is expected**

Aliasing Over-Simplified

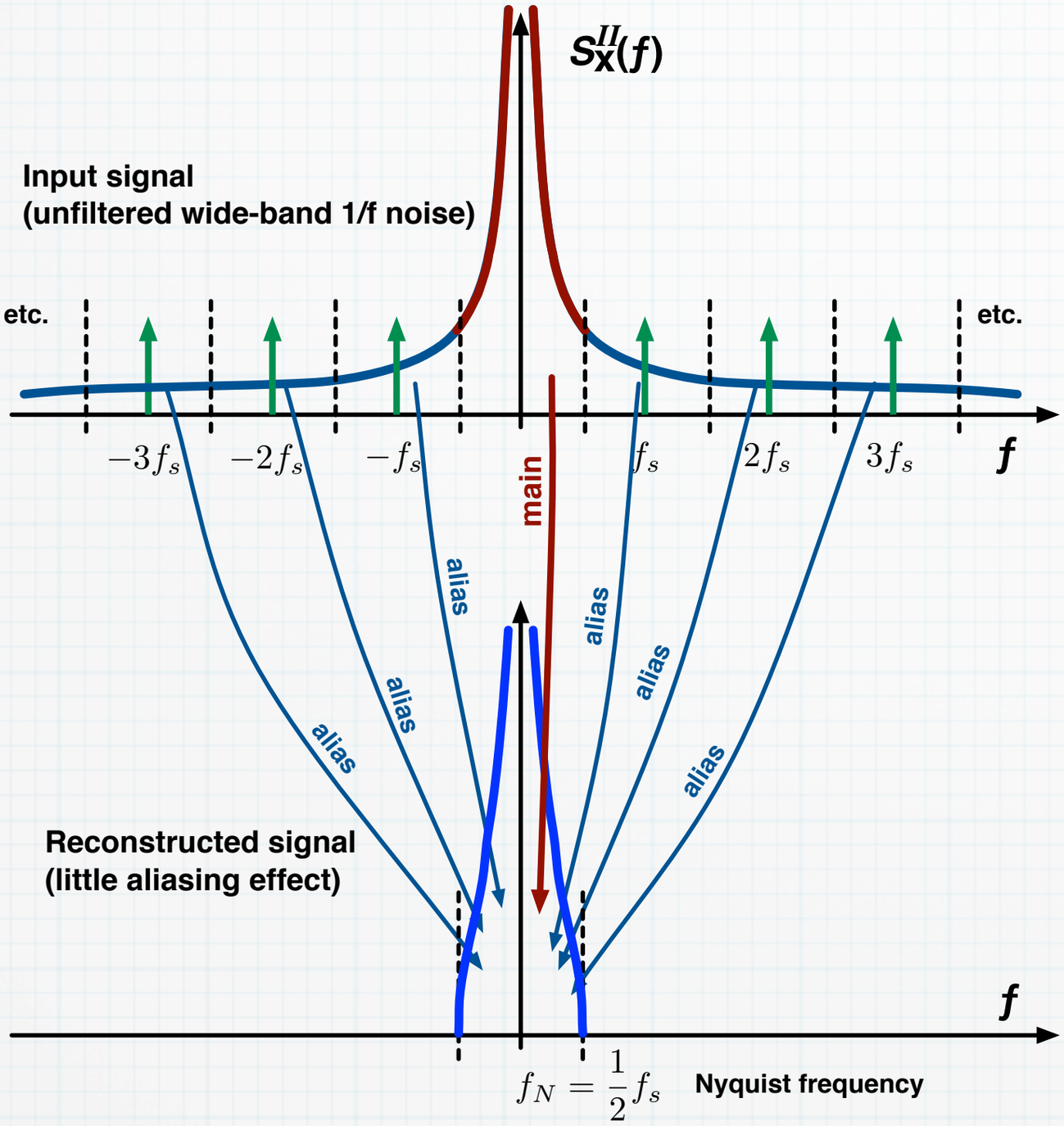


- **The Parseval Theorem states that**
  the total energy (or power) calculated in the time domain and in the frequency domain is the same
- **Ergodicity allows to**
  interchange time domain and statistical ensemble

N'B' = N"B"

…and PM noise scales up with the reciprocal of the carrier frequency

Aliasing and 1/f Noise



Low power in the high-f aliases

Little or no effect on the noise spectrum

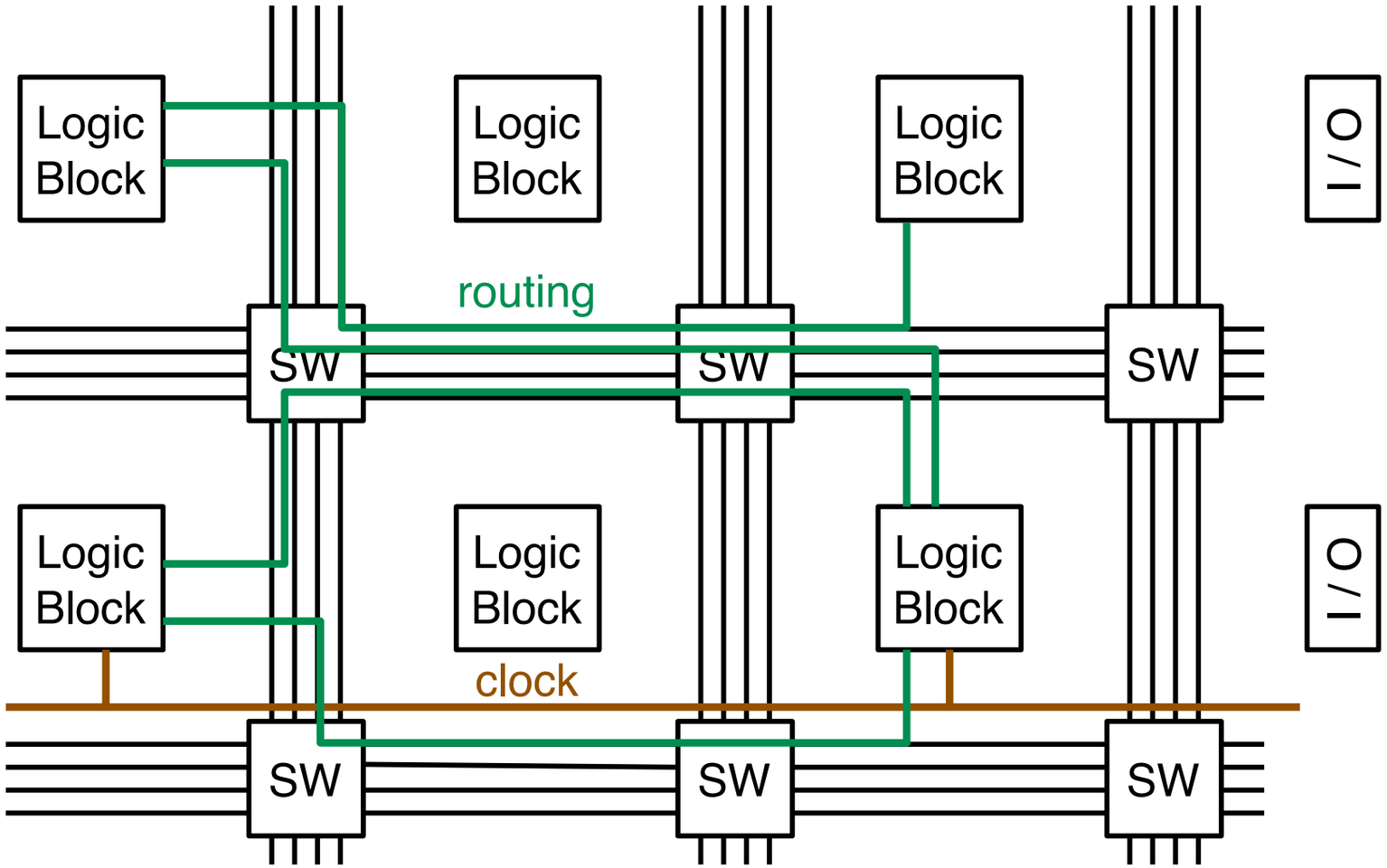
And virtually no effect with $1/f^2$, $1/f^3$, $1/f^4$ …

2 – FPGAs

- Noise Mechanisms
- Examples
- Additional Facts

Noise Mechanisms

FPGA Interconnection Structure



Device dependent blocks

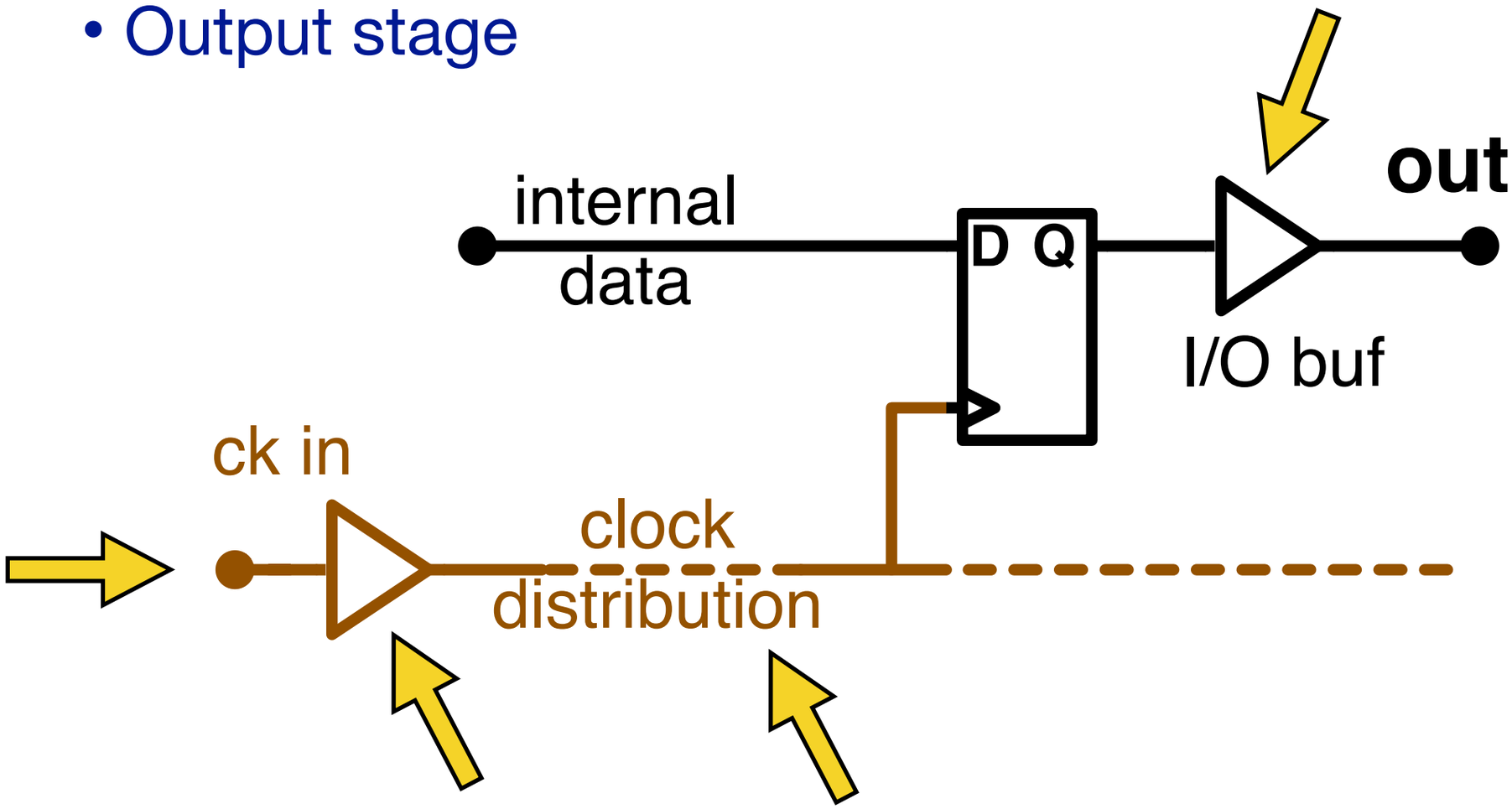
- Input/Output
- RAM
- PLL
- NCO
- …etc.

Delay & jitter

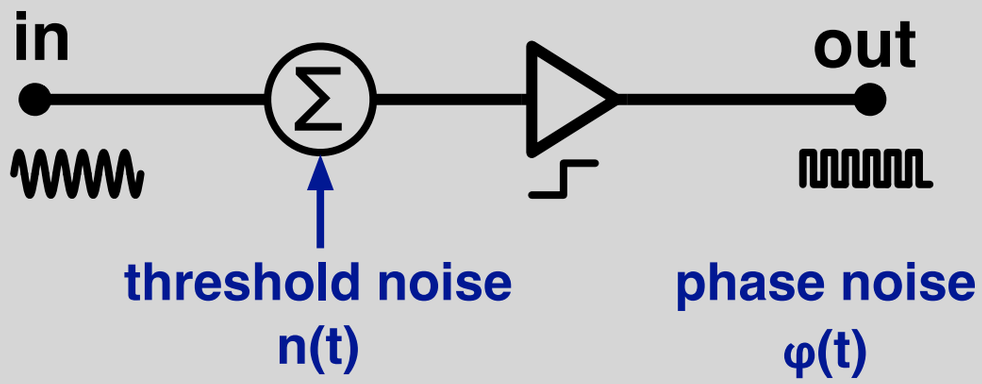
- General routing through switch points
  - Delay & jitter rather uniform in a block
  - Large spread over the interconnect matrix
- Dedicated clock lines managed separately
  - Low and predictable delay & jitter

Output Jitter Limitations

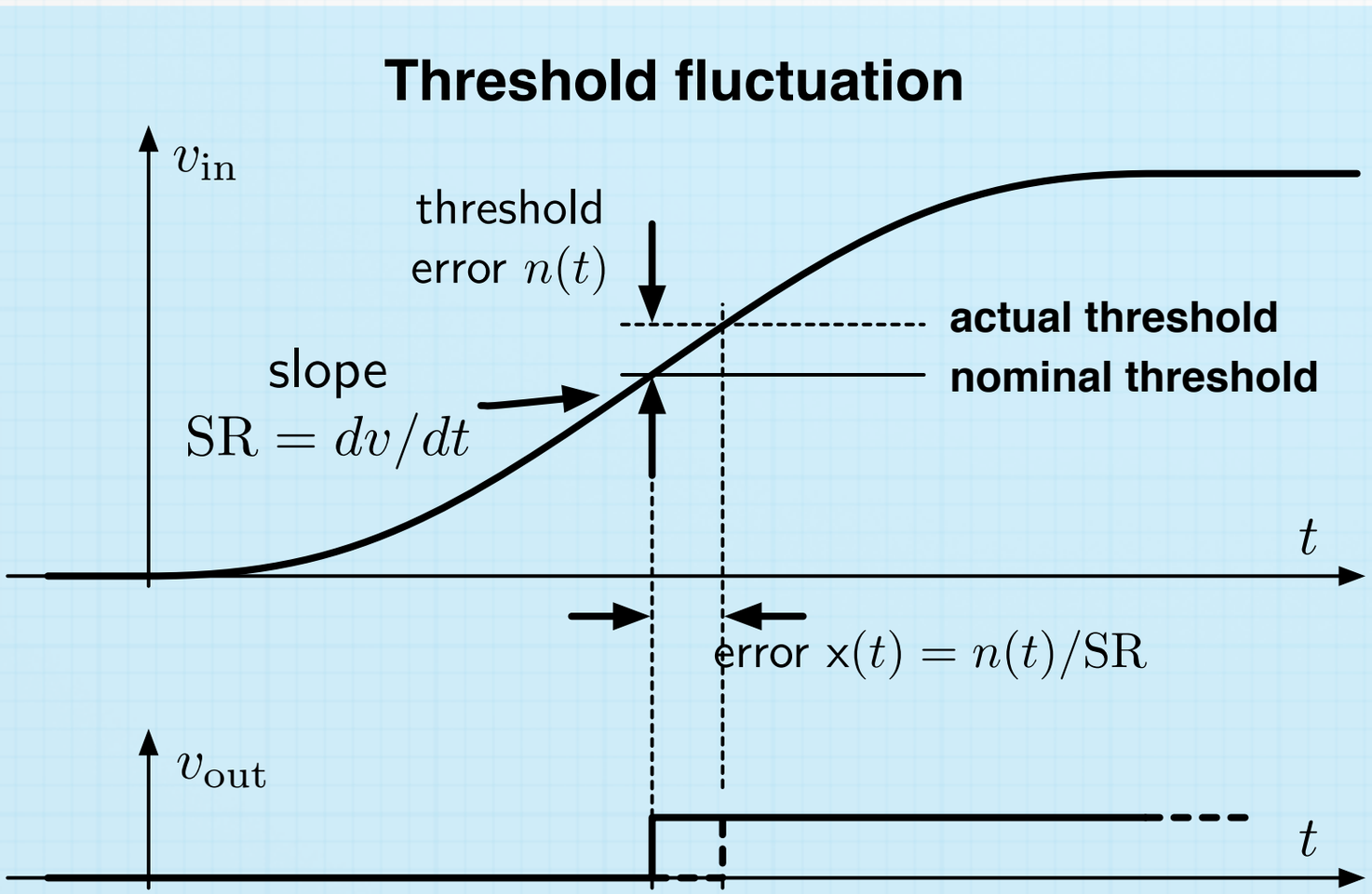
- Output can be synchronized to the clock
- Jitter cannot be smaller than
  - External clock signal
  - Clock input stage
  - Clock distribution
  - Output stage



Phase Noise in the Input Stage



Threshold fluctuation



mechanism

$$\text{x}(t) = \frac{n(t)}{(\text{SR})(t)}$$

$$\varphi(t) = \frac{2\pi\nu_0\, n(t)}{(\text{SR})(t)}$$

Phase Noise in the Input Stage

Sinusoidal signal

$$v(t) = V_0\,[1+\alpha(t)]\cos\left[2\pi\nu_0 t + \varphi(t)\right] \quad \Rightarrow \quad \mathrm{SR} = 2\pi\nu_0\,V_0$$

$$\mathrm{x}(t) = \frac{n(t)}{\mathrm{SR}} \qquad \longrightarrow \quad \mathrm{x}(t) = \frac{1}{2\pi\nu_0}\frac{n(t)}{V_0}$$

$$\varphi(t) = \frac{2\pi\nu_0\,n(t)}{\mathrm{SR}} \quad \longrightarrow \quad \varphi(t) = \frac{n(t)}{V_0}$$

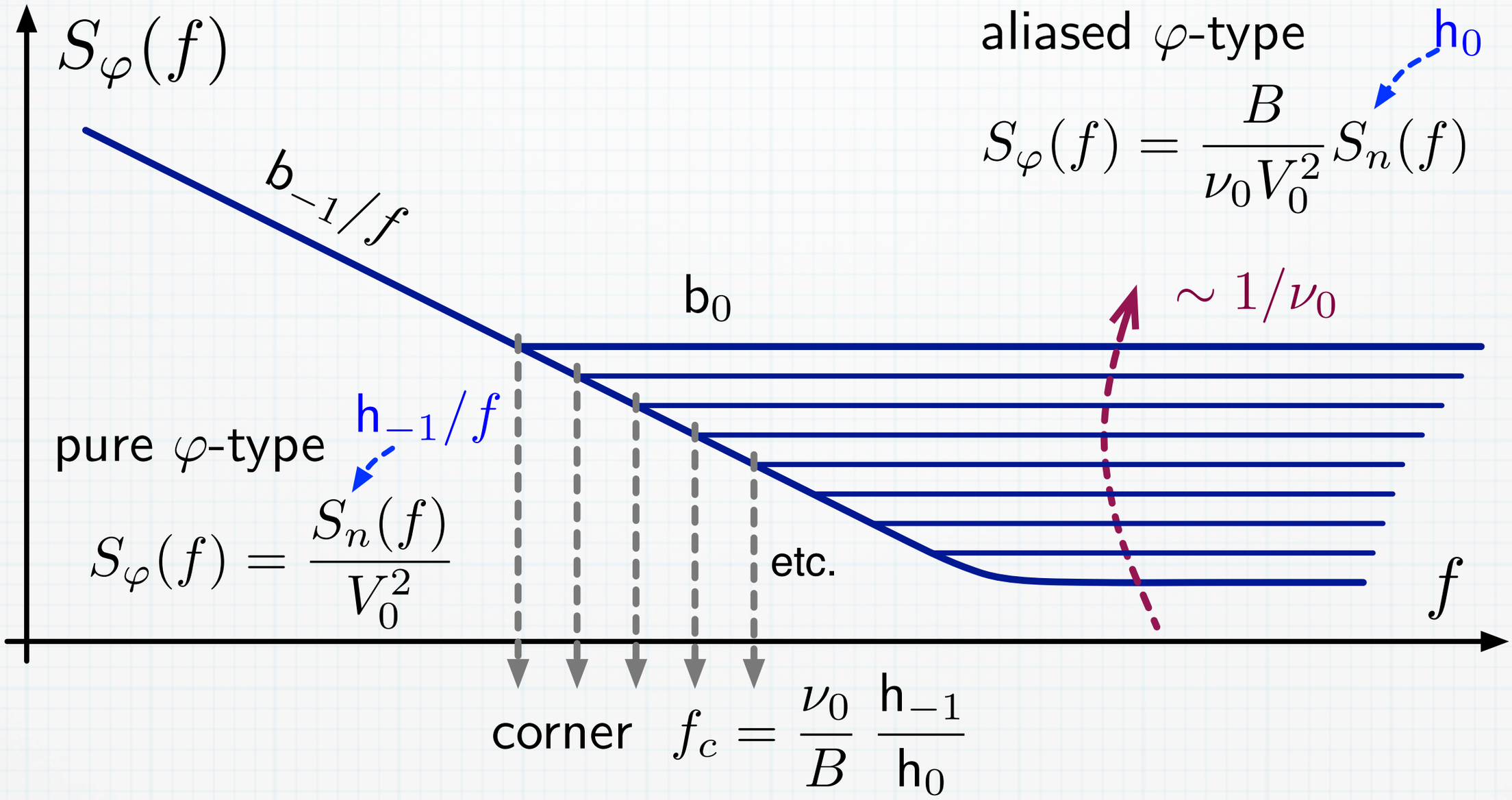
φ-type noise

$$S_\varphi(f) = \frac{S_n(f)}{V_0^2}$$

constant vs ν_0

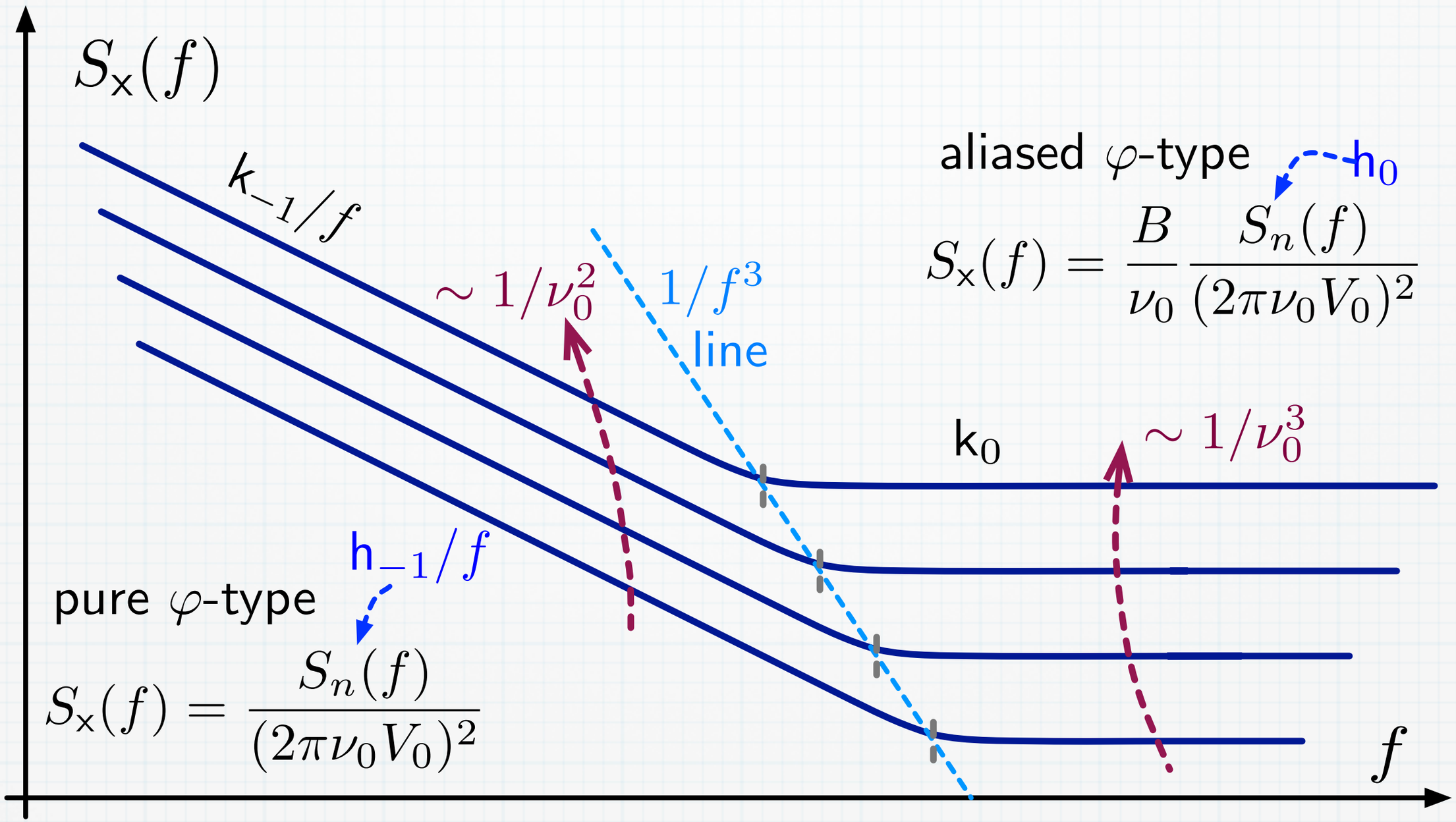
φ-type PM Noise

Remember that white noise is subject to aliasing, flicker is not



Power law $S_n(f) = \sum h_i f^i$ [do not mistake with $S_y(f)$]

φ-type Jitter



aliased φ-type

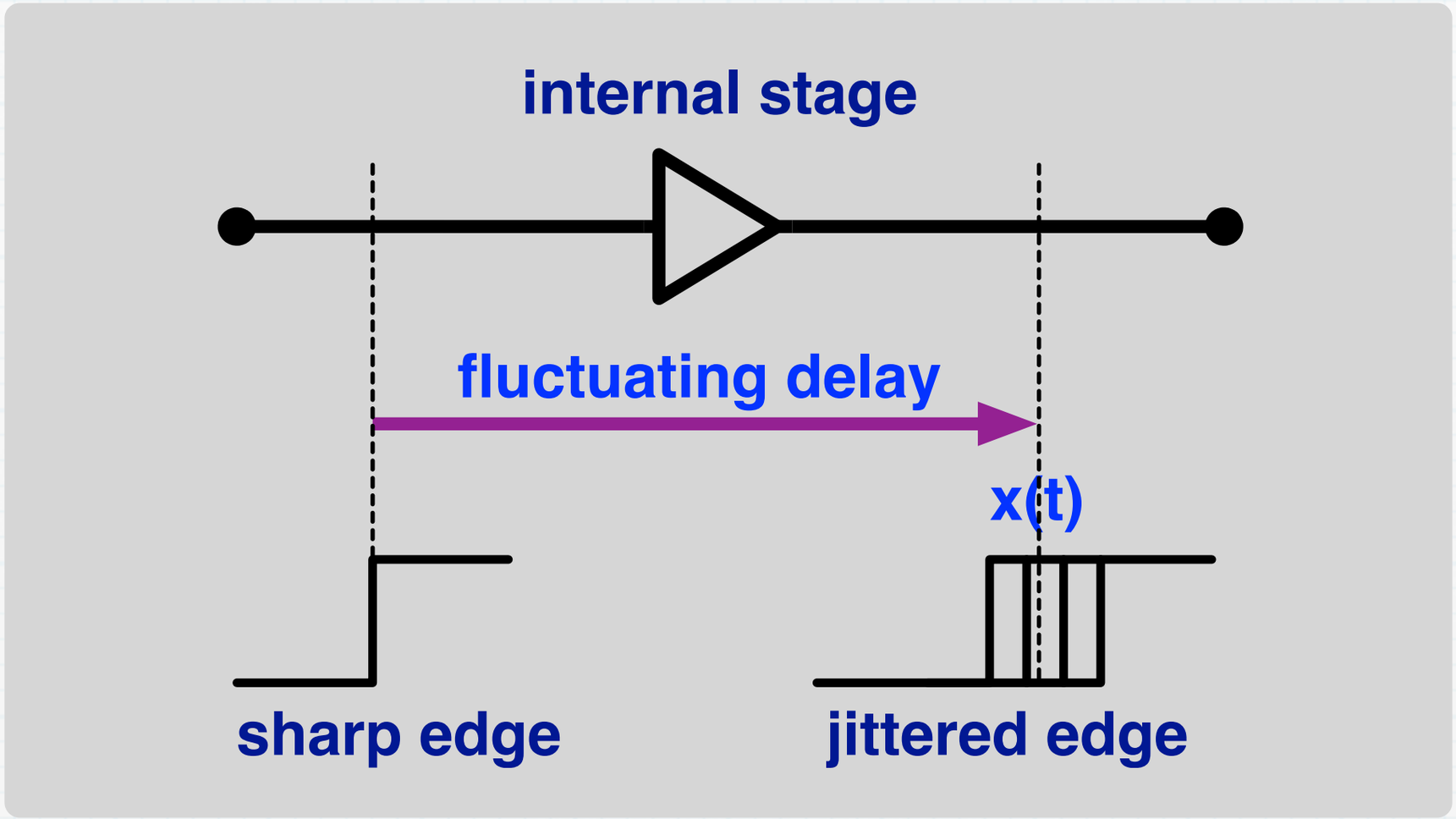
h_0

$$S_x(f) = \frac{B}{\nu_0} \frac{S_n(f)}{(2\pi\nu_0 V_0)^2}$$

Power law $S_x(f) = \sum k_i f^i$ and $S_n(f) = \sum h_i f^i$

Internal Delay Fluctuation

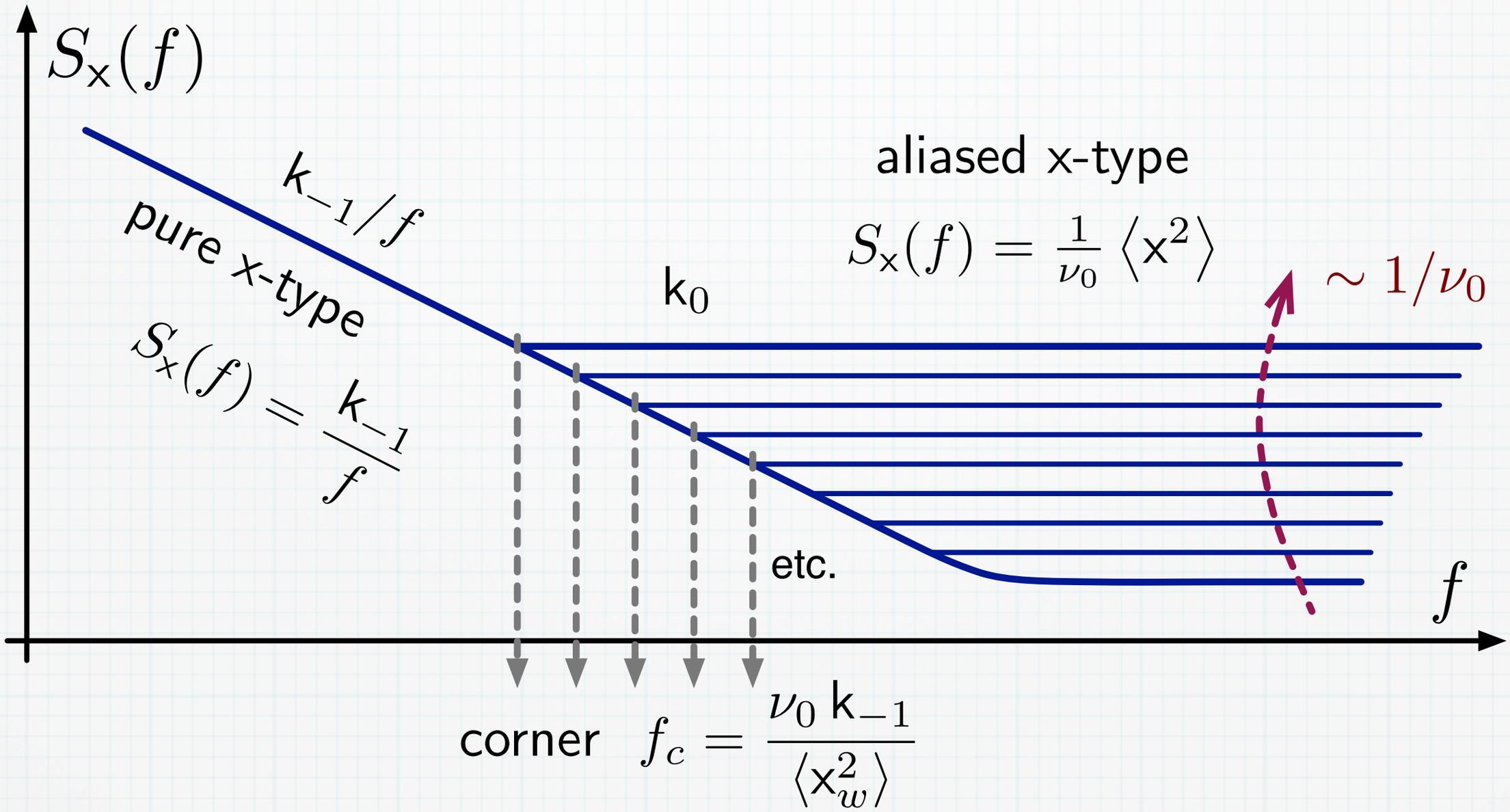
x-type noise



- The internal delay fluctuates by an amount x(t)
- This has nothing to do with threshold and frequency

x-type Jitter

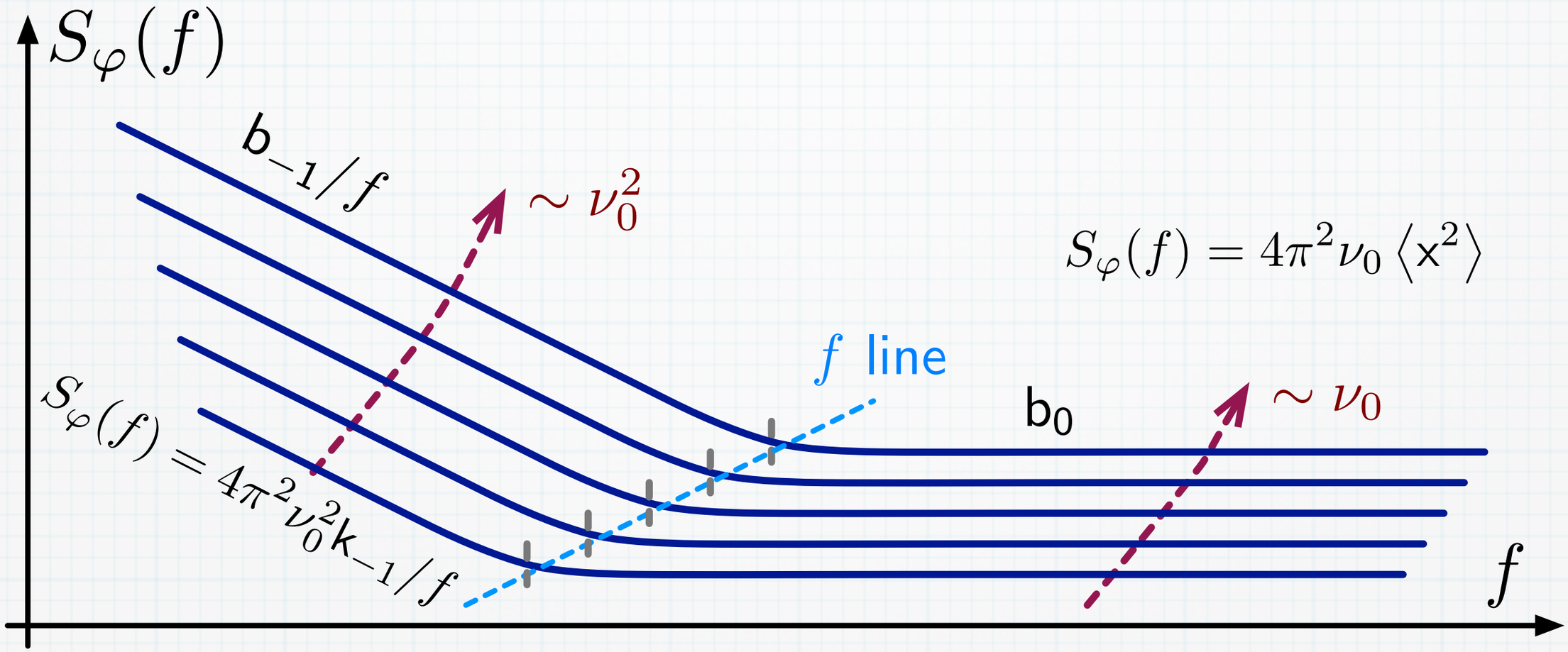
Remember that white noise is subject to aliasing, flicker is not



Power law $S_x(f) = \sum k_i f^i$

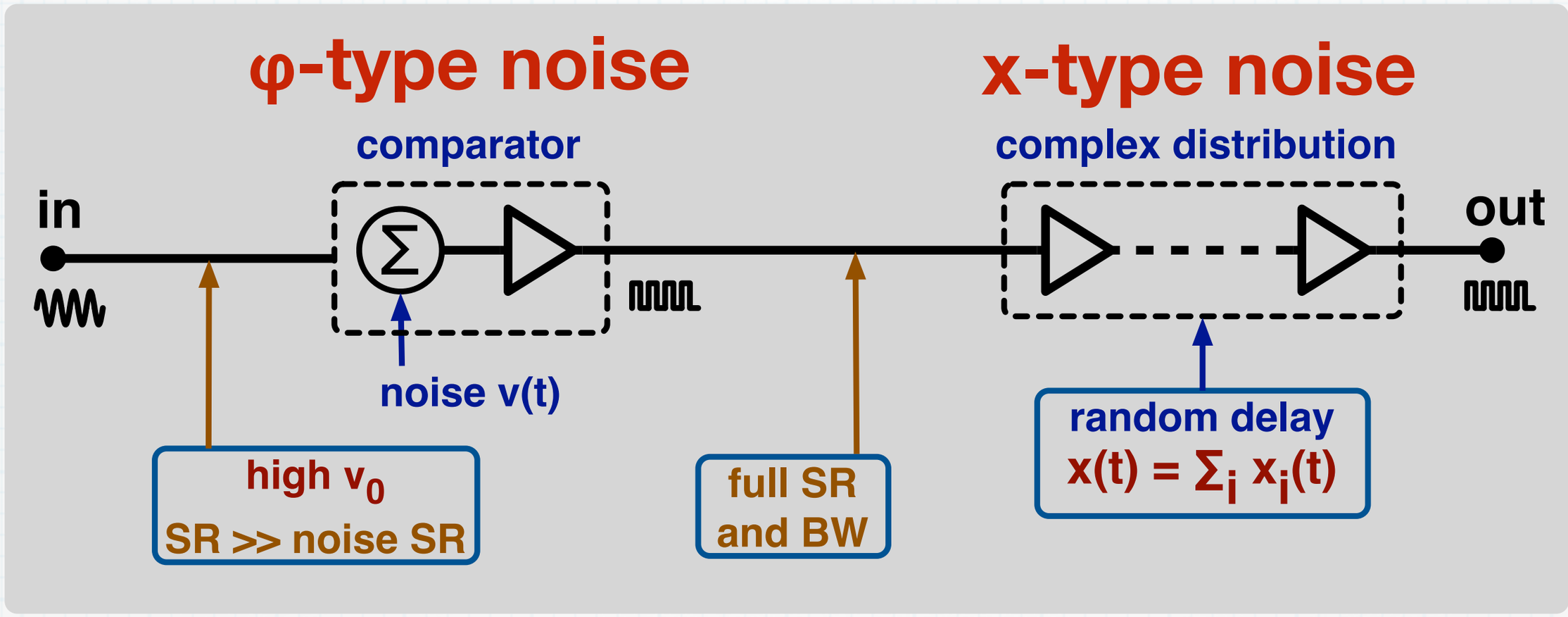
x-Type PM Noise

Remember that white noise is subject to aliasing, flicker is not



$$S_\varphi(f) = 4\pi^2\nu_0 \left\langle x^2 \right\rangle$$

Full Noise Mechanism



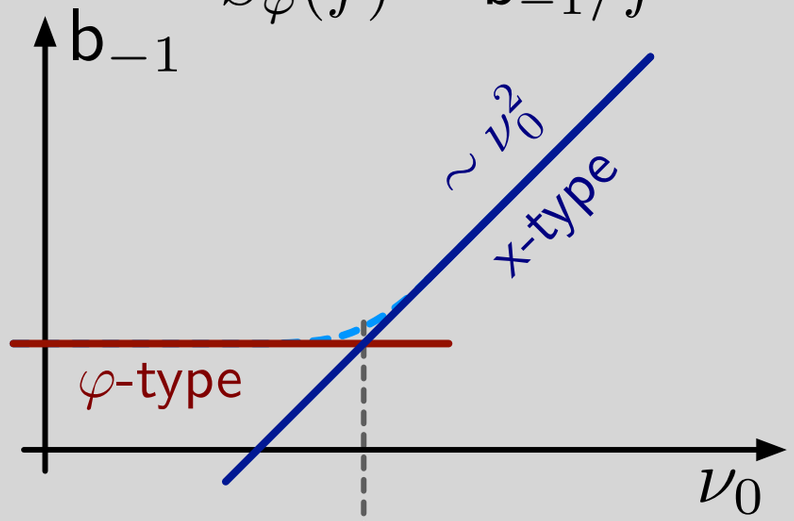
- The φ-type noise noise may show up or not, depending on input noise and SR
- At the comparator out, the edges attain full SR and bandwidth of the technology
- Complex distribution –> independent fluctuations add up

$$x(t) = \sum_i x_i(t) \quad \text{and} \quad \langle x^2(t) \rangle = \sum_i \langle x_i^2(t) \rangle$$

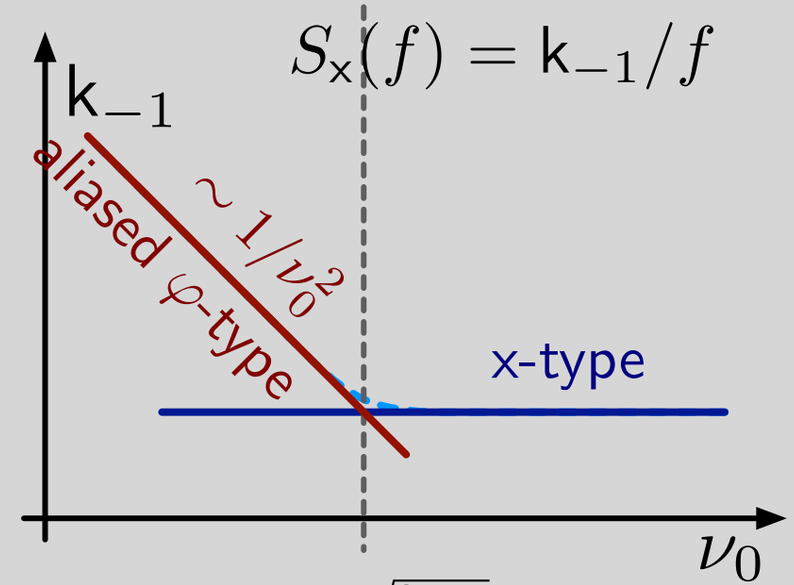
Full Noise Mechanism

Flicker (not aliased)

$$S_\varphi(f) = \mathsf{b}_{-1}/f$$



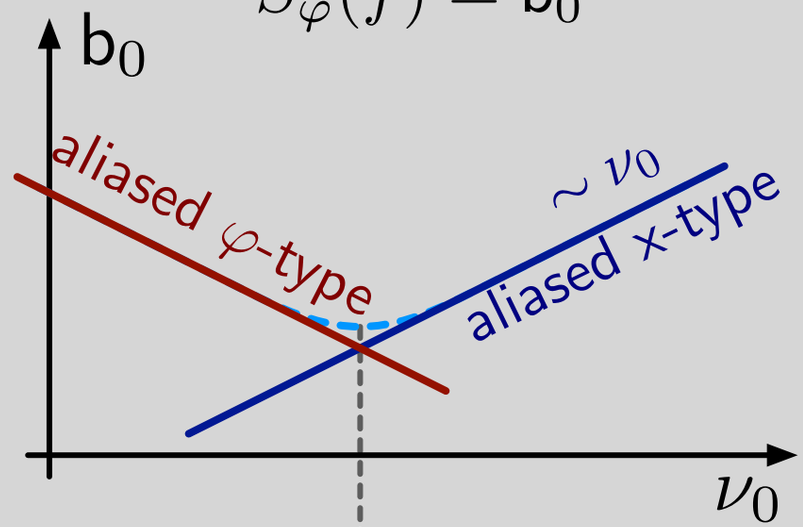
$$S_\mathsf{x}(f) = \mathsf{k}_{-1}/f$$



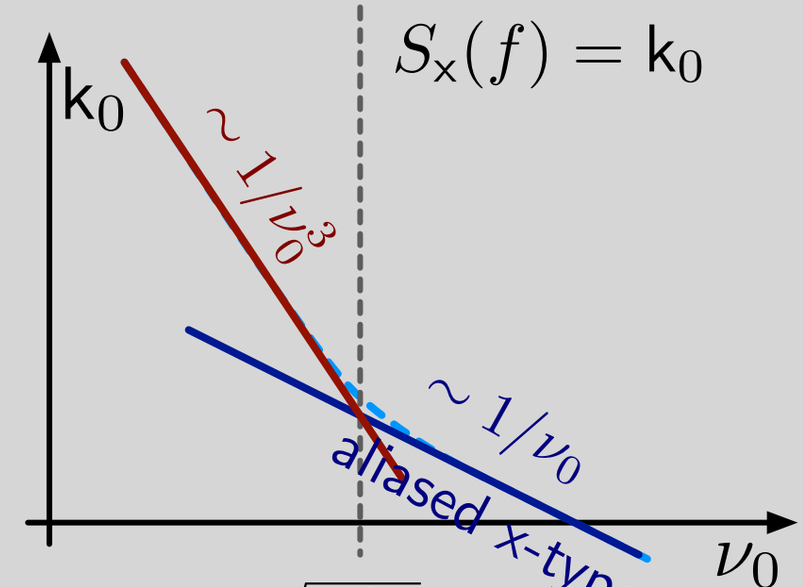
$$\frac{1}{2\pi V_0}\sqrt{\frac{\mathsf{h}_{-1}}{\mathsf{k}_{-1}}}$$

White (aliased)

$$S_\varphi(f) = \mathsf{b}_0$$



$$S_\mathsf{x}(f) = \mathsf{k}_0$$



$$\frac{1}{2\pi V_0}\sqrt{\frac{B\,\mathsf{h}_0}{\langle \mathsf{x}^2\rangle}}$$

Summary of the Noise Types

Noise class	Dependence on ν_0	
	$S_\varphi(f)$	$S_\mathrm{x}(f)$
Pure φ-type	C vs. ν_0	$1/\nu_0^2$
Aliased φ-type	$1/\nu_0$	$1/\nu_0^3$
Pure x-type	ν_0^2	C vs. ν_0
Aliased x-type	ν_0	$1/\nu_0$

- **Pure x-type. High speed circuits, inside the device. Must be 1/f, otherwise aliasing shows up**
- **Aliased x-type. High speed circuits, inside the device, at low switching frequency. The clock must be either high frequency sin(), or sharp square wave, so that the threshold has no effect.**

Noise Types and AVAR

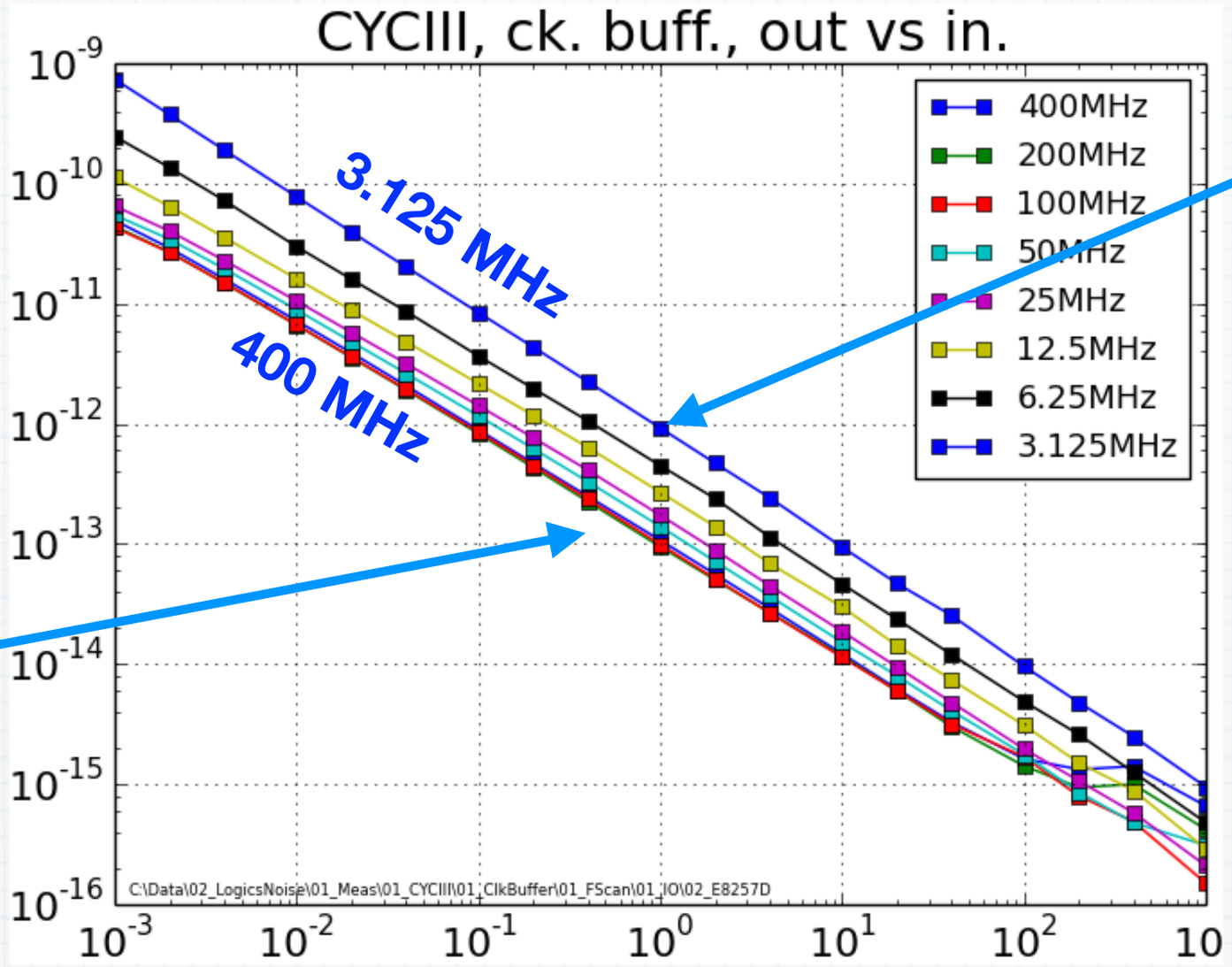
High frequency

$\sigma_y^2(\tau)$ indep. of ν_0

h_1 indep. of ν_0

$b_{-1} \sim \nu_0^2$

pure x type



Low frequency

$\sigma_y^2(\tau) \sim 1/\nu_0^2$

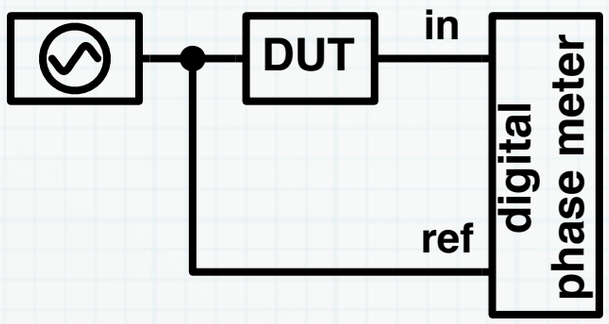
$h_1 \sim 1/\nu_0^2$

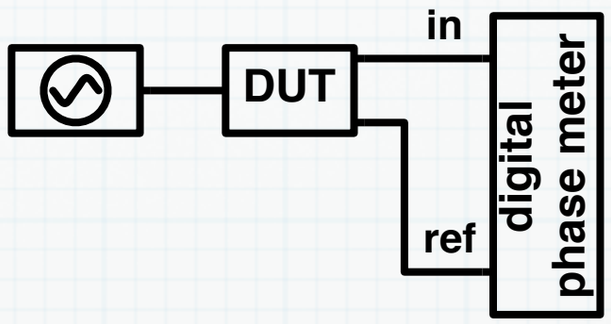
$b_{-1} = C$ vs. ν_0

pure φ type

Examples

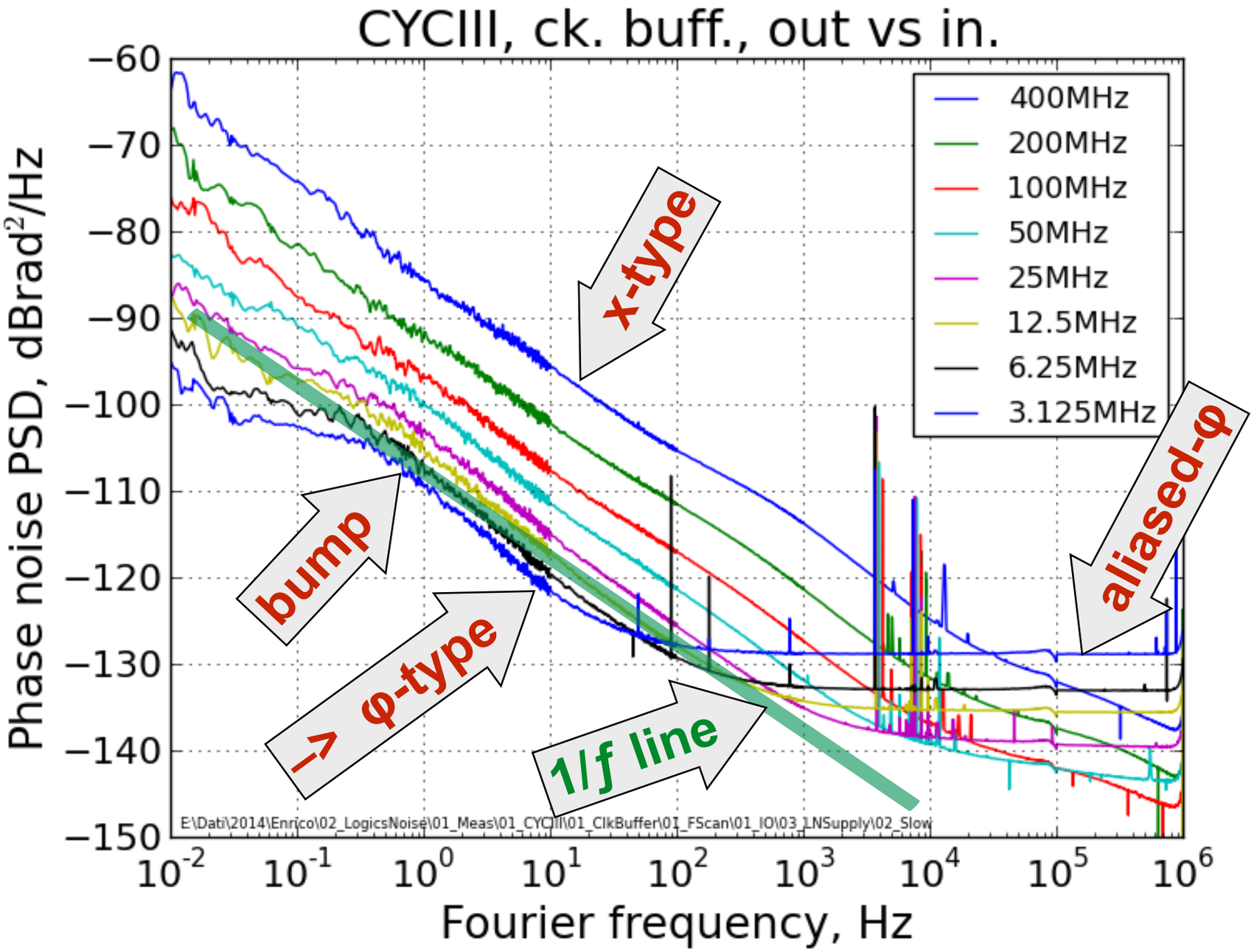
Measurements are performed with the Symmetricom (Microsemi) DS 5125 and DS 5120 dual-channel phase meter

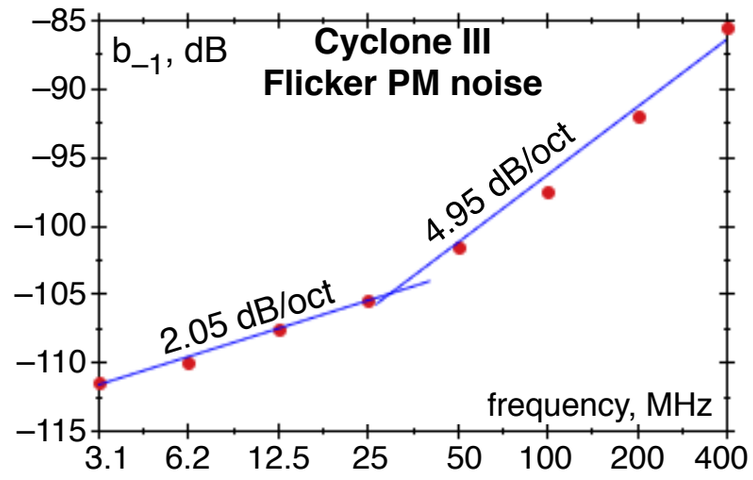


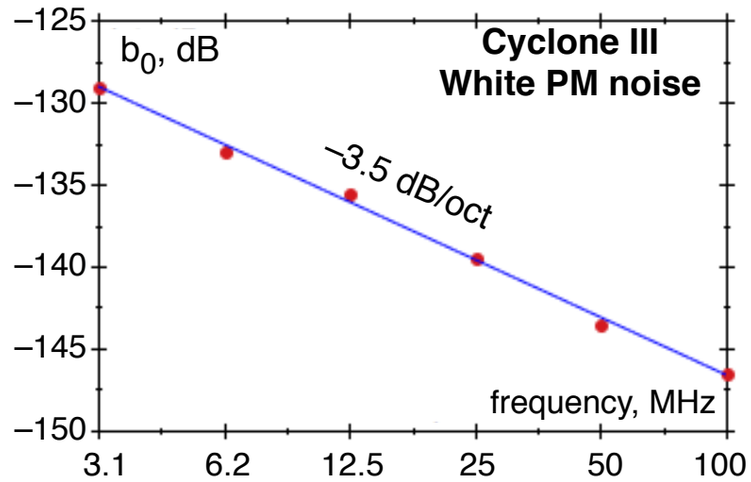


Allow (input frequency) ≠ (ref frequency)

Cyclone III Clock Buffer







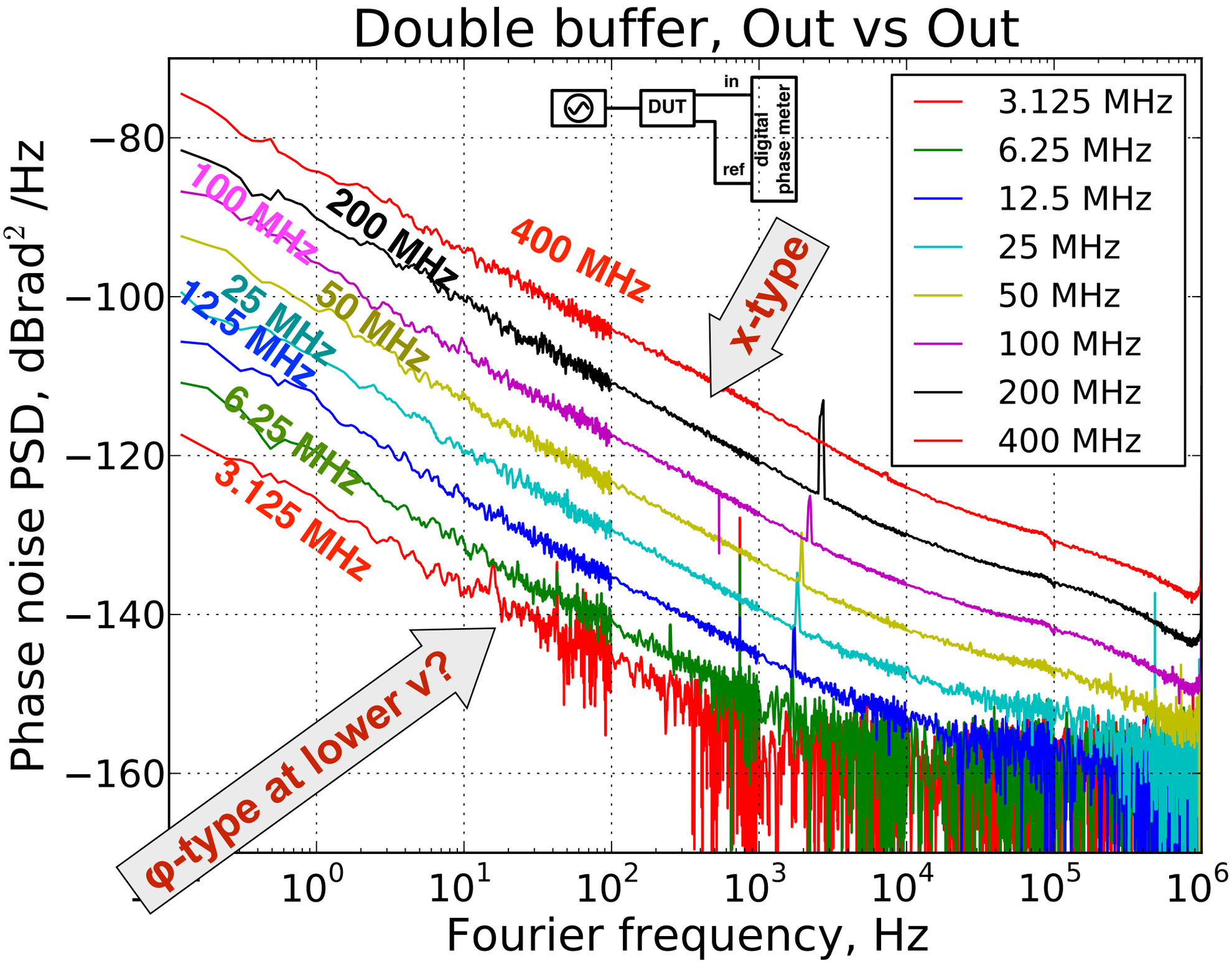
Flicker

- High v_0 –> scales as v_0 (x-type)
- Low v_0, –> to φ-type (bumps 0.1–10 Hz)

White

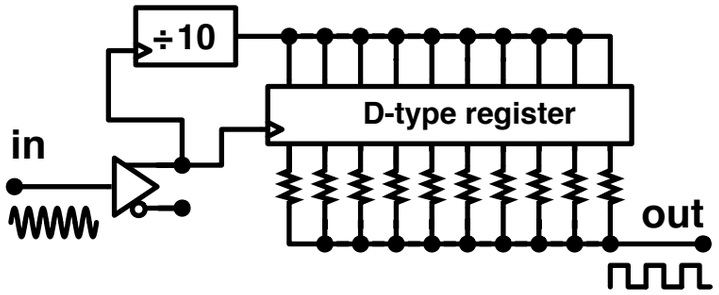
- Aliasing shows up at low v_0

Cyclone III Output Buffer

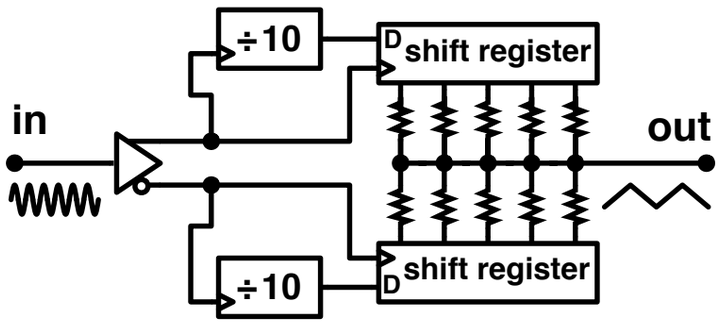


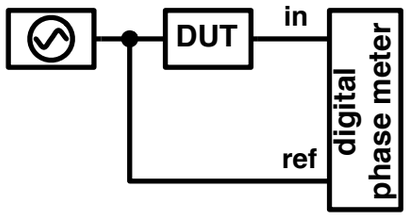
MAX 3000 CPLD [300 nm] (1)

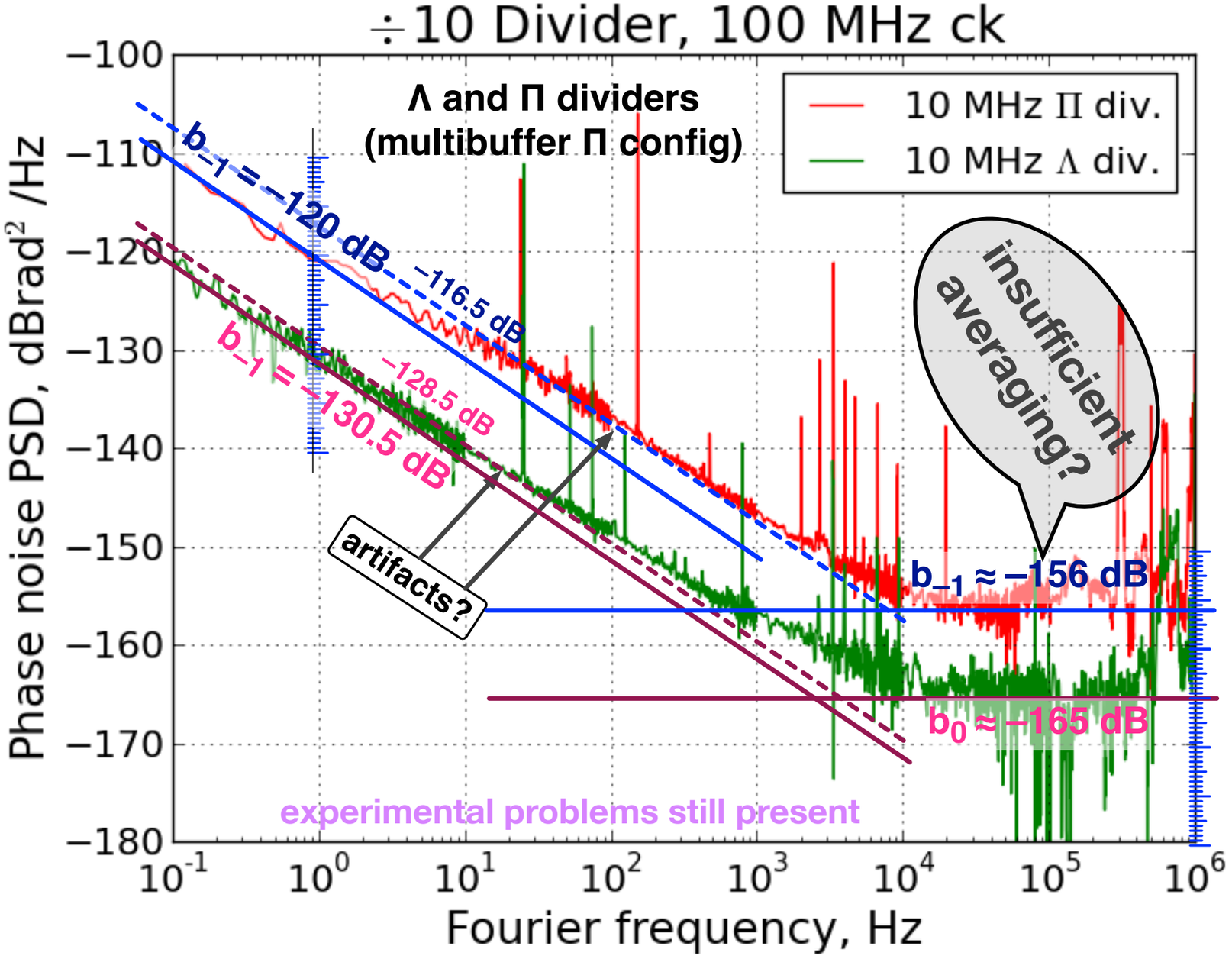
Π divider



Λ divider

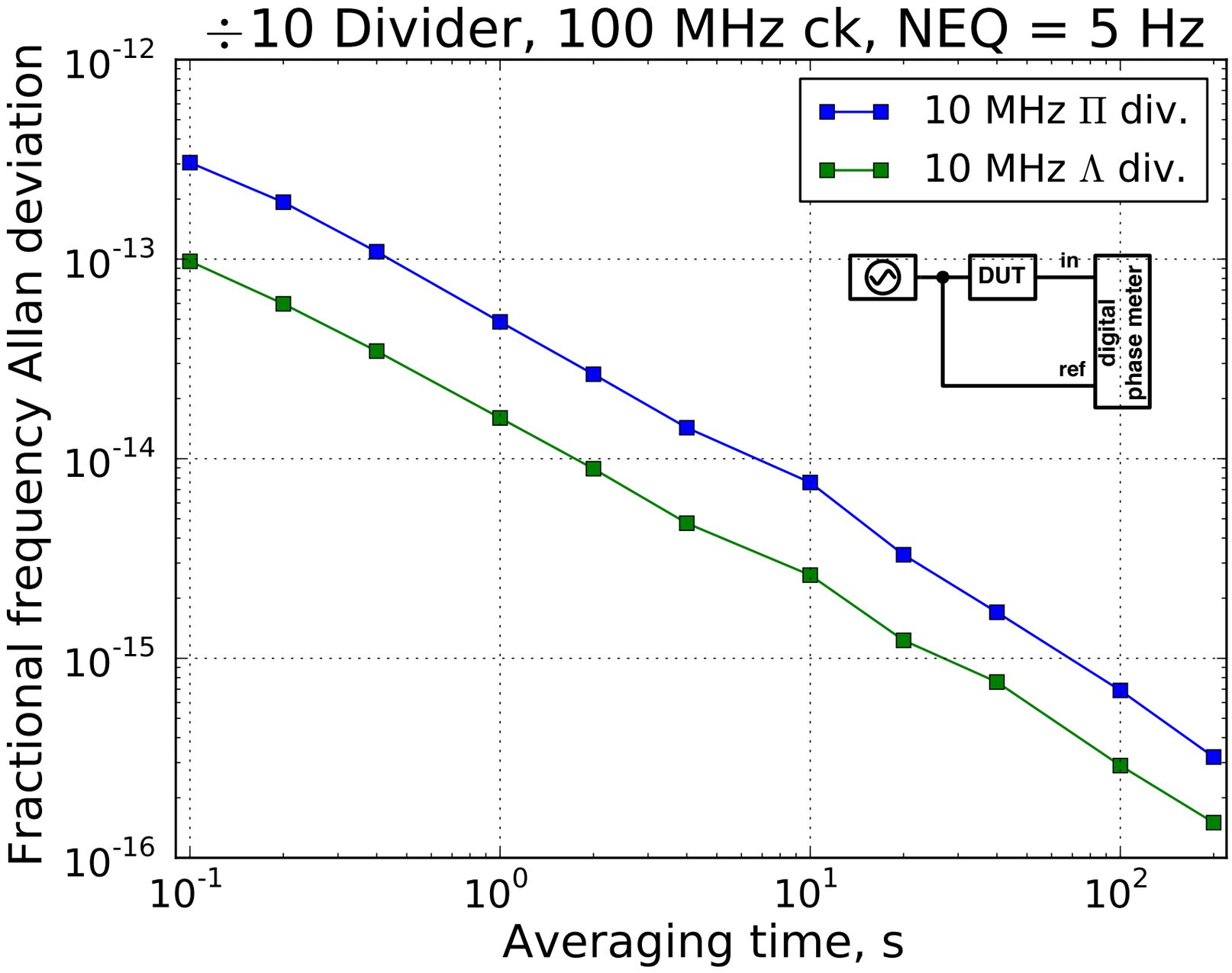






- **Flicker region –> Negligible aliasing**
- **The Π divider is still not well explained**
- **The Λ divider exhibits low 1/f and low white noise**

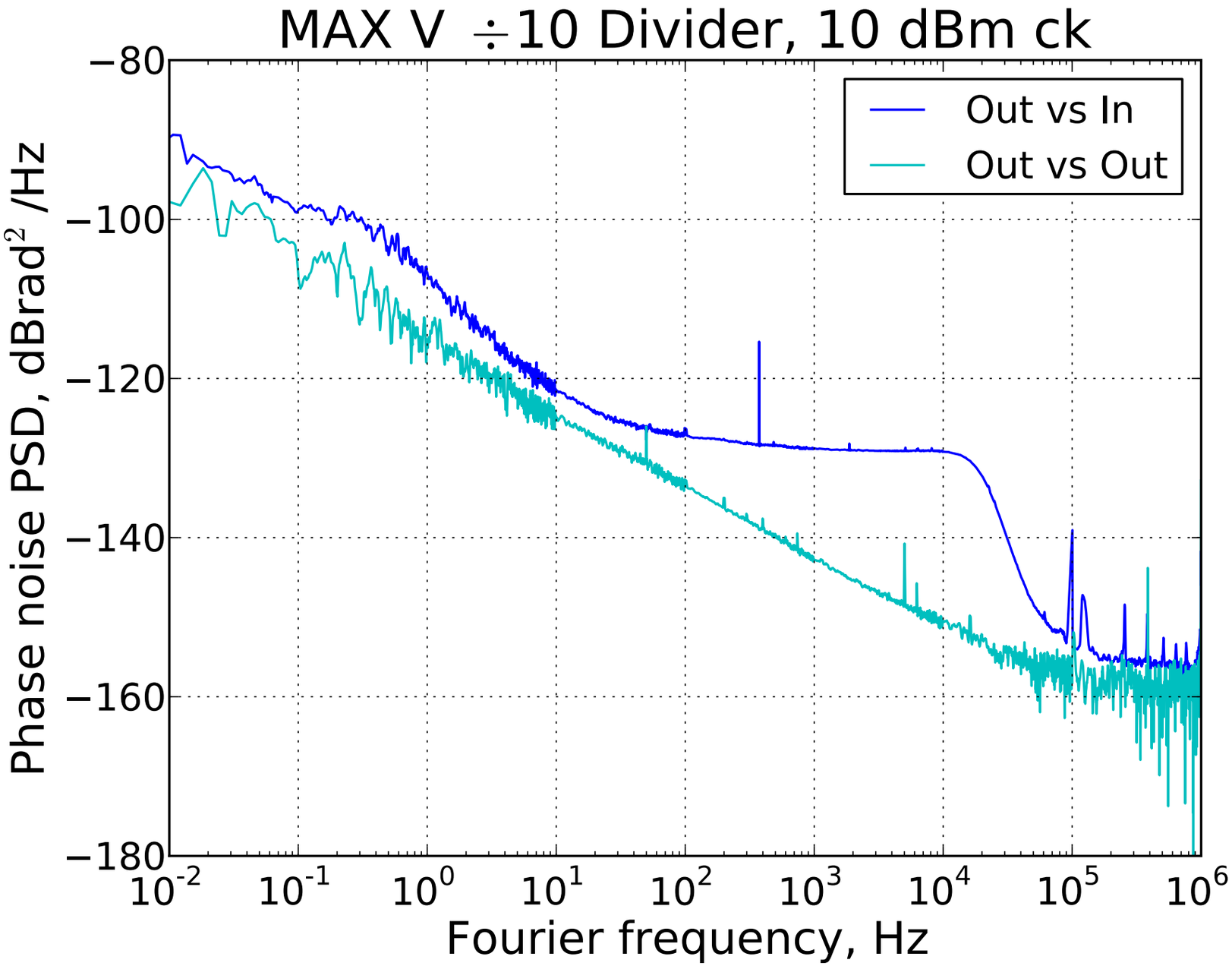
MAX 3000 CPLD [300 nm] (2)



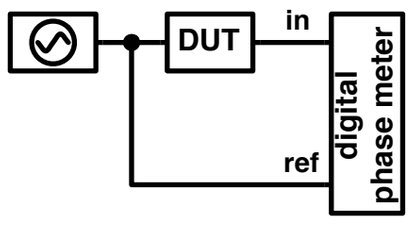
- **Slope 1/τ, typical of white and flicker PM noise**
- **The Λ divider performs 2×10^{-14} at τ = 1 s, 10 MHz output**

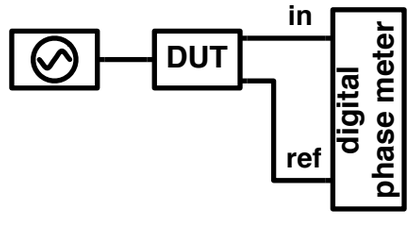
Max V CPLD [180 nm]

We do not trust this spectrum (bump –> supply voltage?)



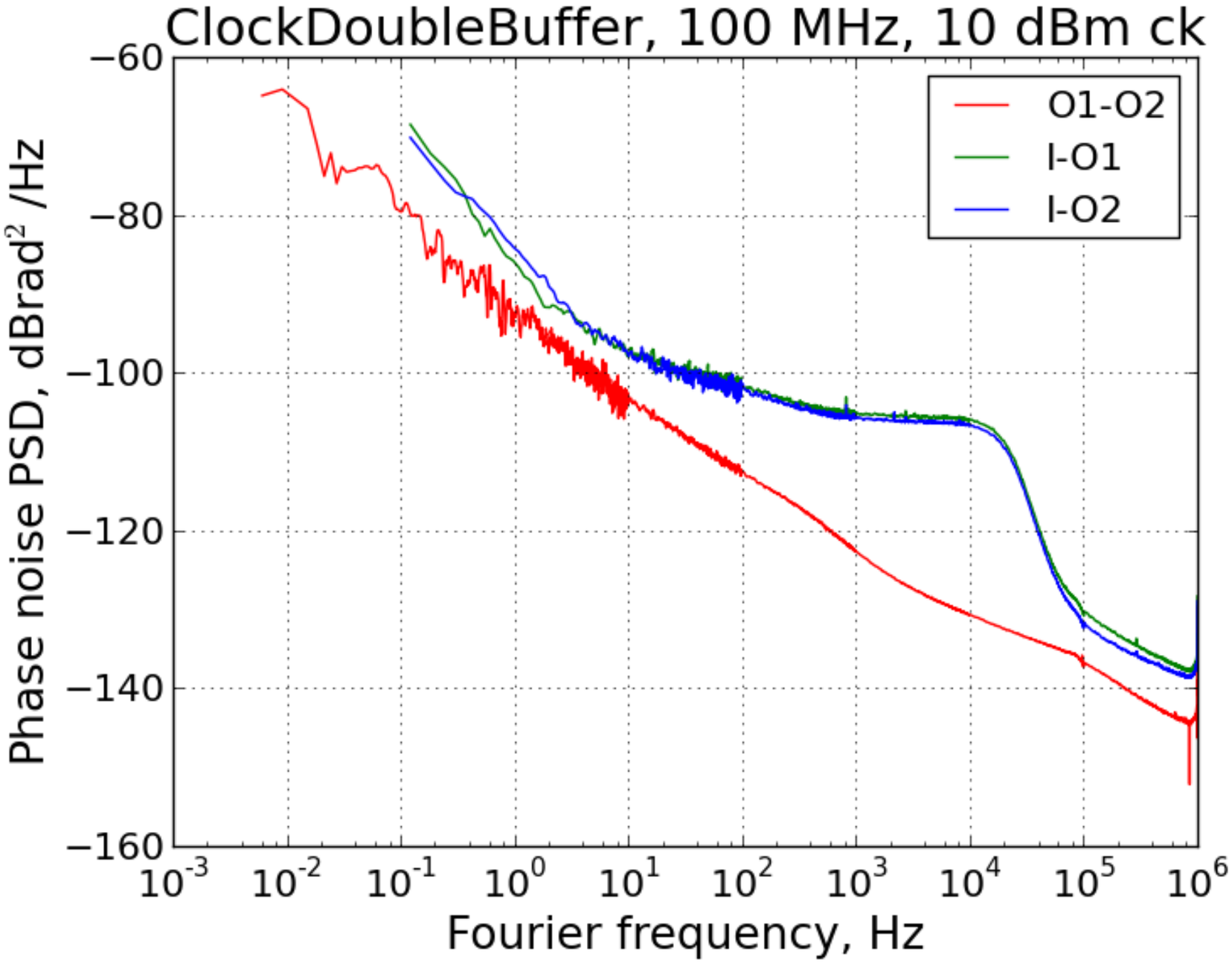
- **Two lambda dividers**
  - **output-to-output and common clock,**
  - **low f, emphasizes the 1/f noise**
- **Same, only output-to-output and common clock**





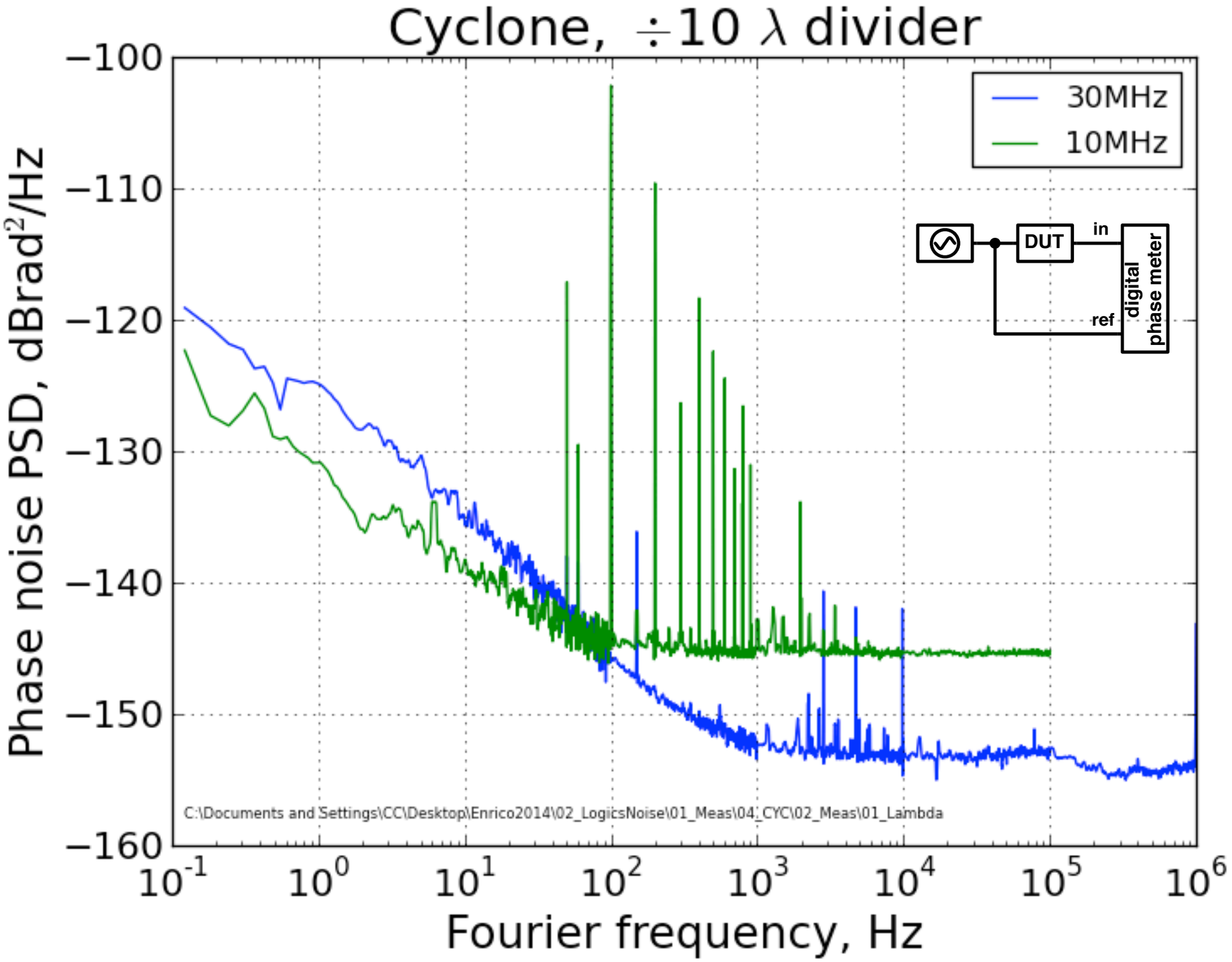
Max V CPLD [180 nm]

We do not trust this spectrum (bump –> supply voltage?)

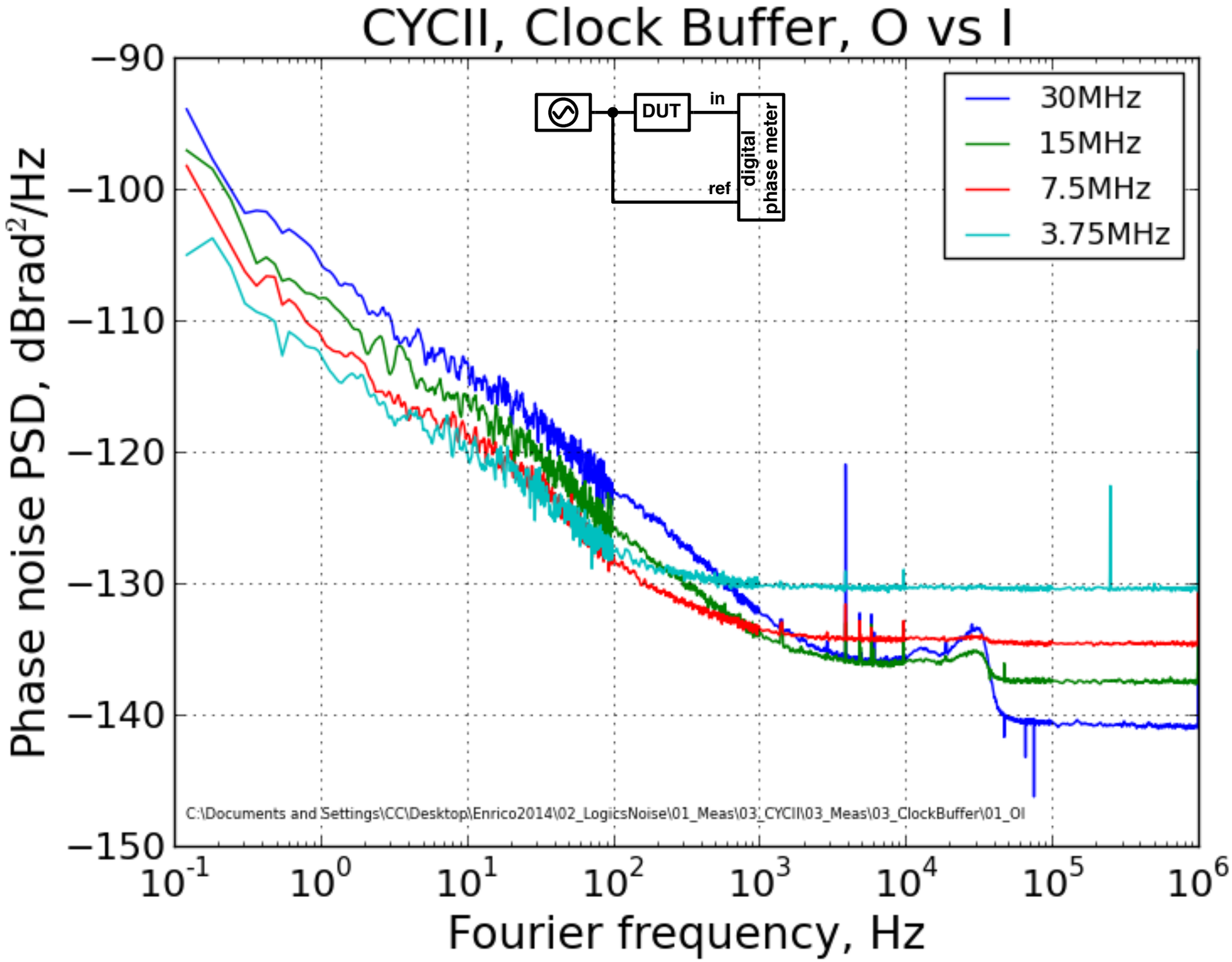


- Two lambda dividers
  - output-to-output and common clock,
    - low f, emphasizes the $1/f$ noise
- Clock, difference between the two outputs

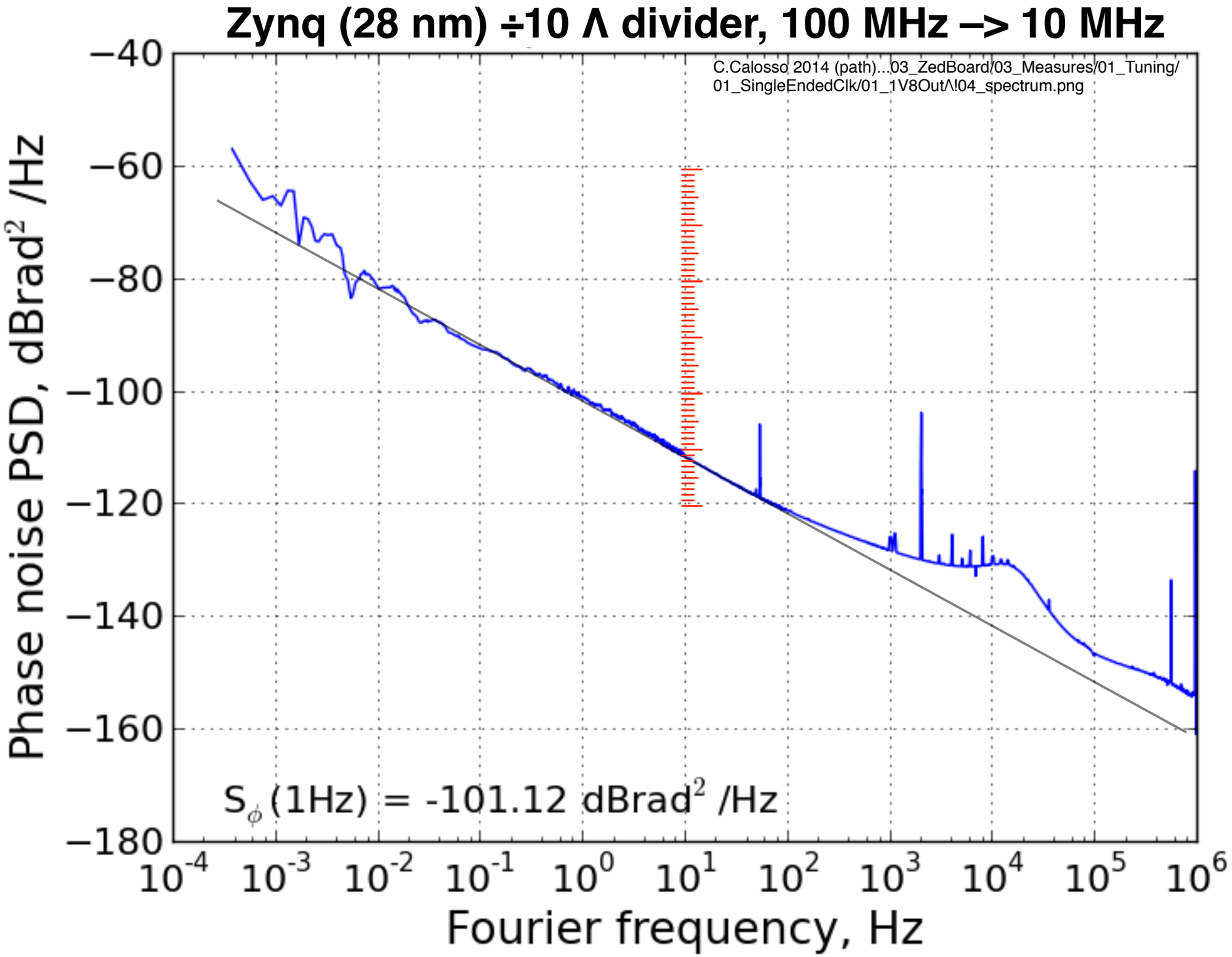
Cyclone II Λ Divider [90 nm]



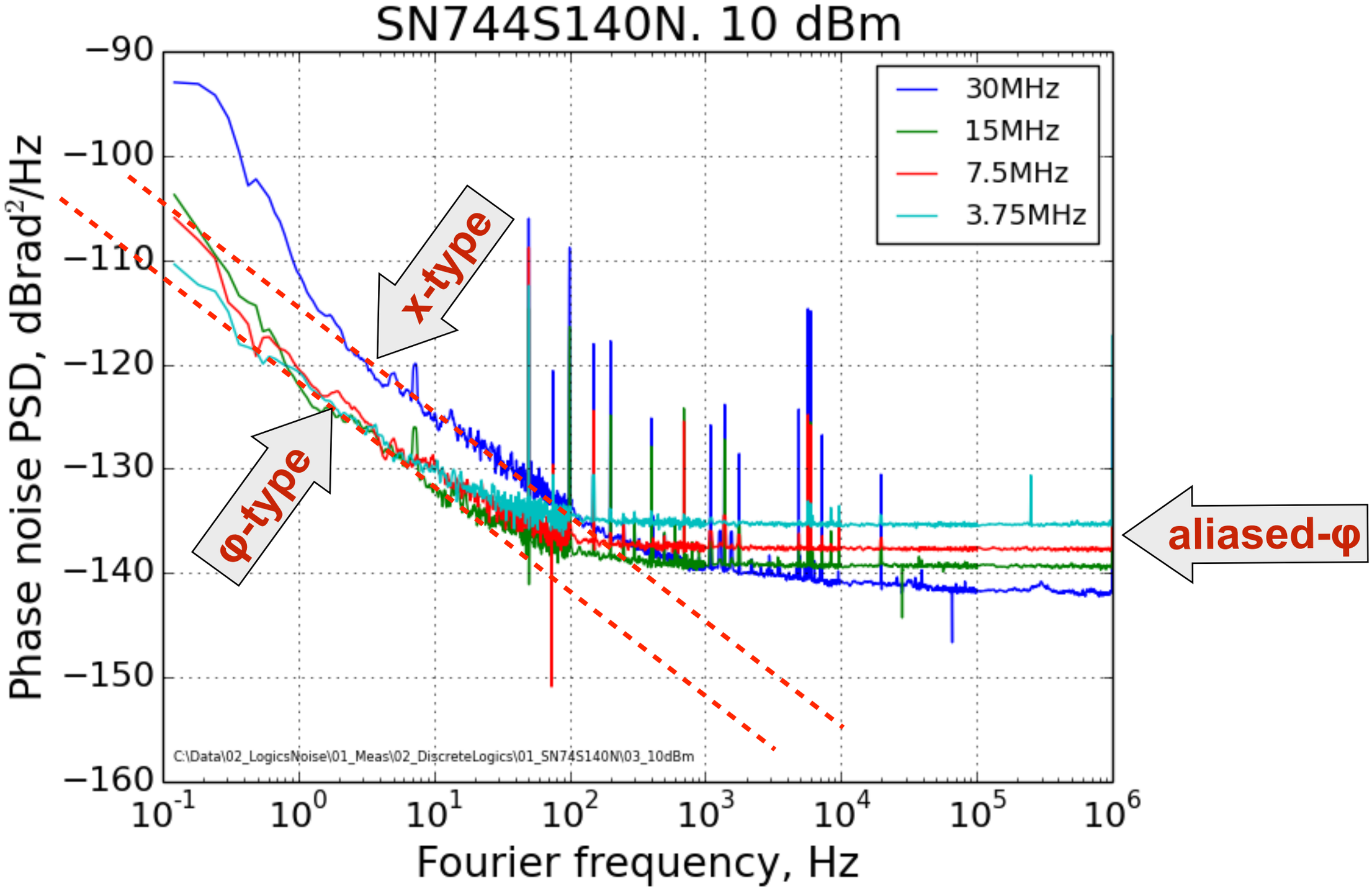
Cyclone II Clock Buffer [90 nm]



Zynq (28 nm), Λ Divider



74S140 – Old TTL 50 Ω Driver

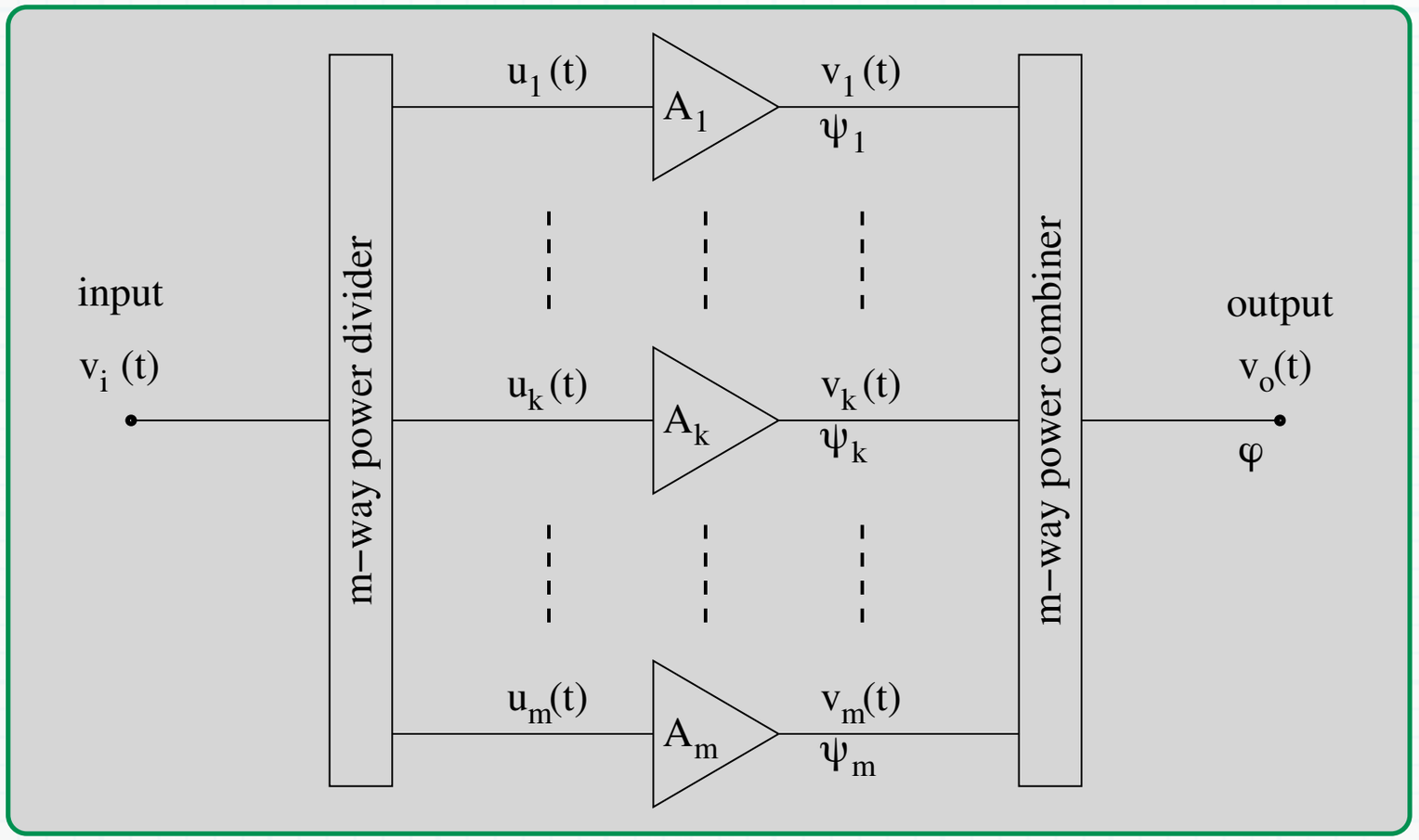


Some Facts

Related to Phase and Noise

- Volume Law
- Input Chatter
- Internal PLL
- Thermal Effects
- ……

Rationale for the Volume Law



$$b_{-1} = \frac{1}{m}\left[b_{-1}\right]_{\text{cell}}$$

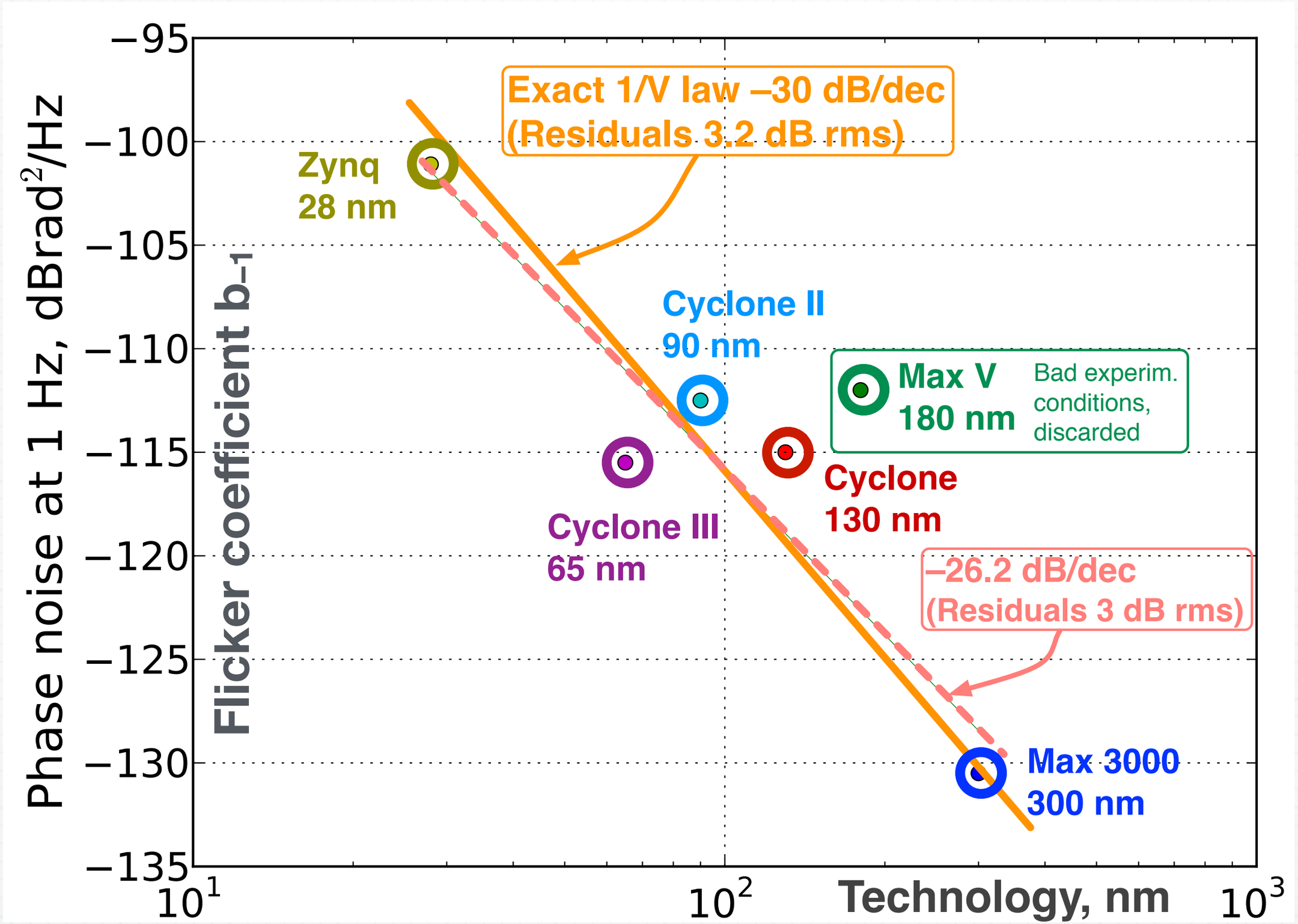
- Flicker coeff b_{-1} is ≈ independent of power
- The flicker of a branch is not increased by splitting the input power
- The carrier adds up coherently, the phase noise adds up statistically
- Hence, the 1/*f* phase noise is reduced by a factor m

Gedankenexperiment

- Flicker is of microscopic origin (Gaussian —> central limit theorem)
- Join the m branches of a parallel device forming a compound
- 1/*f* PM is proportional to the inverse size of the active region

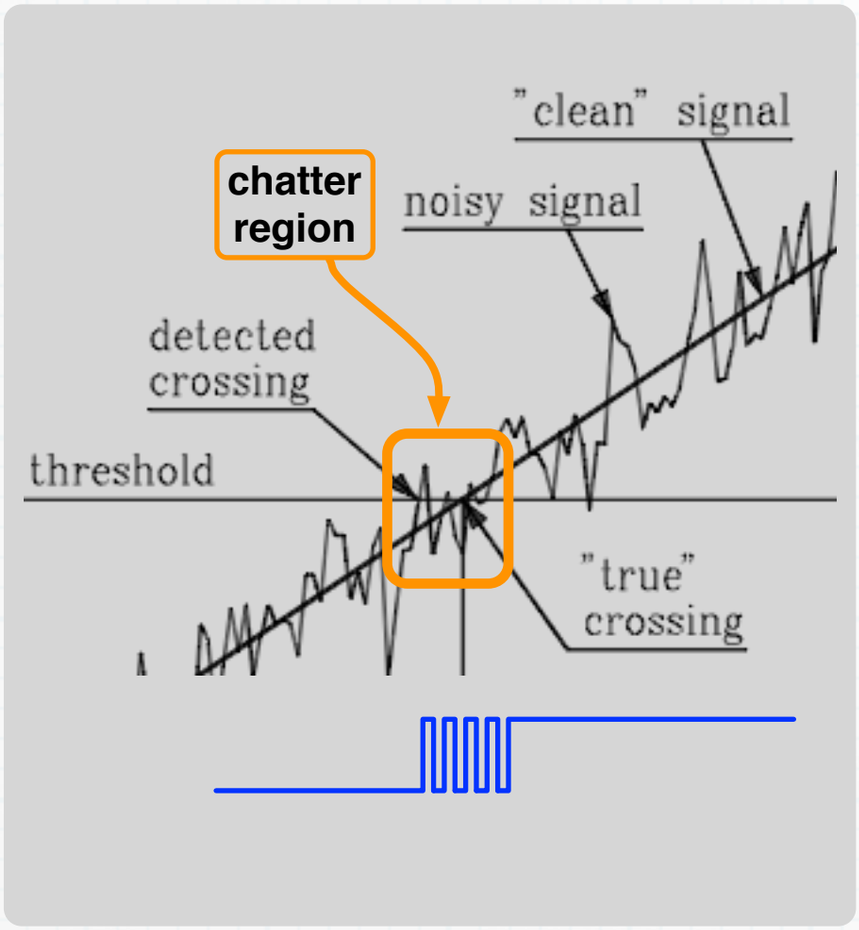
E. Rubiola, Phase Noise and Frequency Stability in Oscillators, Cambridge 2008, ISBN 978-0521-88677-2

The Volume Law!



Details in file DevicesComparison.doc

Input Chatter (1/3)



Chatter occurs when the RMS Slew Rate of noise exceeds the slew rate of the pure signal

Pure signal

$$v(t) = V_0 \cos(2\pi\nu_0 t)$$

$$\mathrm{SR} = 2\pi\nu_0 V_0$$

Wide band noise

$$\langle \mathrm{SR}^2 \rangle = 4\pi^2 \int_0^B f^2 S_V(f)\, df$$

$$= \frac{4\pi^2}{3} \sigma_V^2 B^2 \quad \text{(rms)}$$

Chatter threshold

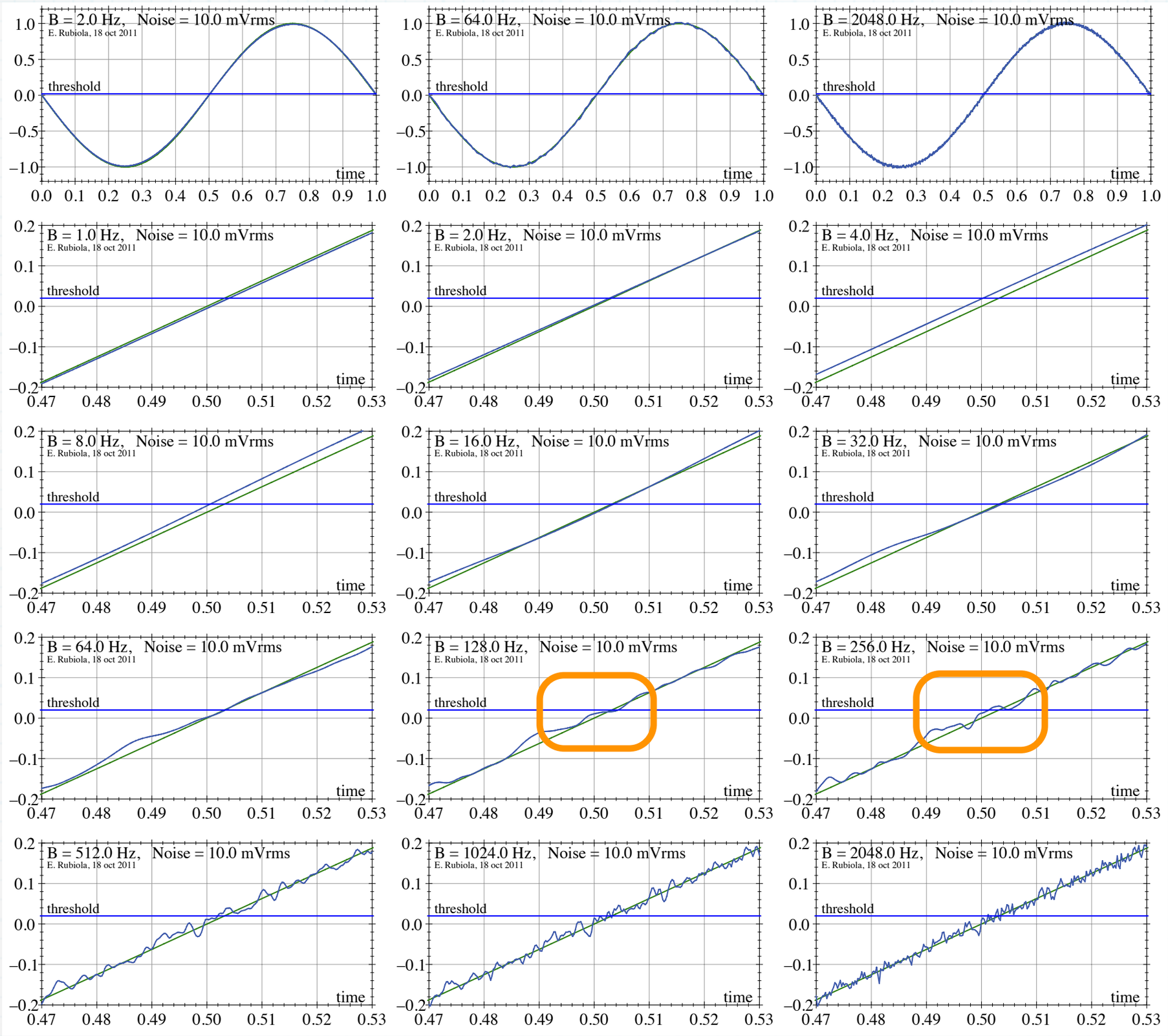
$$\nu_0^2 = \frac{1}{3} \frac{S_v B^3}{V_0^2}$$

Example

- V_0 = 100 mV peak
- 10 nV/√Hz noise
- 650 MHz max –> 2 GHz noise BW
- Chatter threshold ν = 5.2 MHz

With high-speed devices, chatter can occur at unexpectedly high frequencies

Simulation of Chatter (2/3)



Conditions

v_0 = 1 Hz,

V_0 = 1 V_{peak}

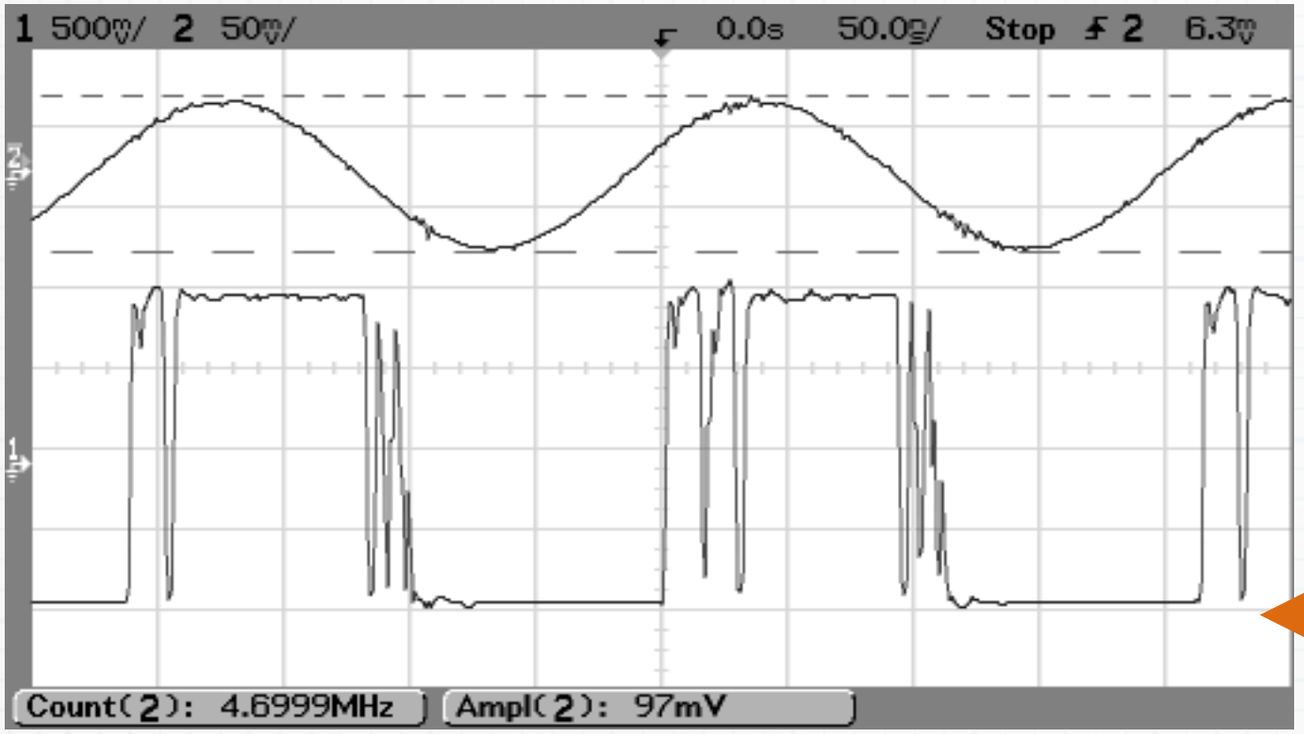
$\sqrt{\langle v_0^2 \rangle}$ = 10 mV rms noise

Noise BW increases in powers of 2

De-normalize for your needs

Input Chatter – Example (3/3)

Good agreement with theory

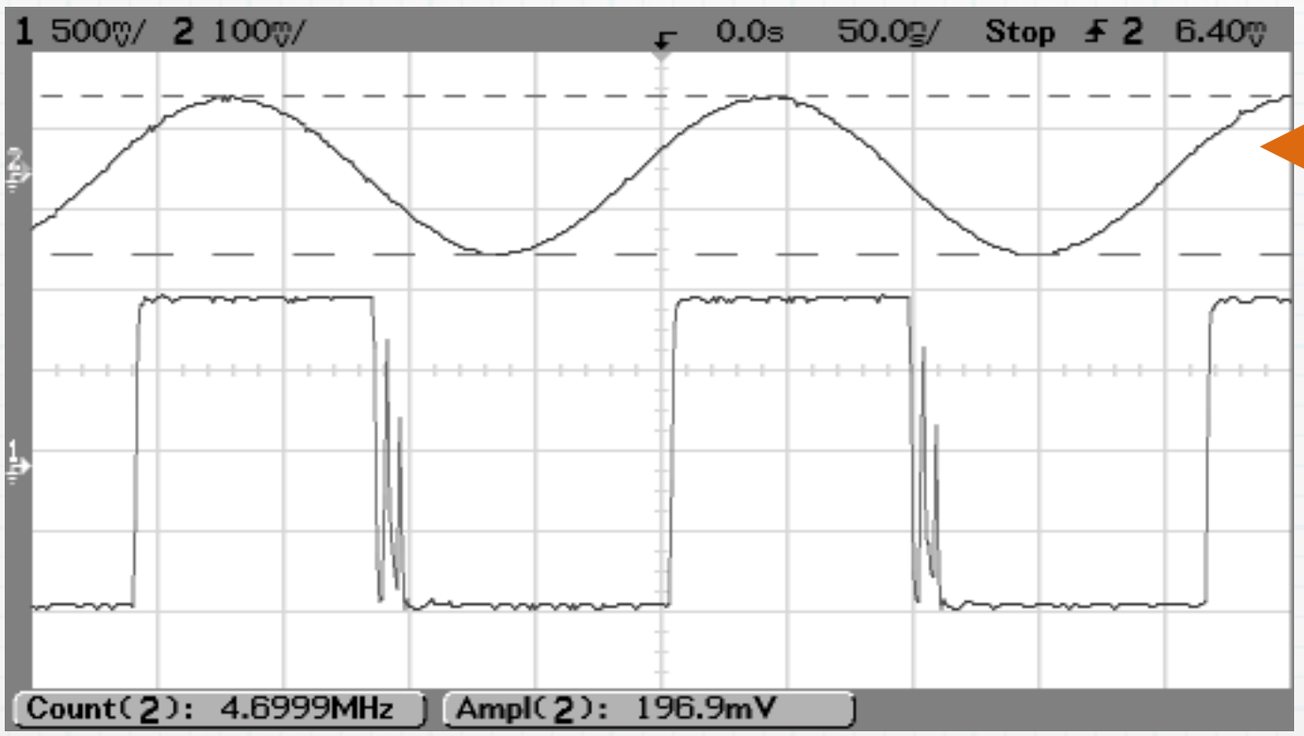


Experiment

- Cyclone III FPGA
- Estimated noise 10 nV/√Hz
- Estimated BW 2 GHz

V_0 = 50 mV (100 mV_{pp})

ν_0 = 4.7 MHz



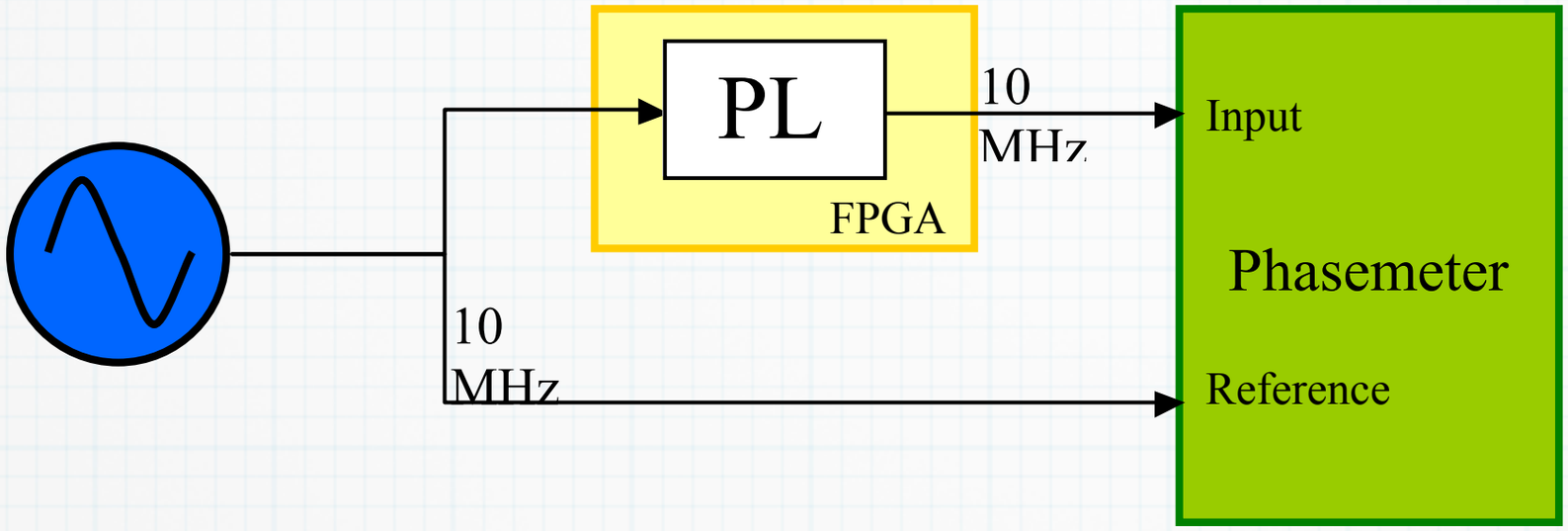
V_0 = 100 mV (200 mV_{pp})

ν_0 = 4.7 MHz

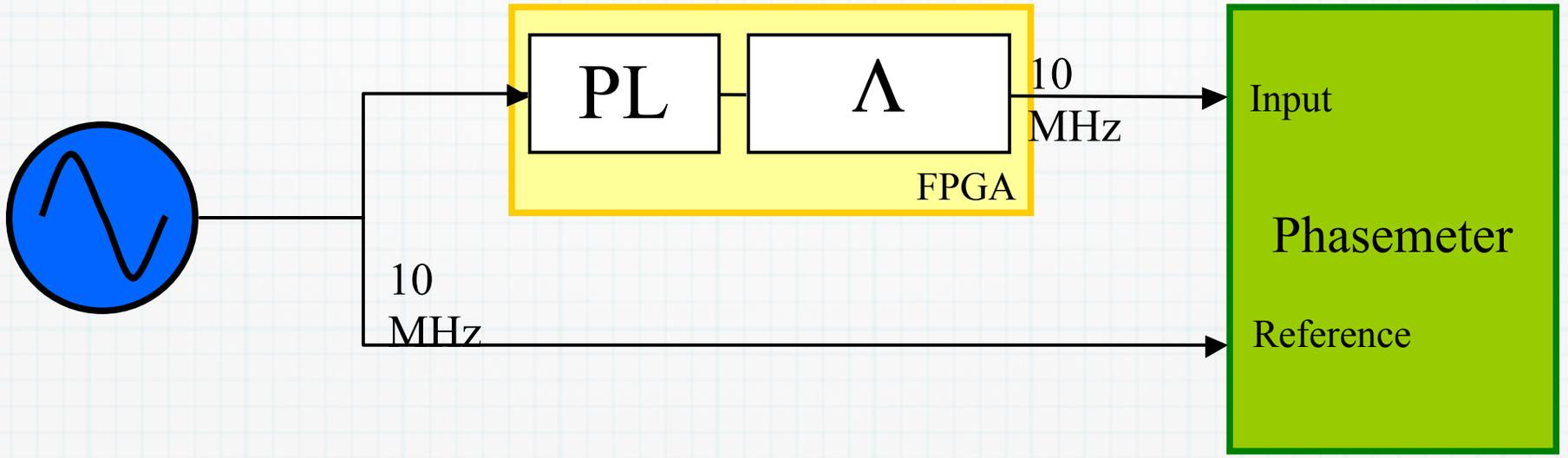
Asymmetry shows up

Explanation takes a detailed electrical model, which we have not

Cyclone III Internal PLL (1/4)

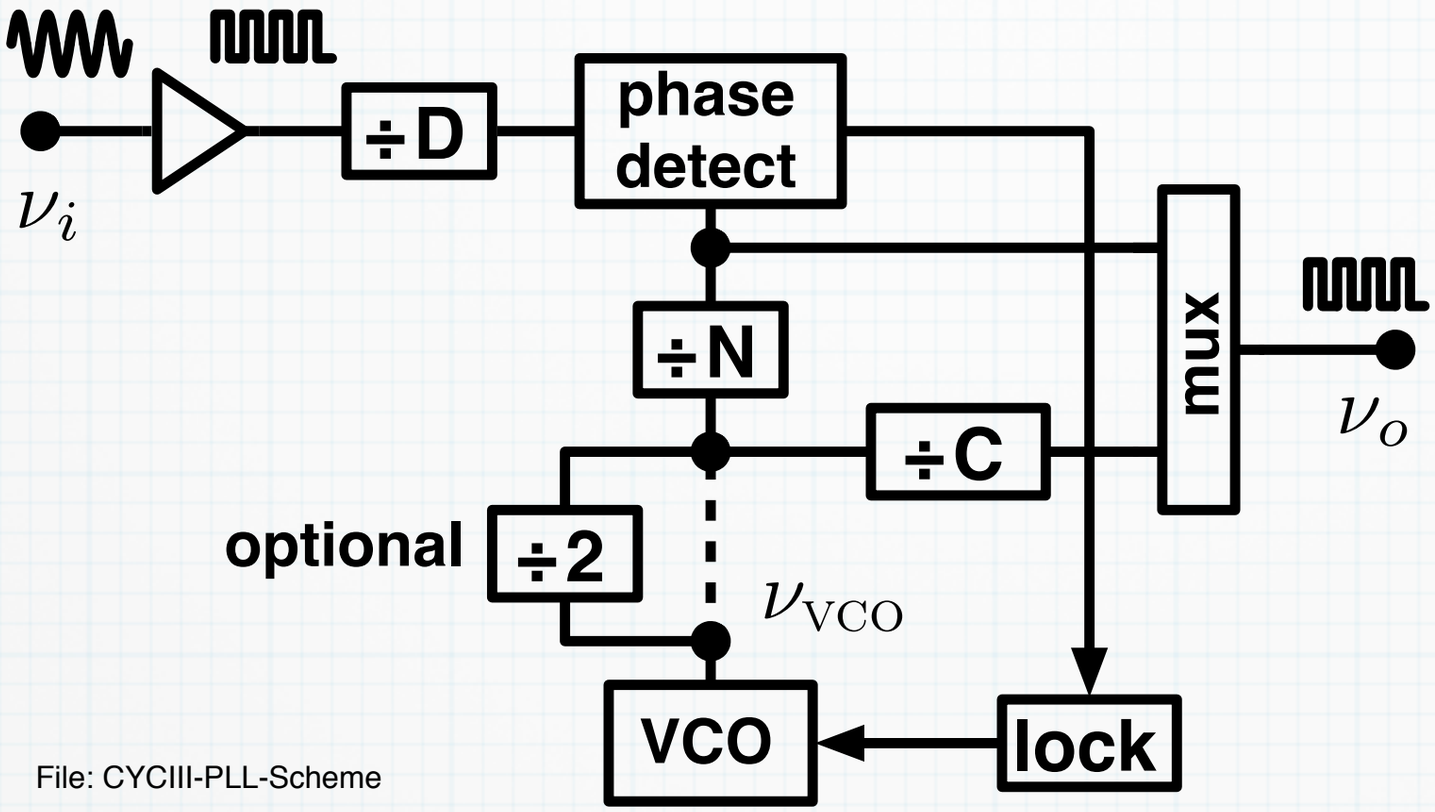


Symmetricom 5120A (30 MHz max)



- **A Λ divider (inside the FPGA) enables the measurement**
  - **The divider noise is low enough**
  - **A trick to work at low frequency**

Cyclone III Internal PLL (2/4)

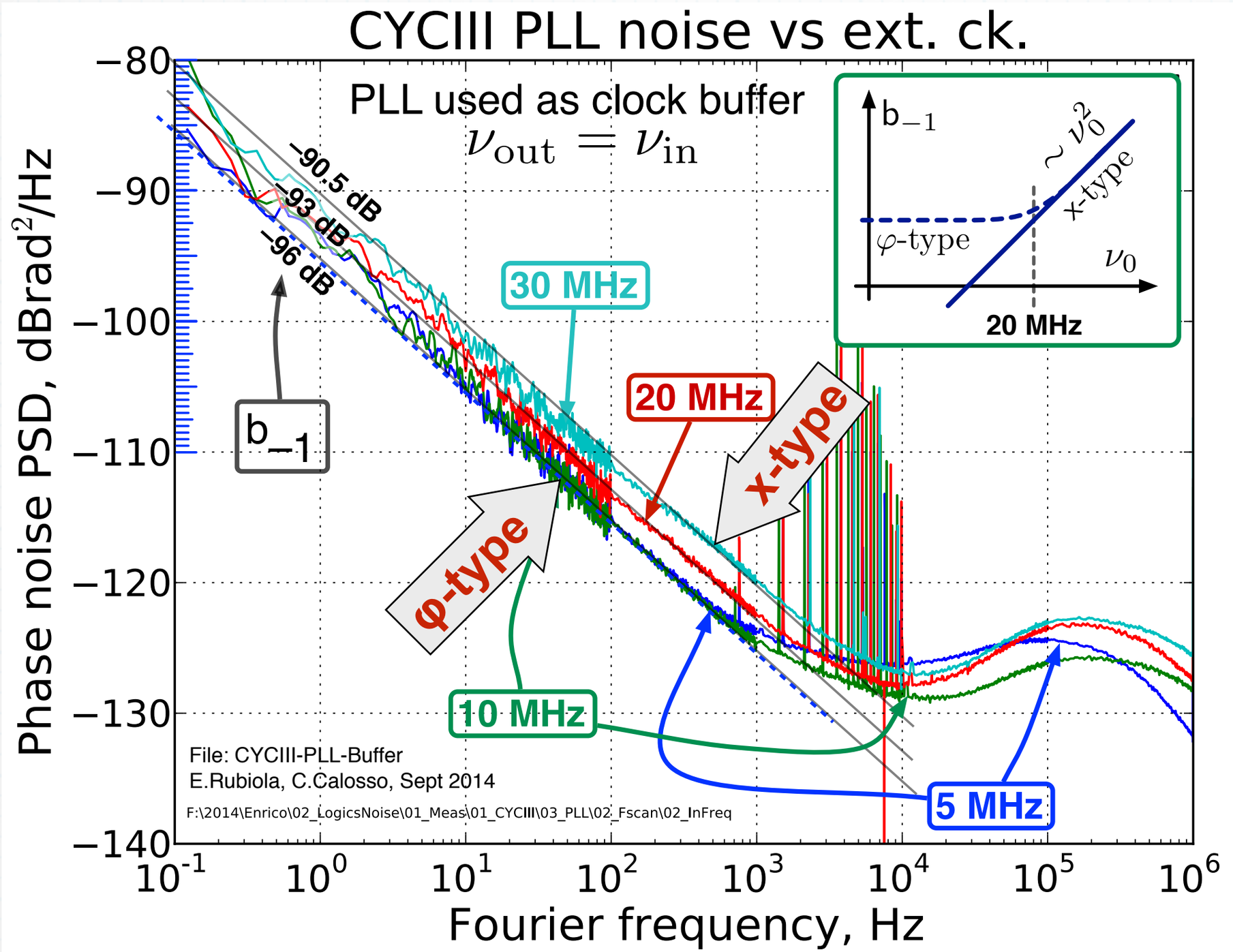


File: CYCIII-PLL-Scheme

- Low-Q LC oscillator (Q ≈ 10), 0.6–1.3 GHz
- Optional ÷2 always present
- We set D = 1 (for lowest noise)
- QUARTUS decides C and N

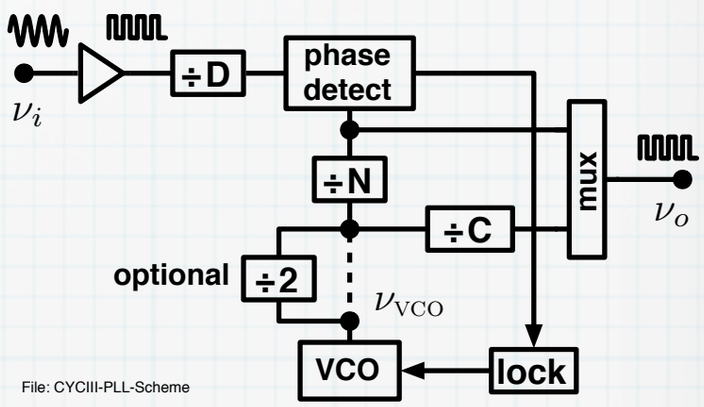
Cyclone III Internal PLL (3/4)

PLL used as a buffer



Crossover between phi-type and x-type at 20 MHz

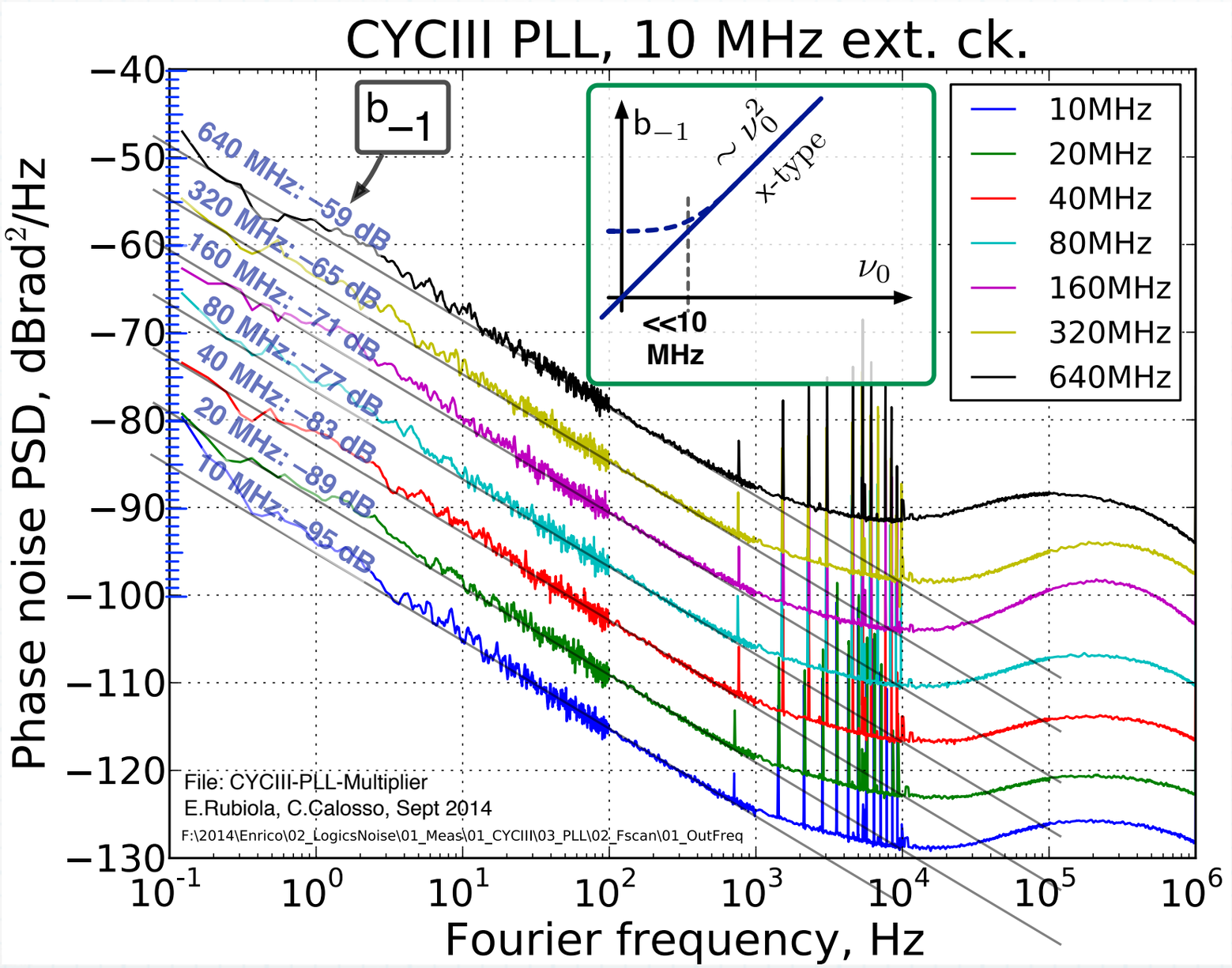
- **φ-type**
  16 µrad/√Hz @ 1 Hz
- **x-type**
  220 fs/√Hz @ 1 Hz



x-type –> analog noise in the phase detector

Cyclone III Internal PLL (4/4)

PLL used as a frequency multiplier

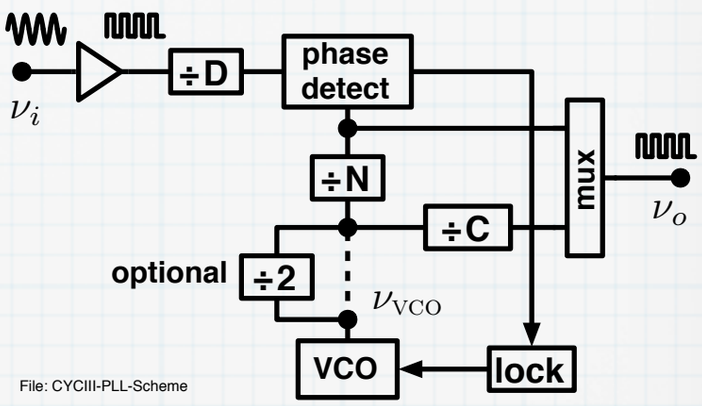


10 MHz input

N x 10 MHz out

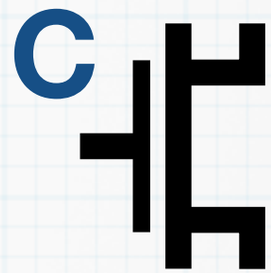
Stability
1.5×10^{-12} @ 1 s
(f_H = 500 Hz)

–115 dB + 20 $\log_{10}(v_0)$ in MHz



- **1/*f* phase noise is dominant**
- **Scales as N^2 –> analog noise in the phase detector**

Thermal Effects (1/3)



Principle

- FPGA dissipation change ΔP by acting on frequency
- Energy $E = CV^2$ dissipated by the gate capacitor in a cycle

Conditions

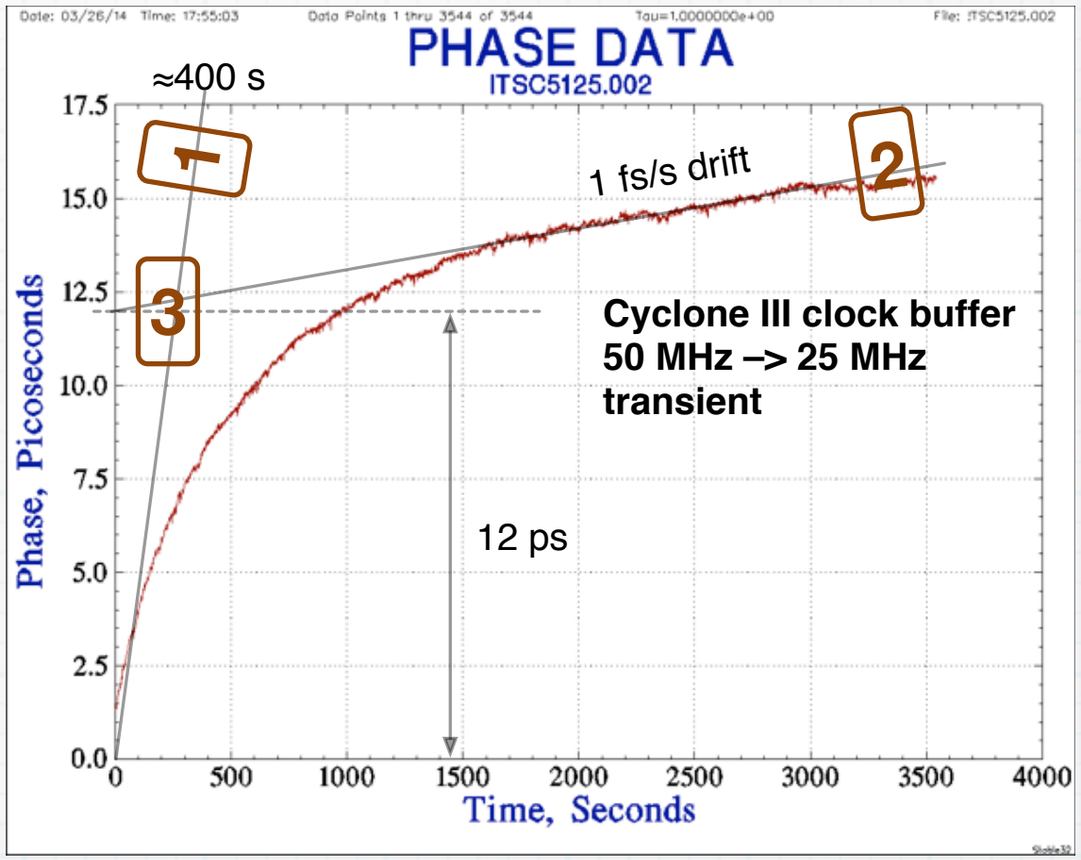
- Cyclone III used as a clock buffer
- Environment temperature fluctuations are filtered out with a small blanket (necessary)
- Two separate measurements (phase meter and counter) –> trusted result

Outcome

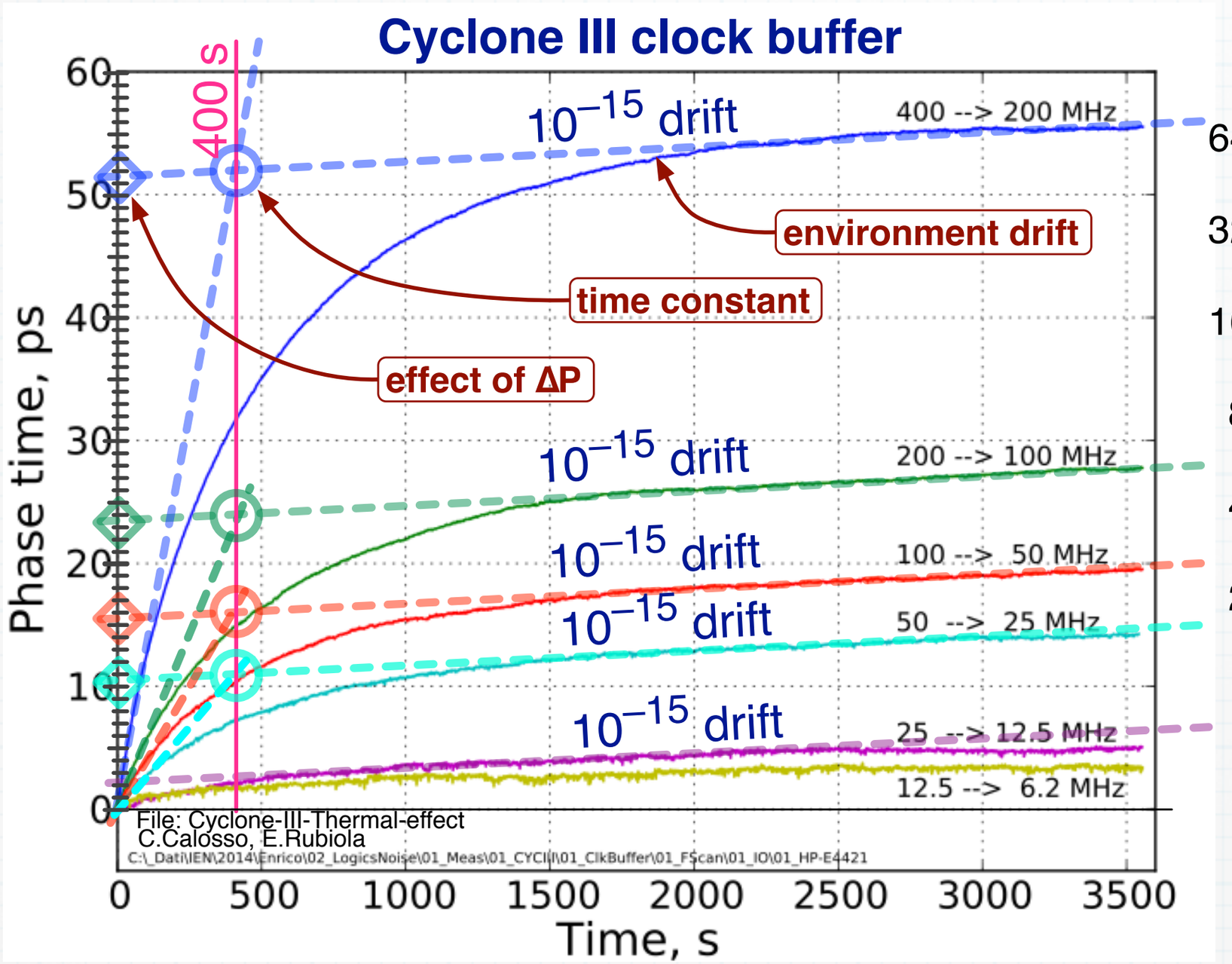
(1) Thermal transient, due to the change of the FPGA dissipation

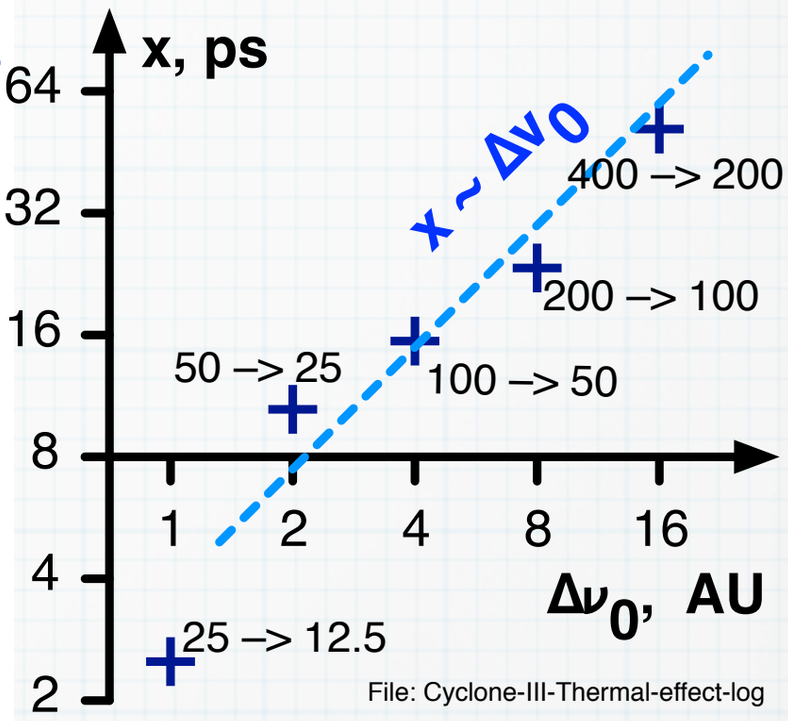
(2) Slow thermal drift, due to the environment

(3) Overall effect of ΔP



Thermal Effects (2/3)



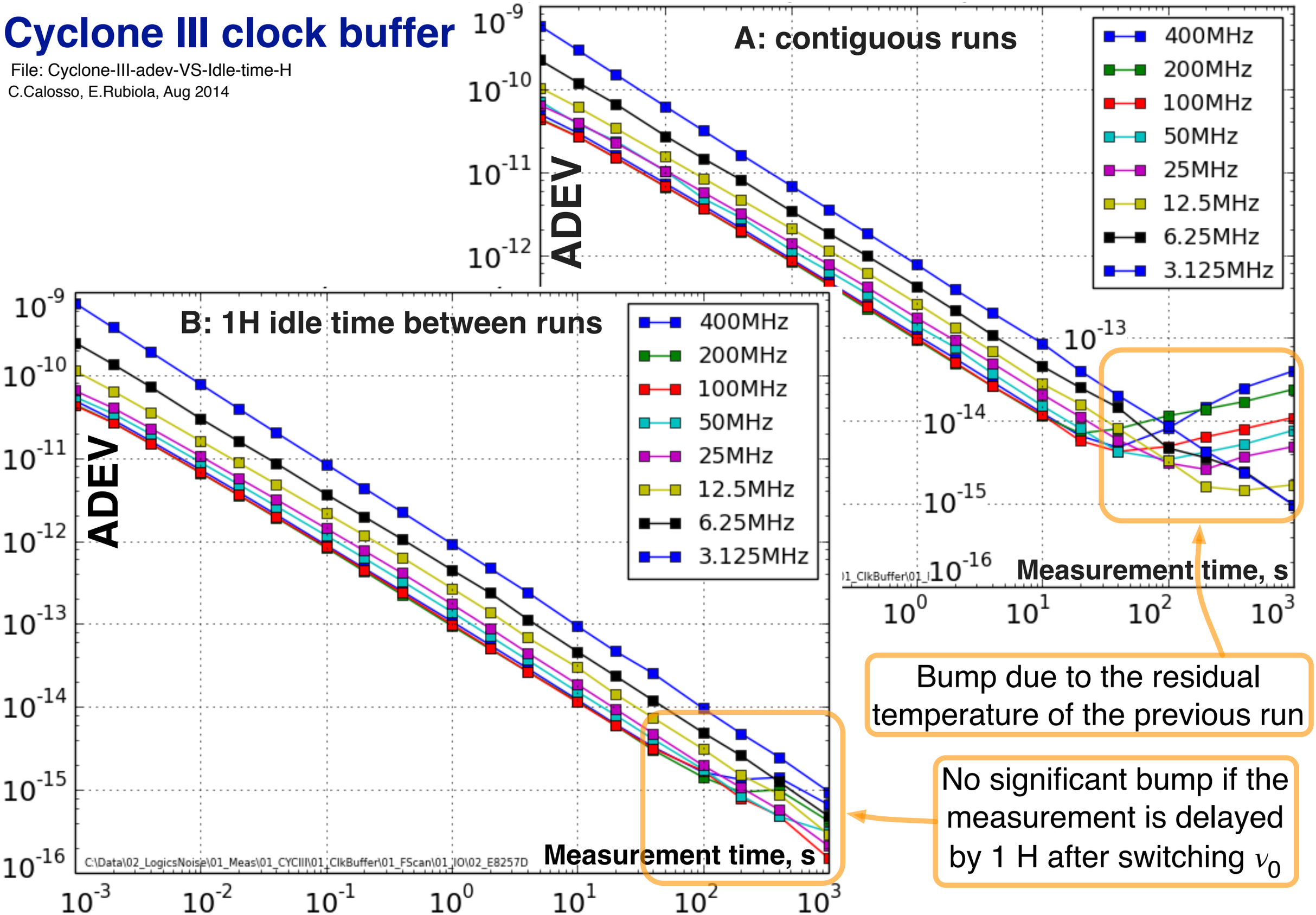


Warning: In real applications, other parts of the same FPGA impact on the temperature, thus on phase – drift is possible

Thermal Effects (3/3)

Cyclone III clock buffer

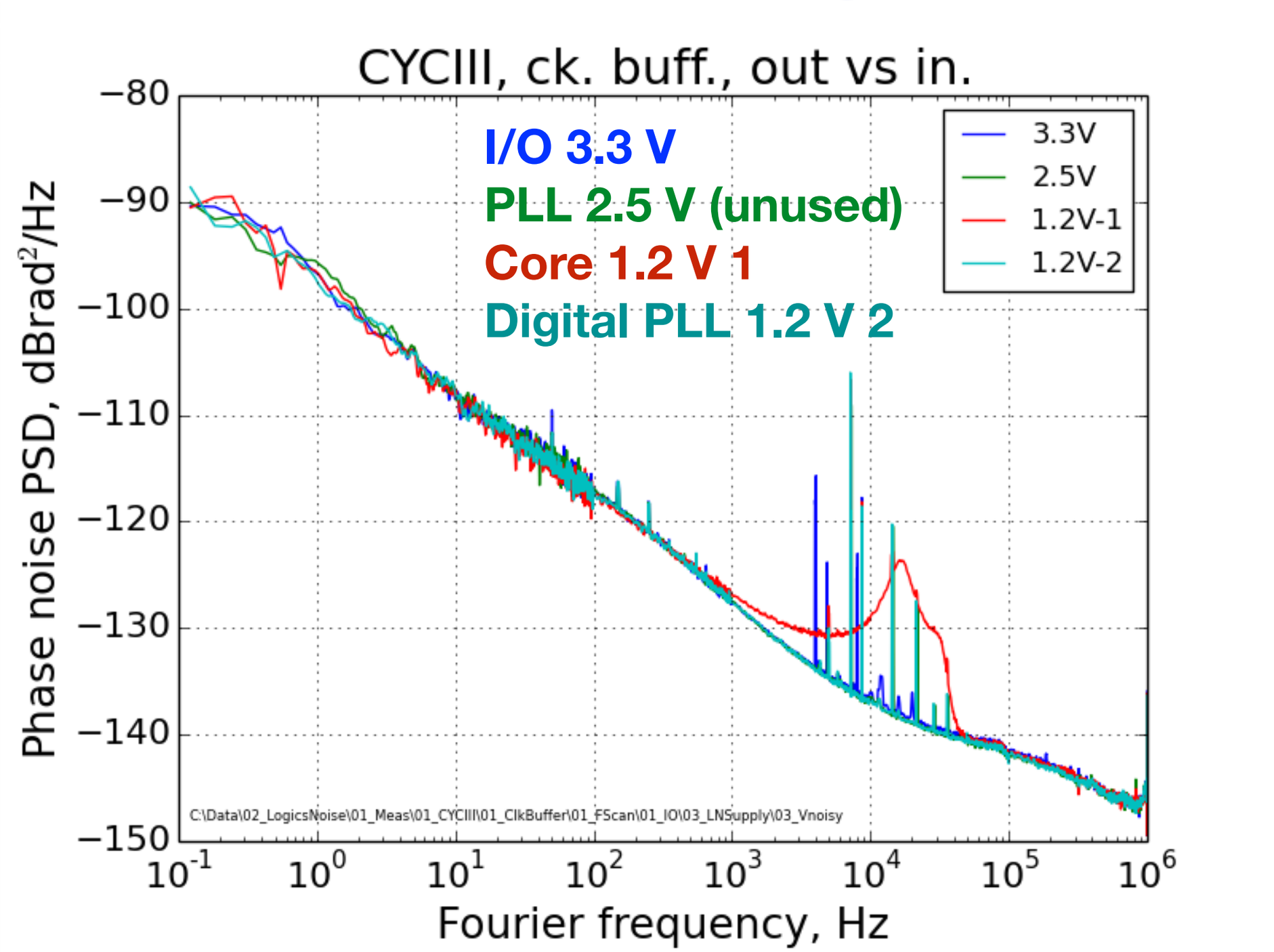
File: Cyclone-III-adev-VS-Idle-time-H
C.Calosso, E.Rubiola, Aug 2014



Bump due to the residual temperature of the previous run

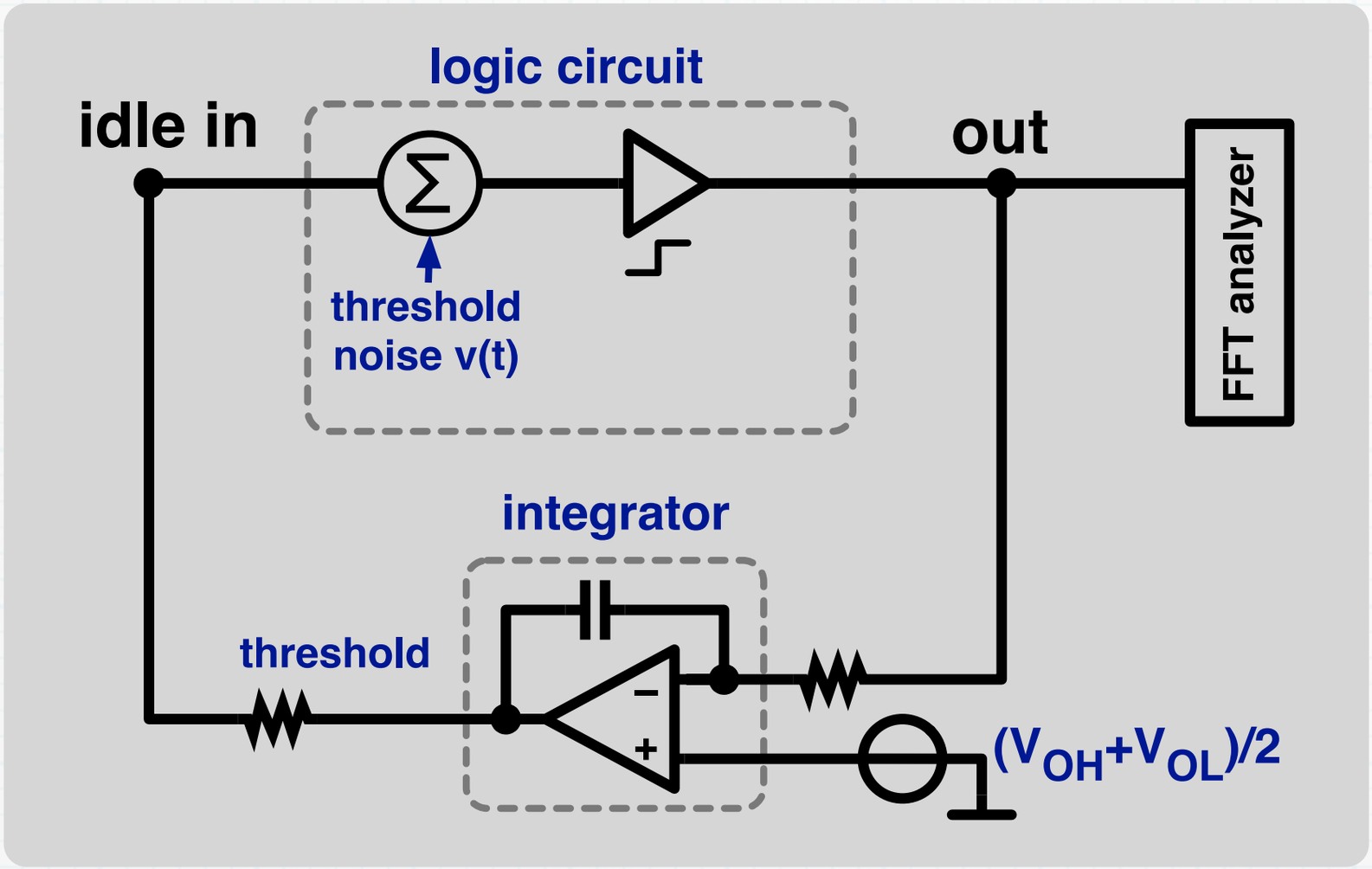
No significant bump if the measurement is delayed by 1 H after switching ν_0

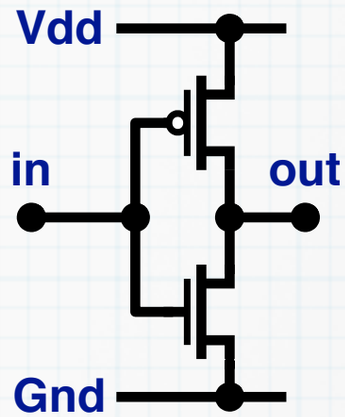
Cyclone III, Voltage Supply



- **All but one low-noise voltage supplies**
- **The noise is critical only in the core supply**

Threshold-Noise Measurement



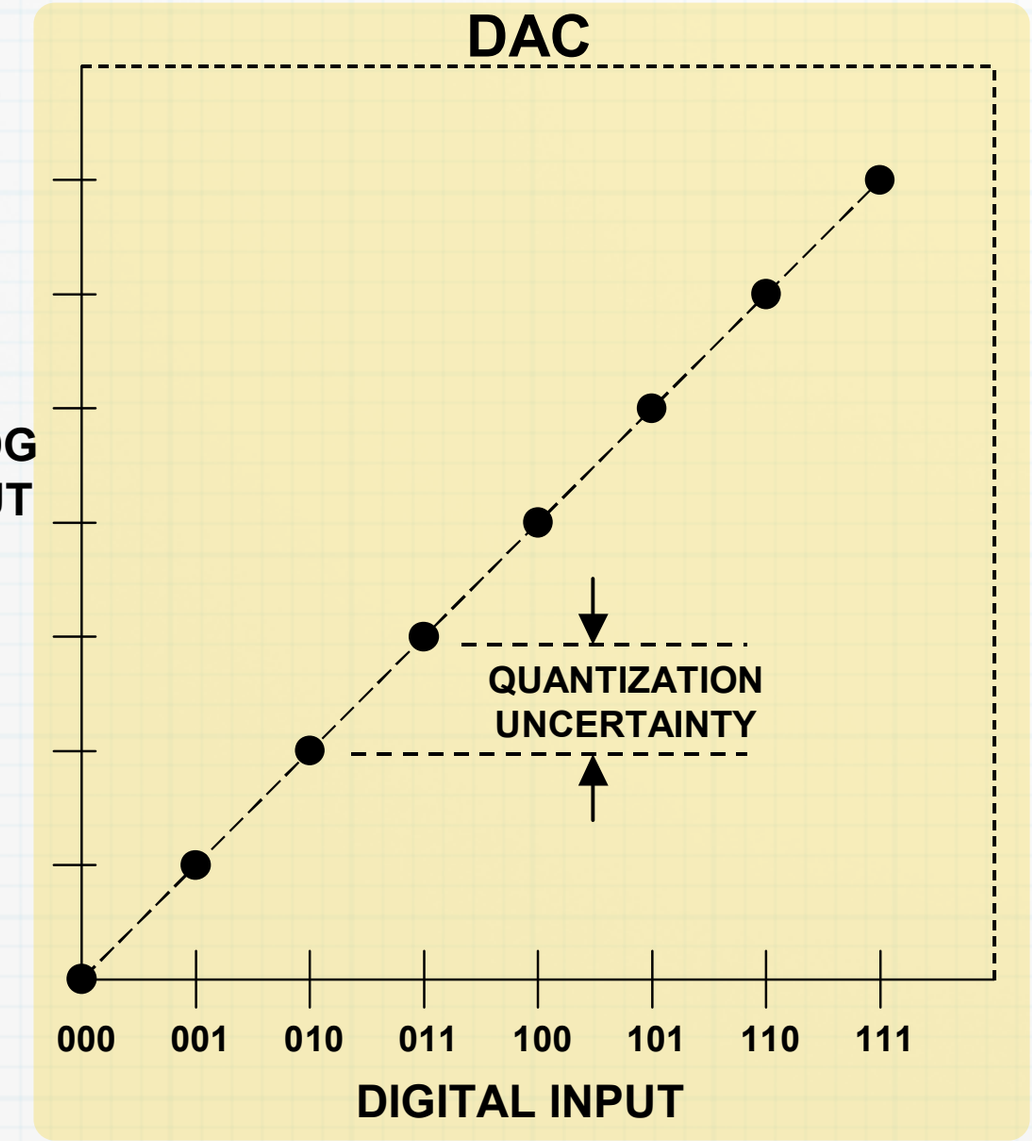


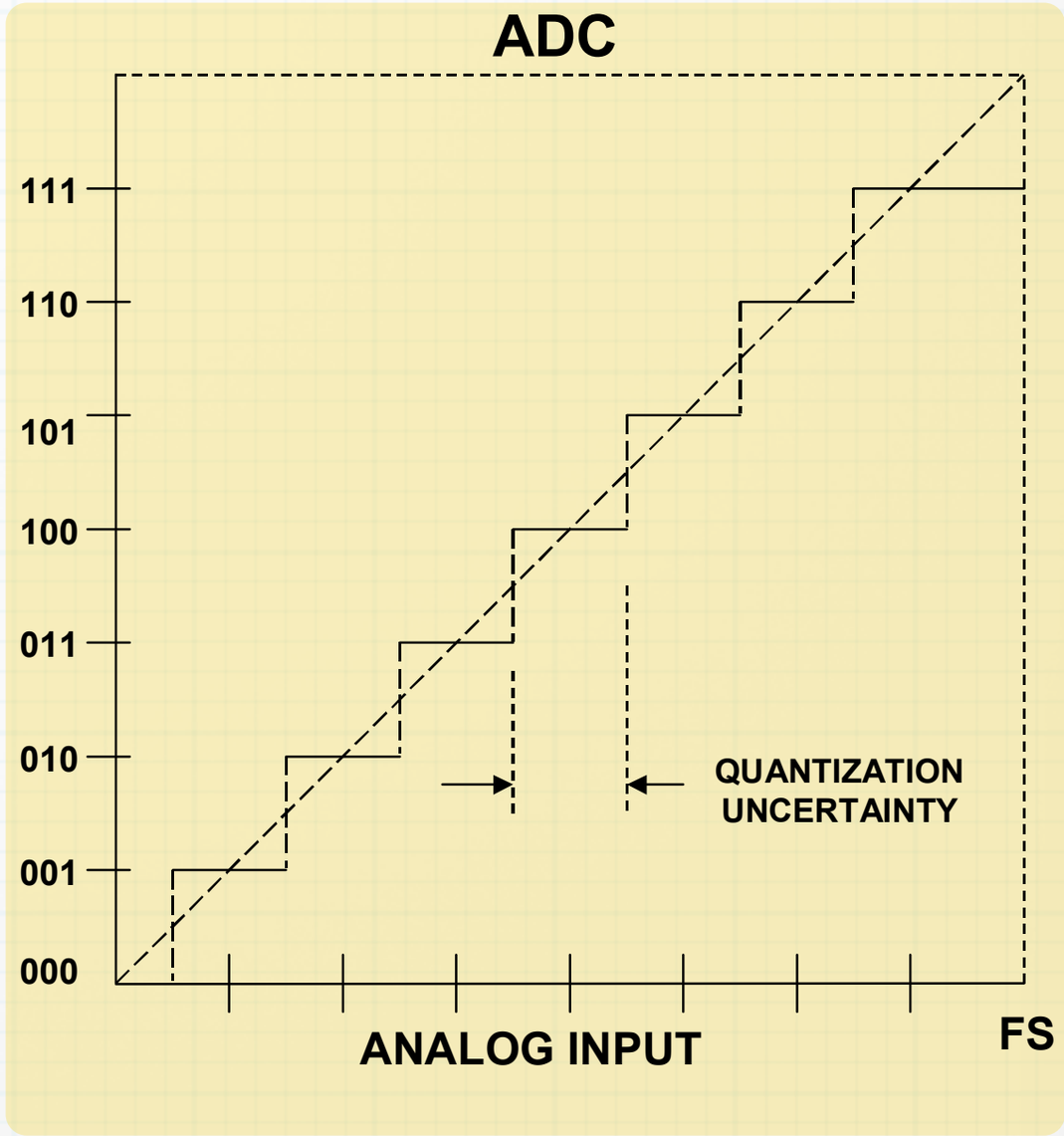
- Keep the logic at the threshold, where it shows analog gain
- Measure the voltage (current) fluctuation needed to stabilise at the threshold
- Works only on simple (old) circuits
- Threshold-mismatched cascade –> gain not accessible
- FPGAs complexity make the analog gain inaccessible

3 – ADCs

Basics

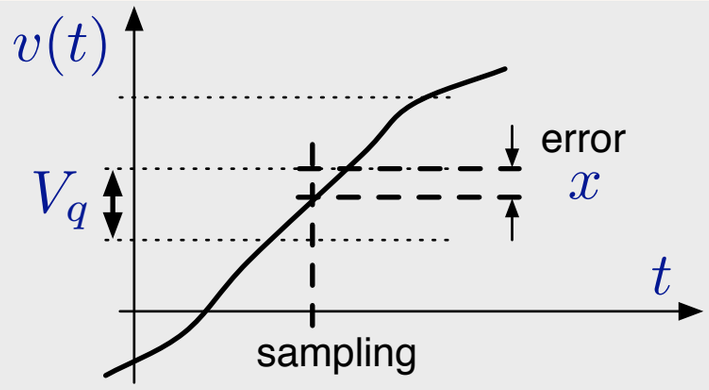
Transfer Function & Quantization



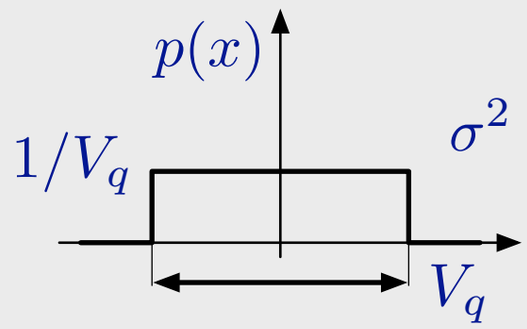


Kester W (ed), *Analog-Digital Conversion*, Fig.2.15, p.2.14,
Analog Devices 2004, ISBN 0-916550-27-3

Spectrum of the Quantization Noise



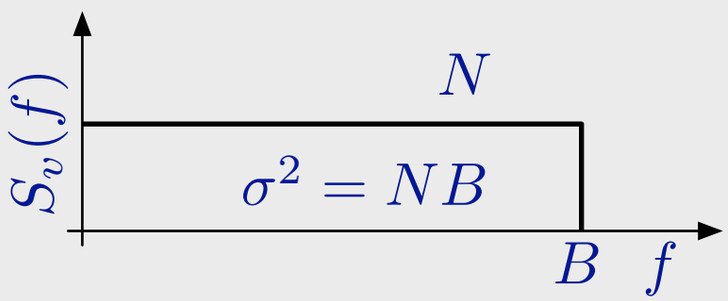
The analog-to-digital converter introduces a quantization error x, $-V_q/2 \le x \le +V_q/2$



$$\sigma^2 = \frac{V_q^2}{12}$$

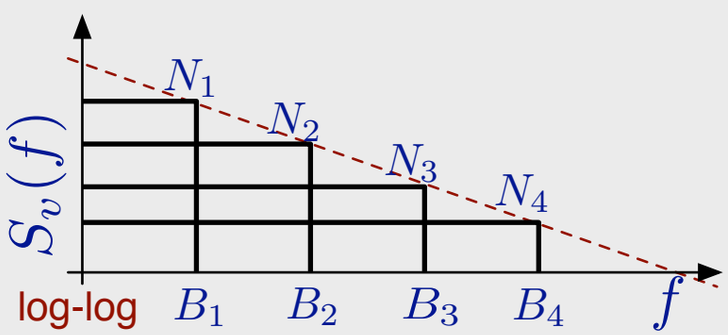
Ergodicity suggests that the quantization noise can be calculated statistically

$$\sigma^2 = \frac{V_q^2}{12}$$



The Parseval theorem states that energy and power can be evaluated by integrating the spectrum

$$NB = \frac{V_q^2}{12}$$



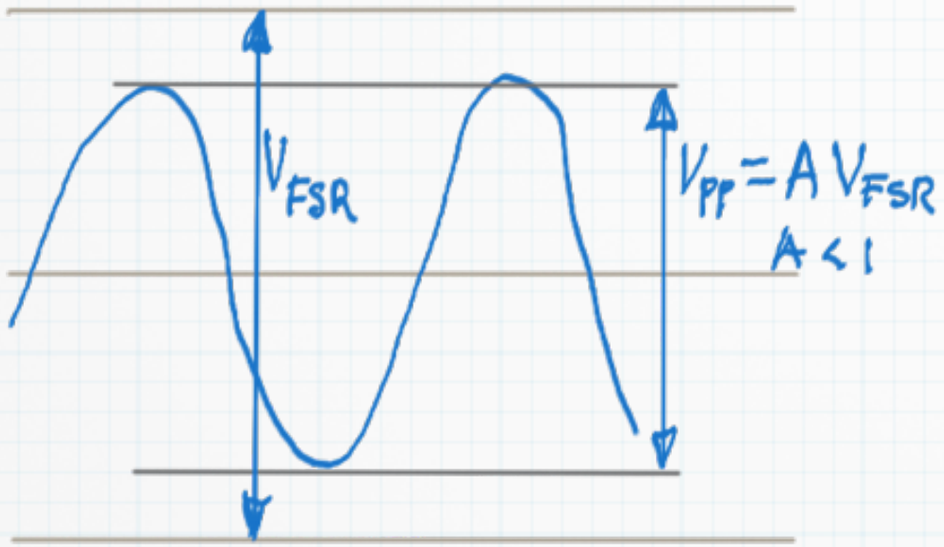
Changing B in geometric progression (decades) yields naturally 1/B (flicker) noise

$$N = \frac{V_q^2}{12B}$$

1/12 is –10.8 dB

Quantization & Sinusoidal Signals

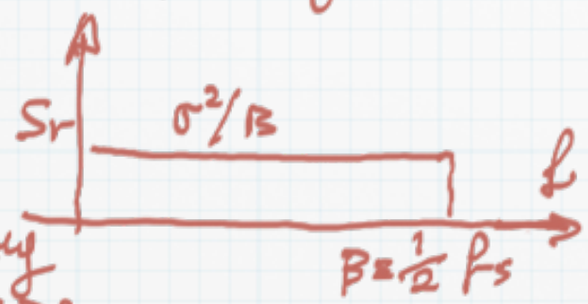
Sampling frequency f_s



Warning: We assume that the noise power is equally distributed in 0...B.

This is not true in our case because sampling and carrier are highly coherent. See Widrow-Kollar Appendix G for details.

Anyway, we temporarily accept the uniform distribution, hoping that the reality is not too far.



Signal power

$$P_0 = \frac{V_{PP}^2}{8} = \frac{A^2 V_{FSR}^2}{8}$$

Noise power

$$\sigma^2 = \frac{V_{LSB}^2}{12}$$

SNR = (3/2) 2^{2m}

6.02 m + 1.76 dB

Parseval theorem

$$S_V = \frac{\sigma^2}{B} \text{ o-- } 1/2\, f_s \Rightarrow S_V = \frac{V_{LSB}^2}{6 f_s}$$

Phase noise $S_\varphi = b_0$ (white)

$$b_0 = \frac{S_V}{P_0} \qquad b_0 = \frac{V_{LSB}^2}{V_{FSR}^2} \cdot \frac{4}{3A^2 f_s}$$

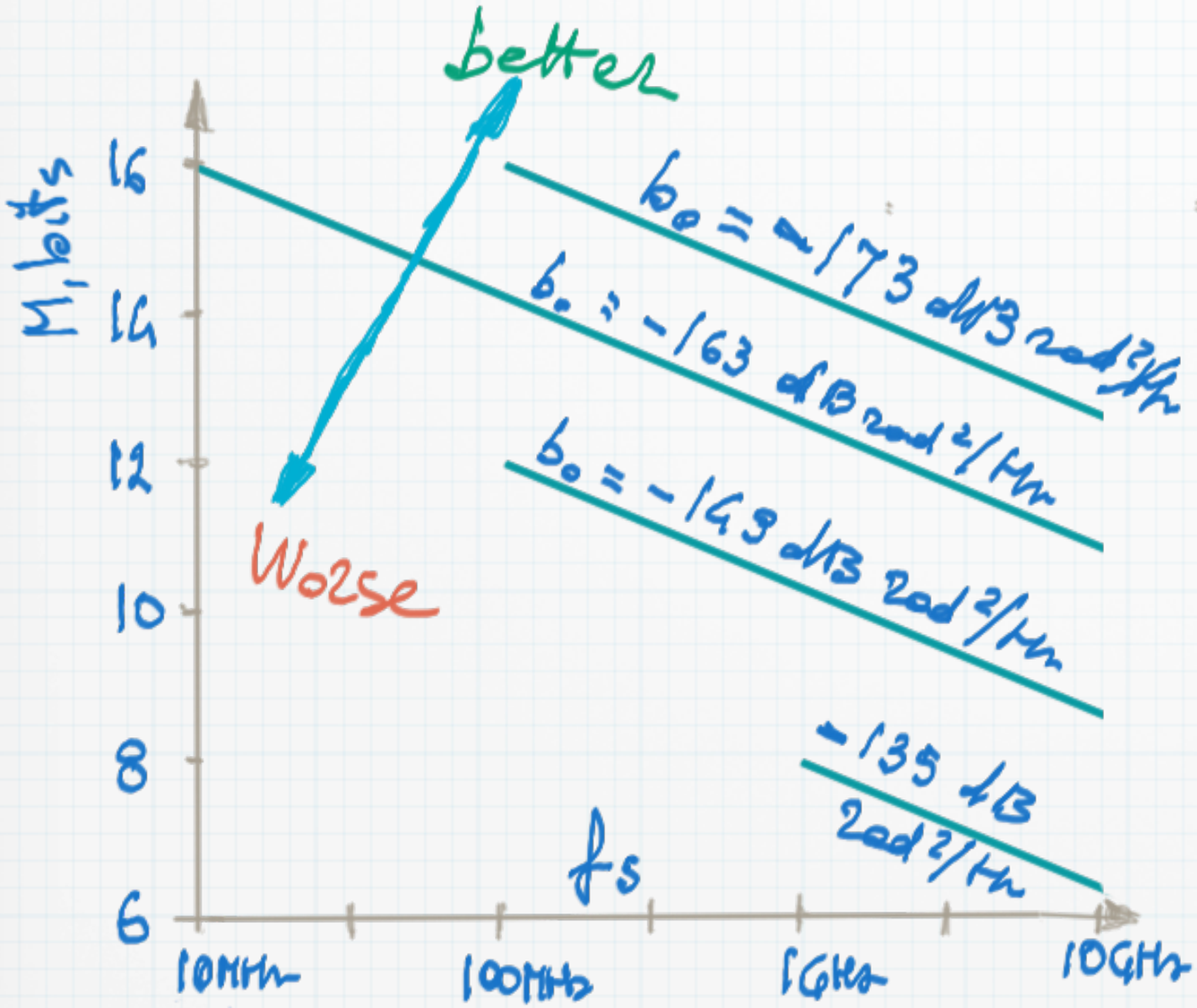
$$b_0 = \frac{1}{(2^M)^2} \frac{4}{3A^2 f_s}$$

6.02 m + 1.25 –10 $\log_{10} f_s$ dB

Approximation (fairly large V_P)

$A^2 = 2/3$ (−1.8 dB) $\Rightarrow b_0 \approx \frac{1}{(2^M)^2} \frac{2}{f_s}$

Phase Noise



$$b_0 = \frac{1}{(2^M)^2}\,\frac{4}{3A^2 f_S}$$

$$b_0 \approx \frac{1}{(2^M)^2}\,\frac{2}{f_S}$$

Cost of 6 dB improvement

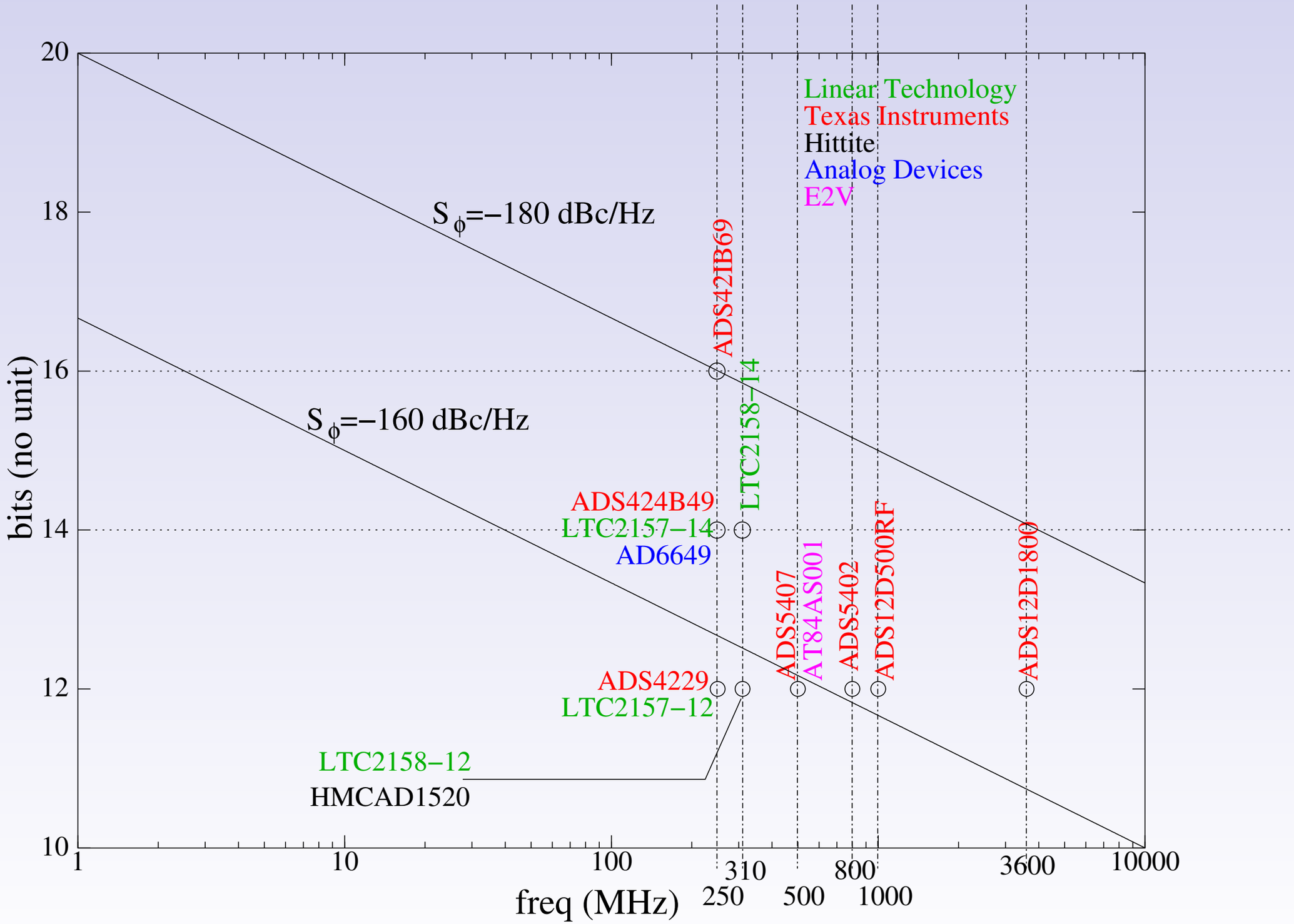
- 1 bit
- factor-of-4 f_S

Obvious conclusion: practical ADCs feature lower b_0 at low f_S because of the higher no. of bits

Selection of dual-channel converters

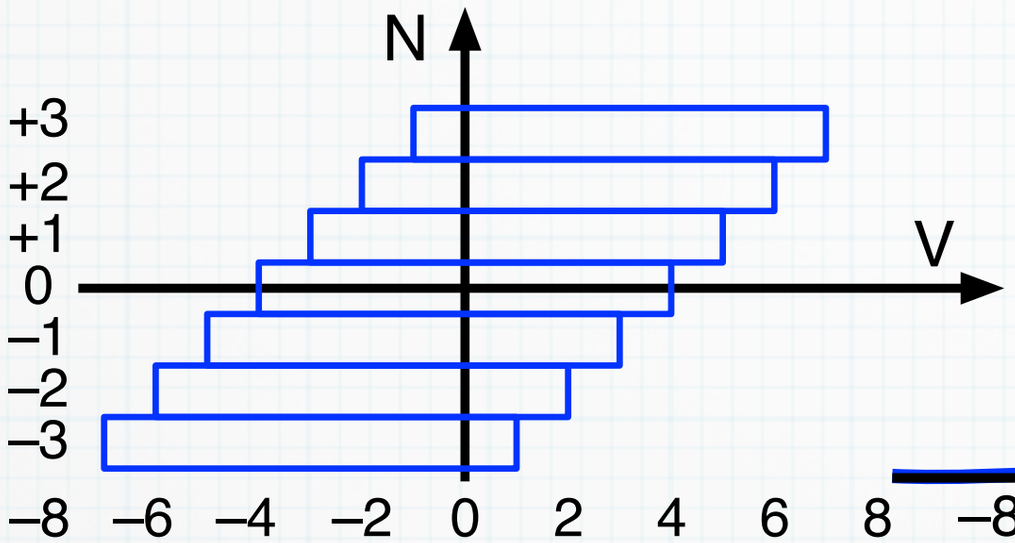
In phase measurements, a dual-channel converter is preferred because the two track-and-hold get the same clock, so the with minimum differential jitter

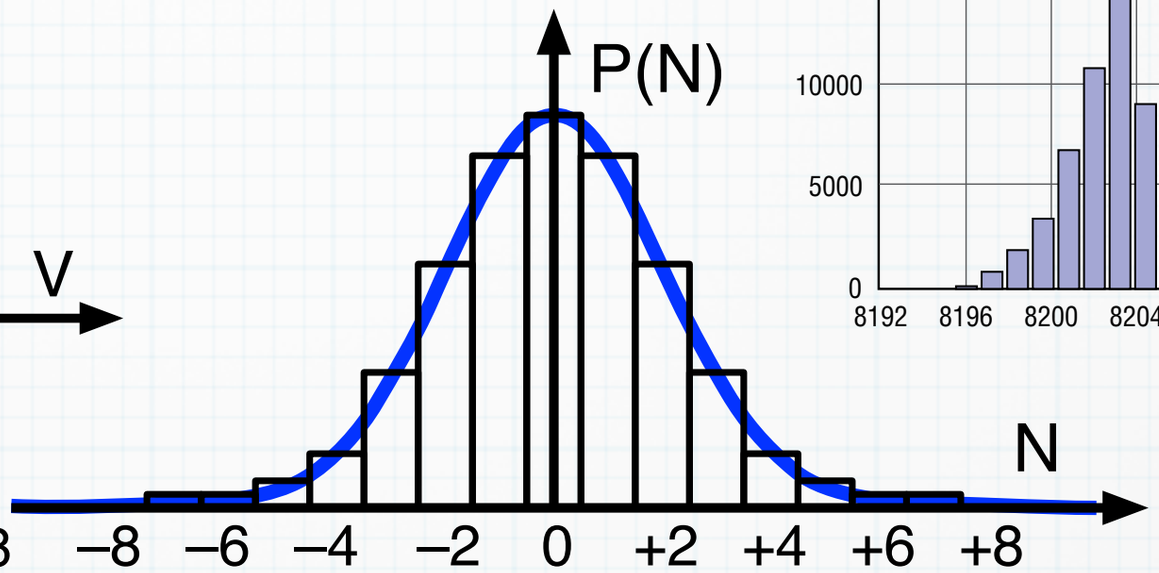
ADC

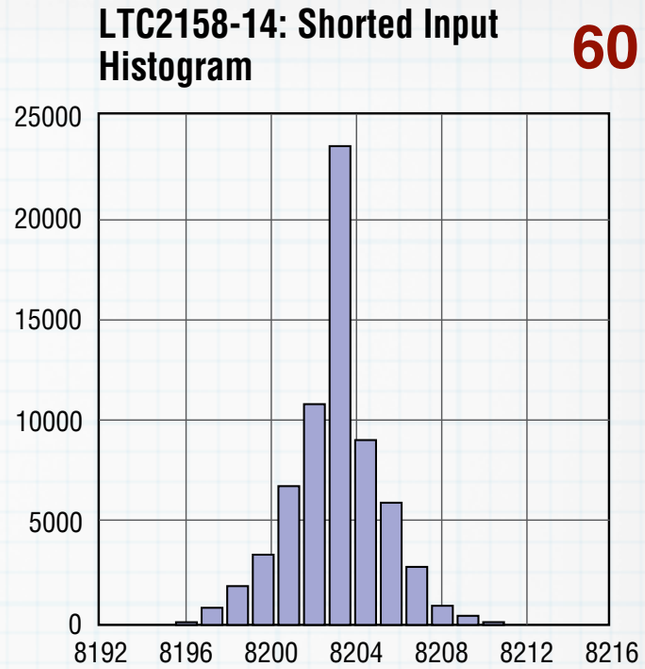


Transition Noise

High-Speed Converters







- Analog noise is higher than quantization noise
- Given a voltage V –> random distribution of output N
- This correct –> $V^2 = V^2_{analog} + V^2_{quant}$
  (don't spoil the resolution with insufficient no of bits)

Information (bits)

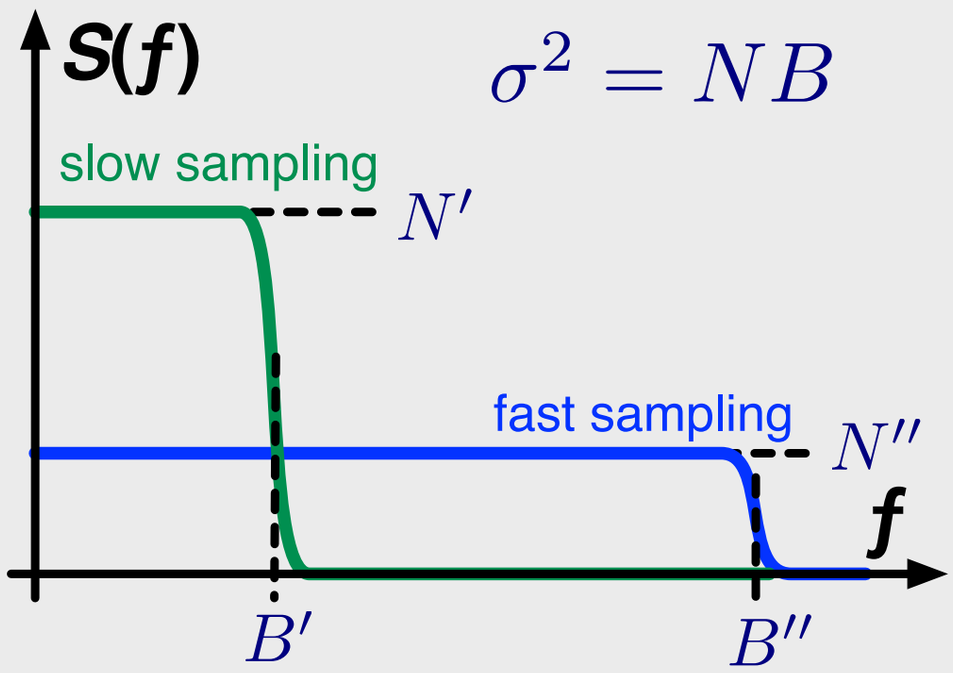
$$I = \sum_i -p_i \log_2(p_i)$$

Equivalent No of Bits

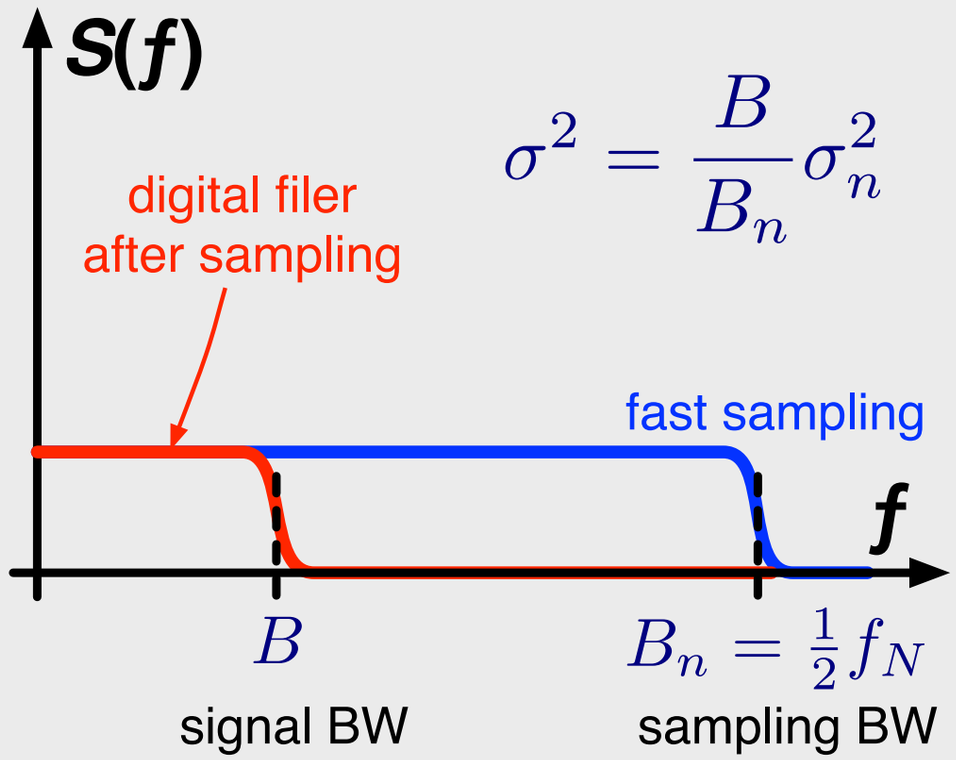
$$\mathrm{ENoB} = \log_2\left[1 + \frac{V_{\mathrm{FSR}}}{\sqrt{12 f_N}\,\sigma_V}\right]$$

Digital Filter and Decimation

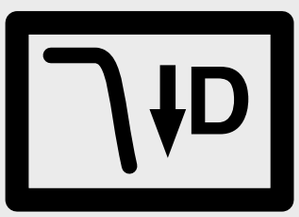
Noise, Sampling, and the Parseval theorem $\sigma^2 = \frac{V_{\mathrm{FSR}}^2}{12 \times 2^{2m}}$

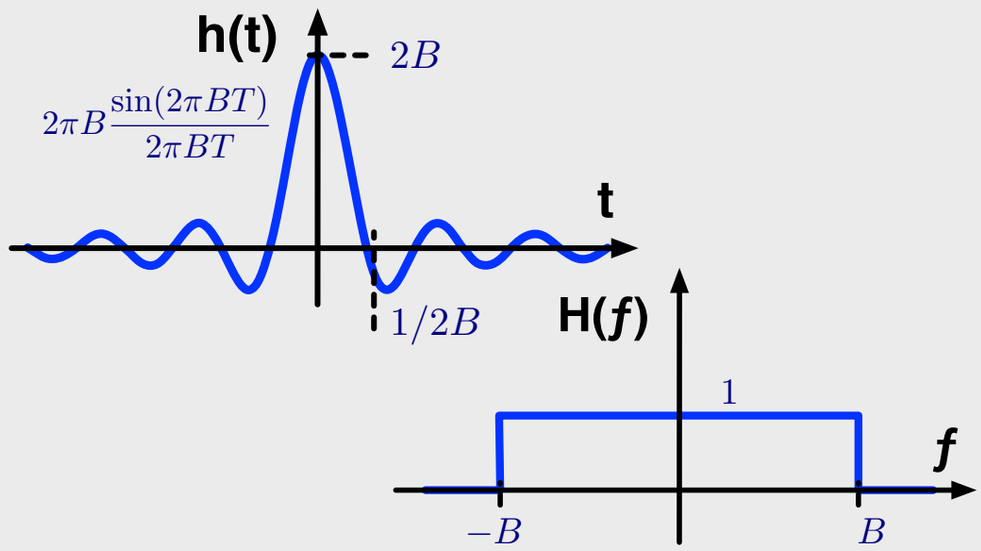


Solution:
Fast sampling, and filter

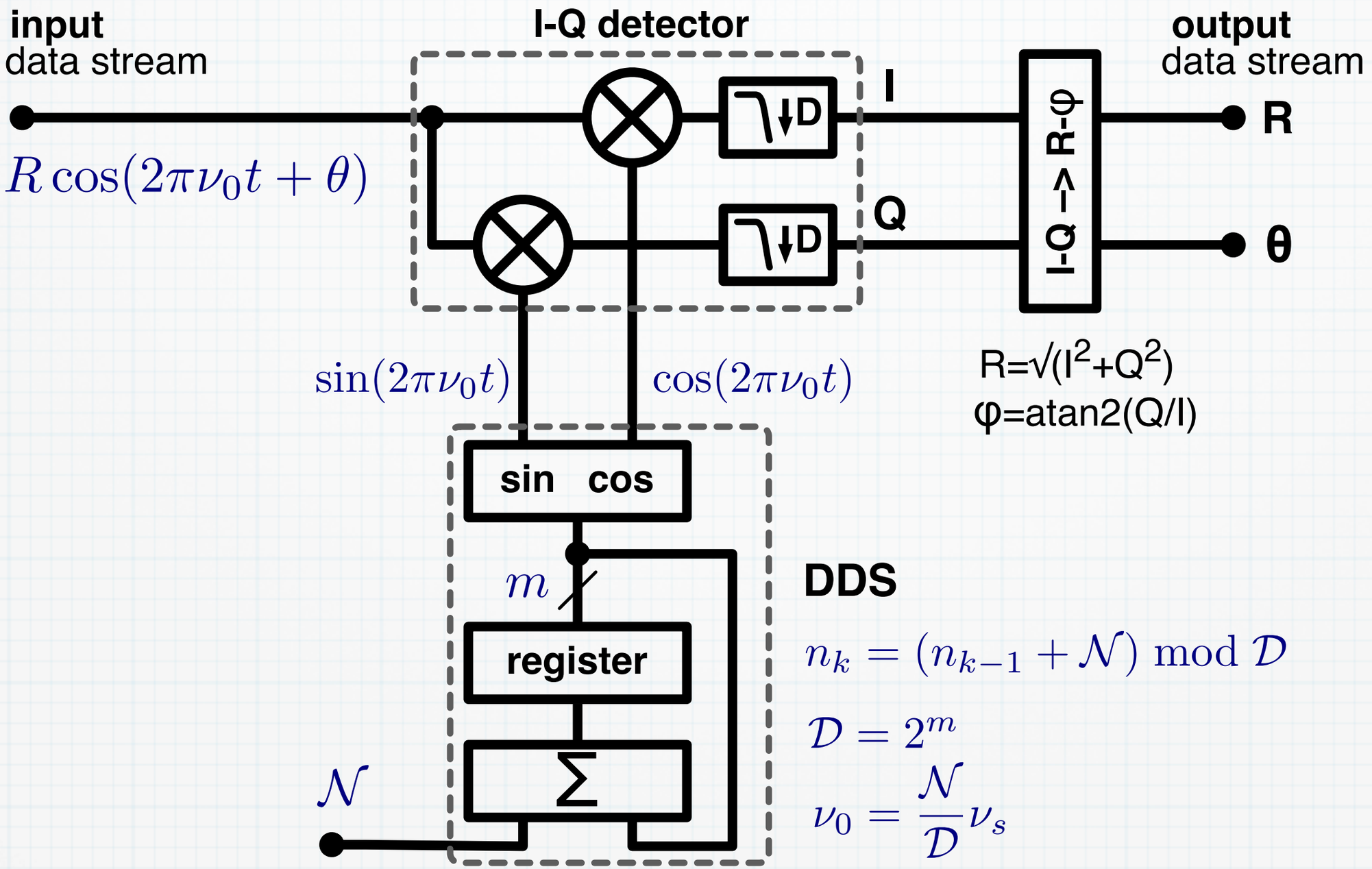


- **Convolution with low-pass h(t)**
- **127 coeff. Blackman-Harris kernel provides 70 dB stop-band attenuation**
- **Future: we will use >>127 coefficients**





Digital Down Conversion



DDS

$$n_k = (n_{k-1} + \mathcal{N}) \bmod \mathcal{D}$$

$$\mathcal{D} = 2^m$$

$$\nu_0 = \frac{\mathcal{N}}{\mathcal{D}}\nu_s$$

DDC

Examples

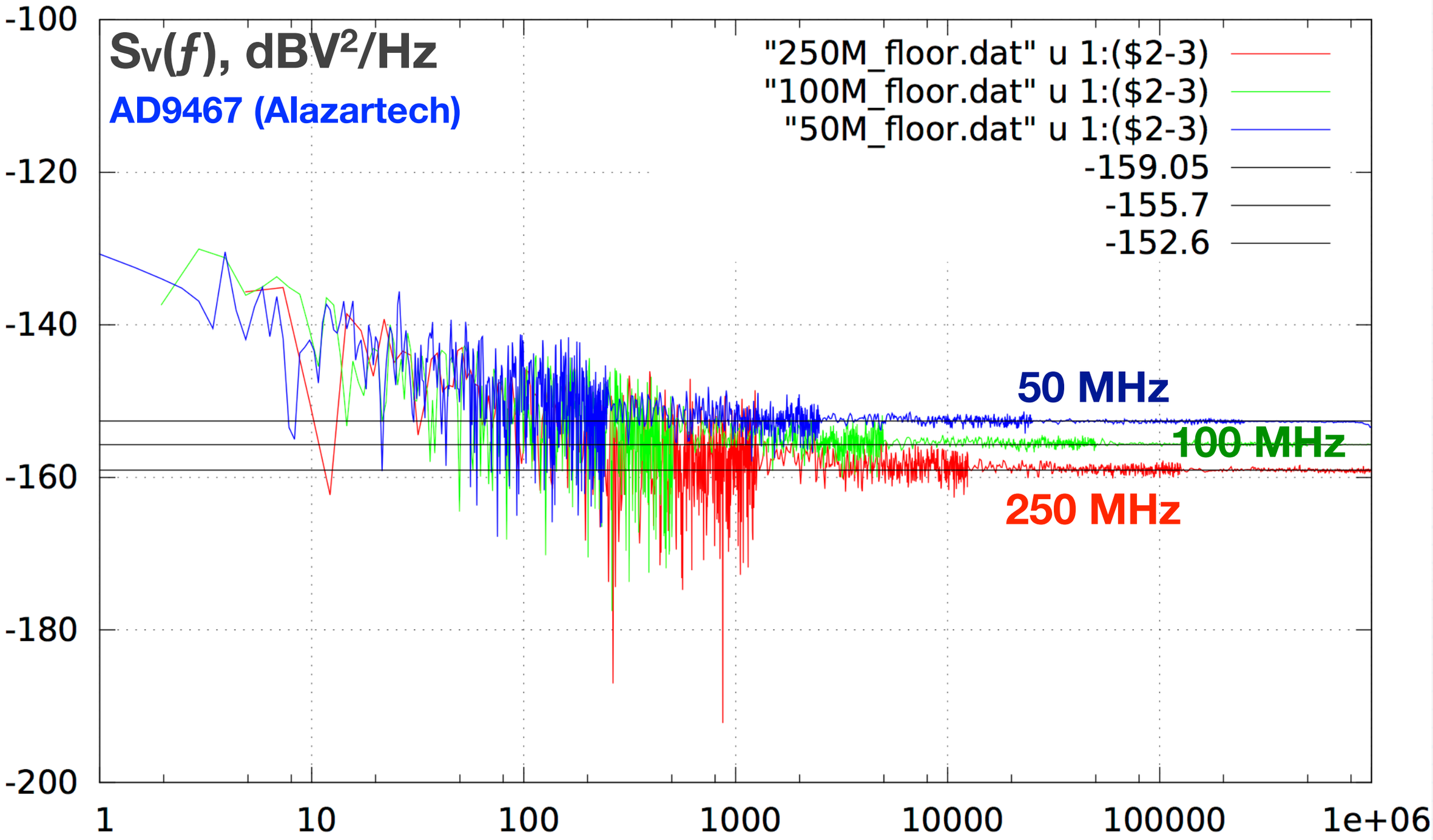
Hardware

ADC type	AD9467 / Single Alazartech	LTC2145 / Dual Red Pitaya	LTC2158 / Dual Eval board
Platform	Computer	Zynq (onboard)	Zynq (separated)
Sampling f Input BW	250 MHz 900 MHz	125 MHz 750 MHz	310 MHz 1250 MHz
Bits / ENoB	16 / 12	14 / 12	14 / 12
Exp.noise ($2V_{fsr}$)	–158 dBV^2/Hz	–155 dBV^2/Hz	–159 dBV^2/Hz
Delay / Jitter	1.2 ns / 60 fs	0? / 100 fs diff 0? / 80 fs single	1 ns / 150 fs
Power supply	1.8 V & 3.3 V 1.33 W	1.8 V 190 mW	1.8 V 725 mW

Dissipation is relevant to thermal stability

For reference, 100 fs jitter is equivalent to			
carrier f	φ rms	$S\varphi(f) = b_0$	$10 \log_{10}[L(f)]$
10 MHz	6.3 µrad	4×10^{-18} rad^2/Hz	–177 dBc/Hz
100 MHz	63 µrad	4×10^{-17} rad^2/Hz	–167 dBc/Hz

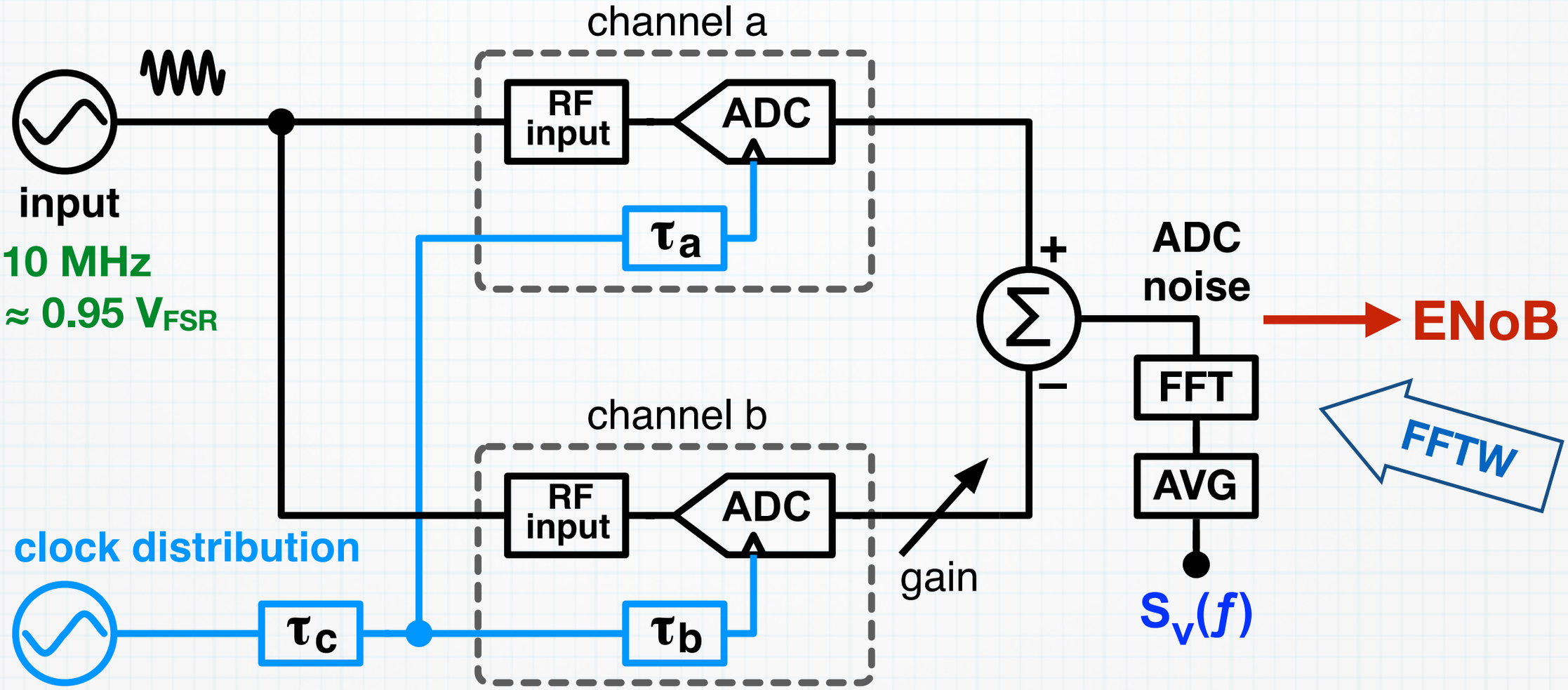
Sampling Frequency



The observed floor fits the theory

We always use the highest sampling frequency

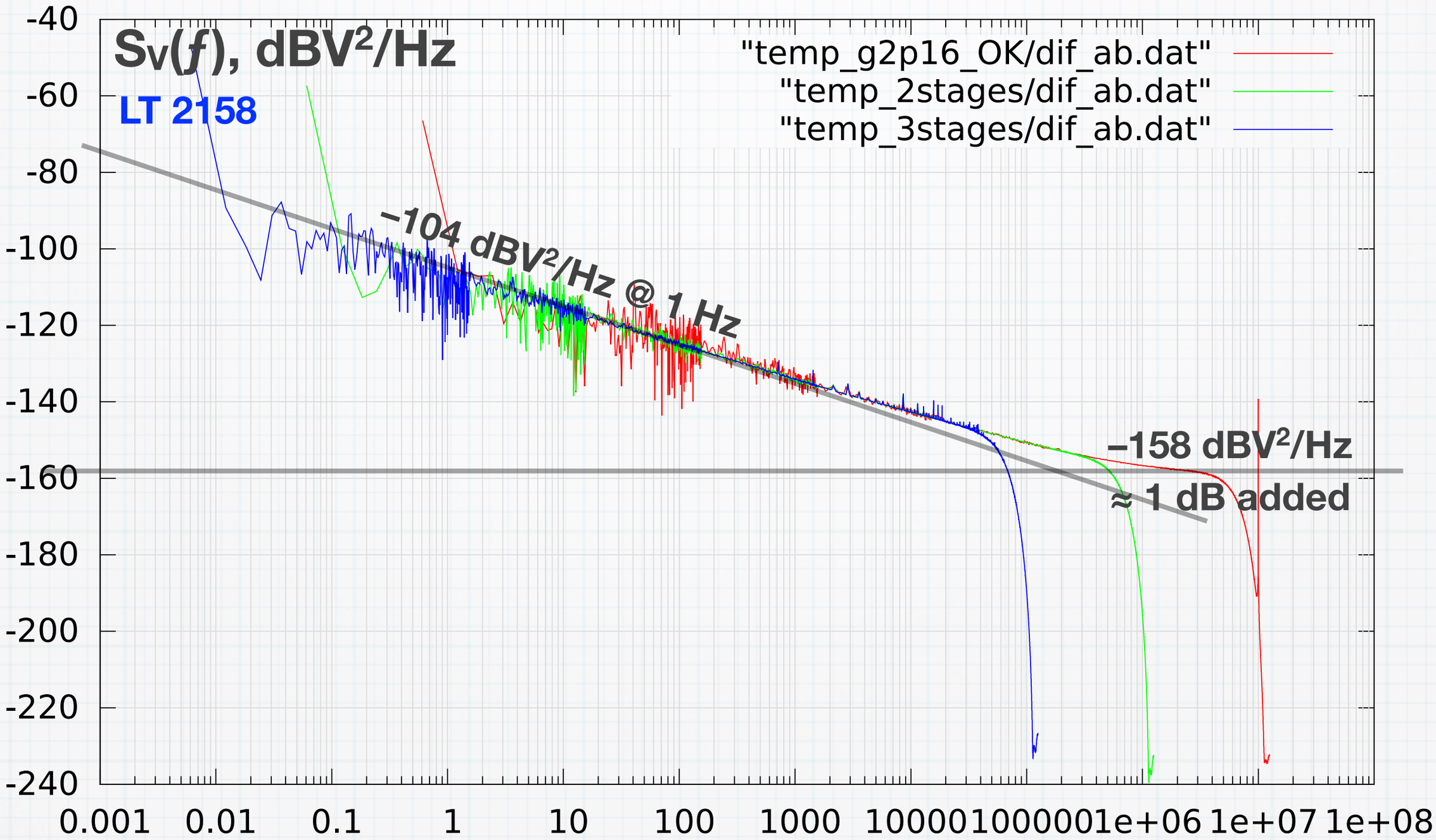
Transition Noise Measurement



The differential clock jitter introduces additional noise due to the asymmetry between AM and PM

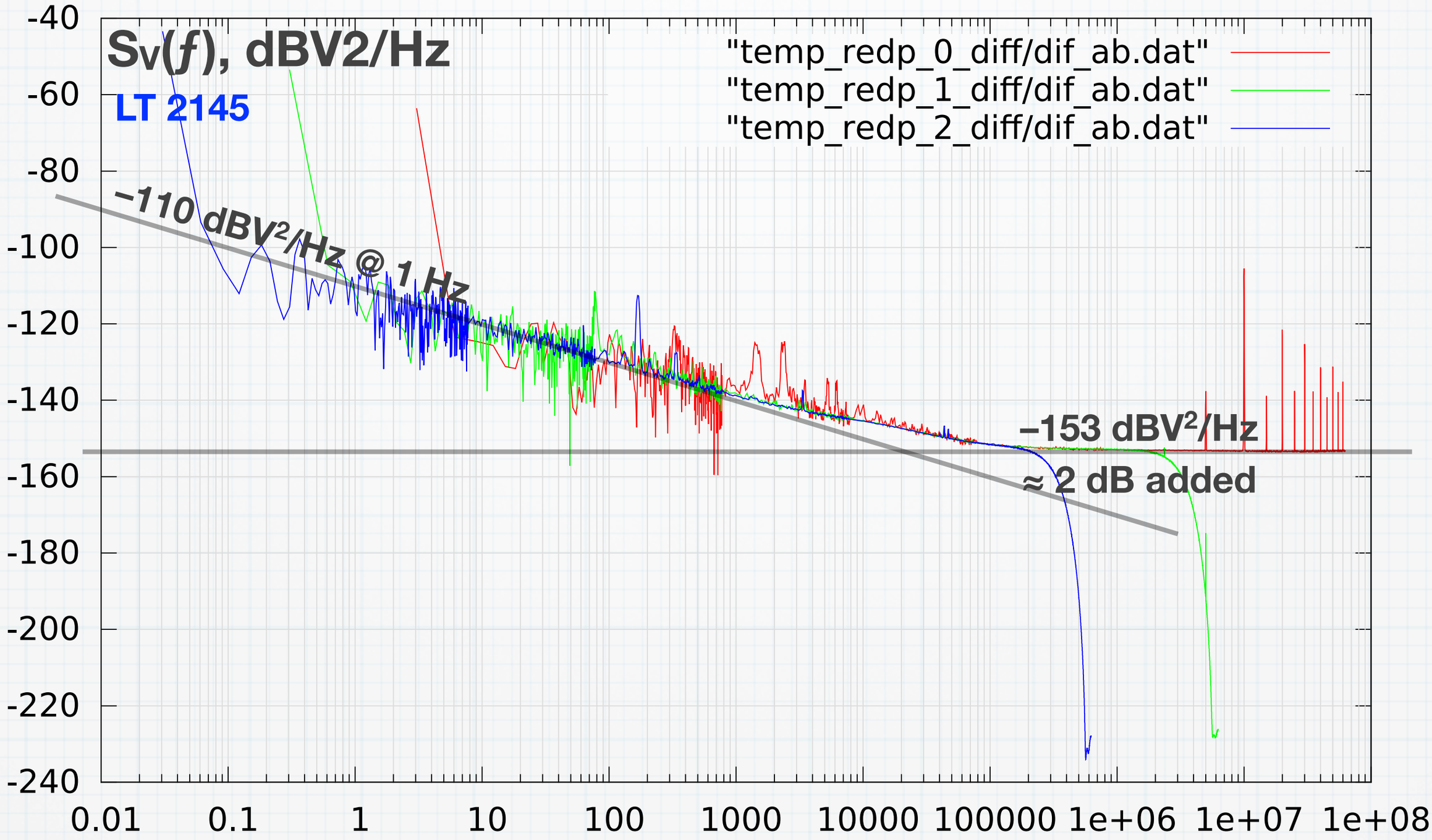
At 10 MHz input, ≈100 fs the effect of jitter does not show up

LT 2158 Noise



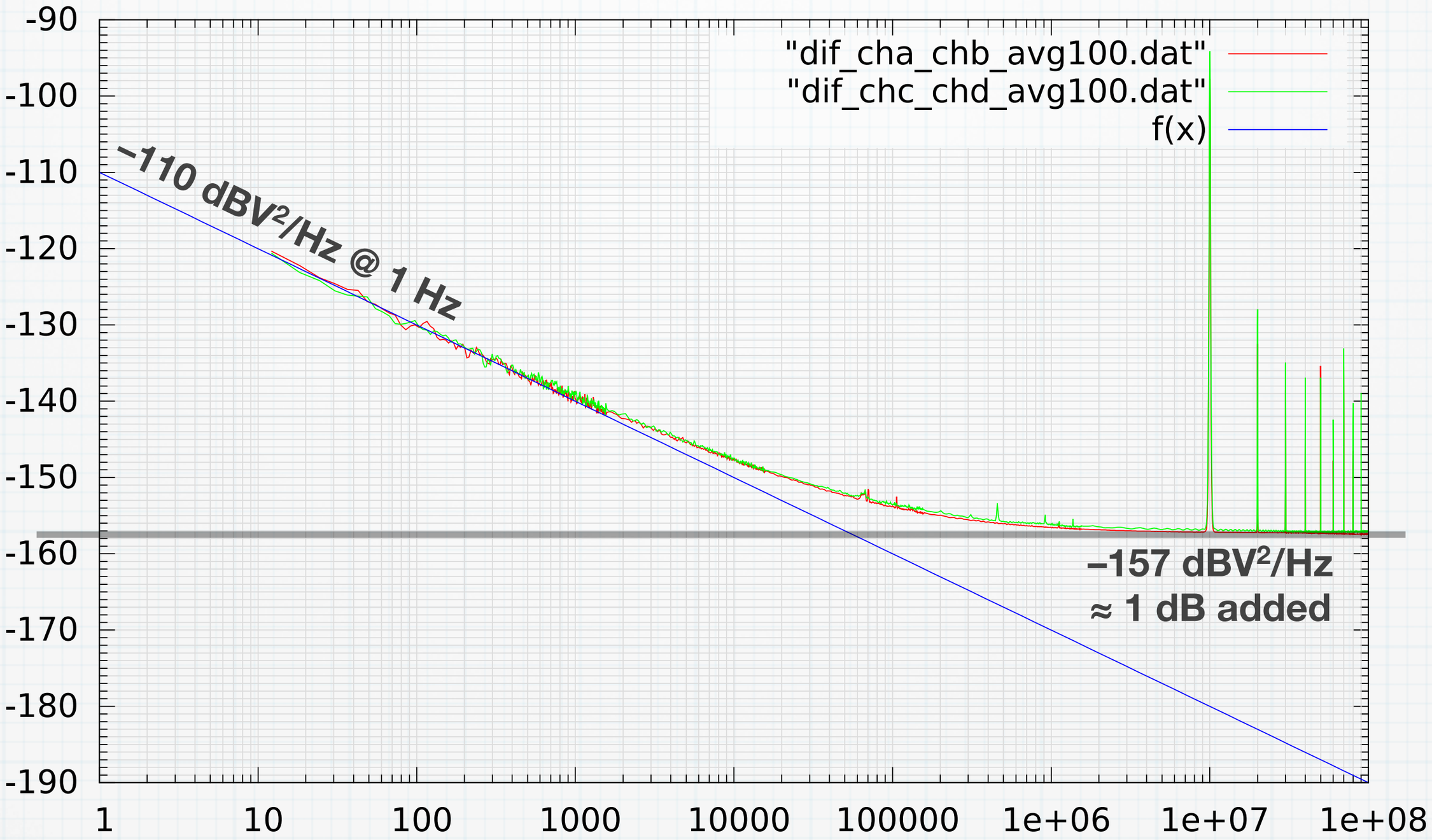
10 MHz, $V_{pp} \approx 0.95\ V_{FSR}$

LT2145 (Red Pitaya) Noise



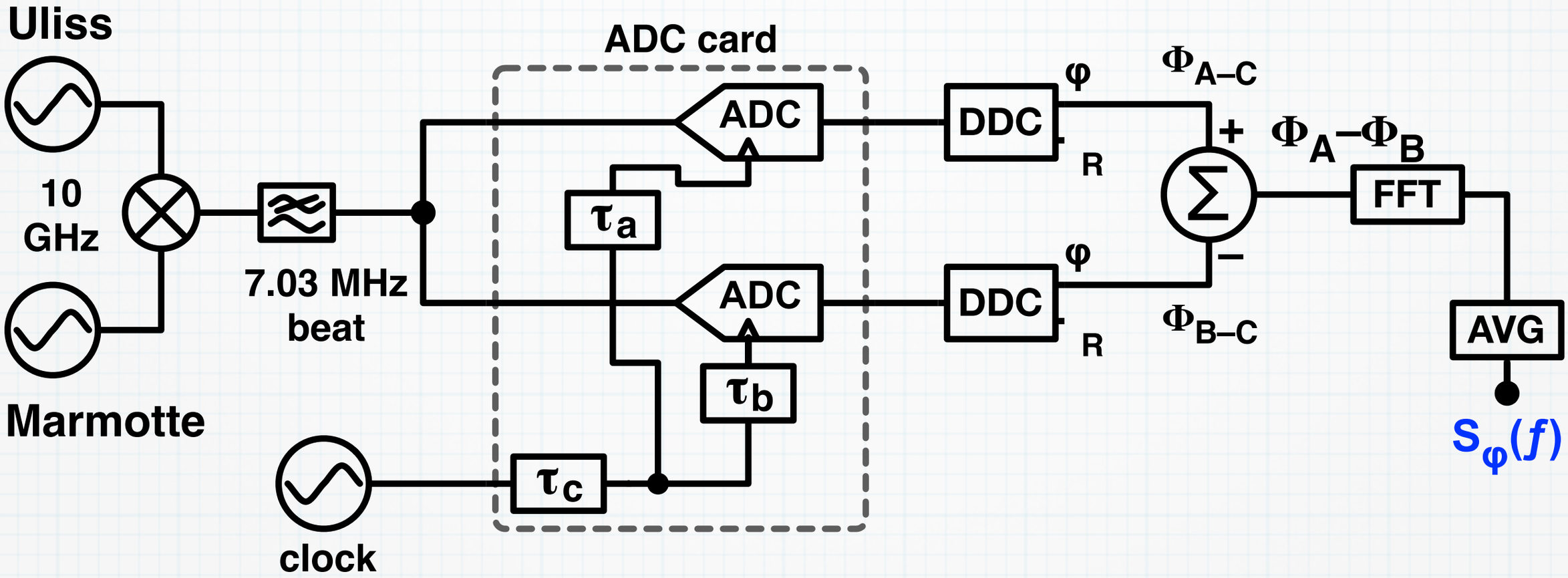
10 MHz, $V_{pp} \approx 0.95\ V_{FSR}$

AD9467 (Alazartech) Noise



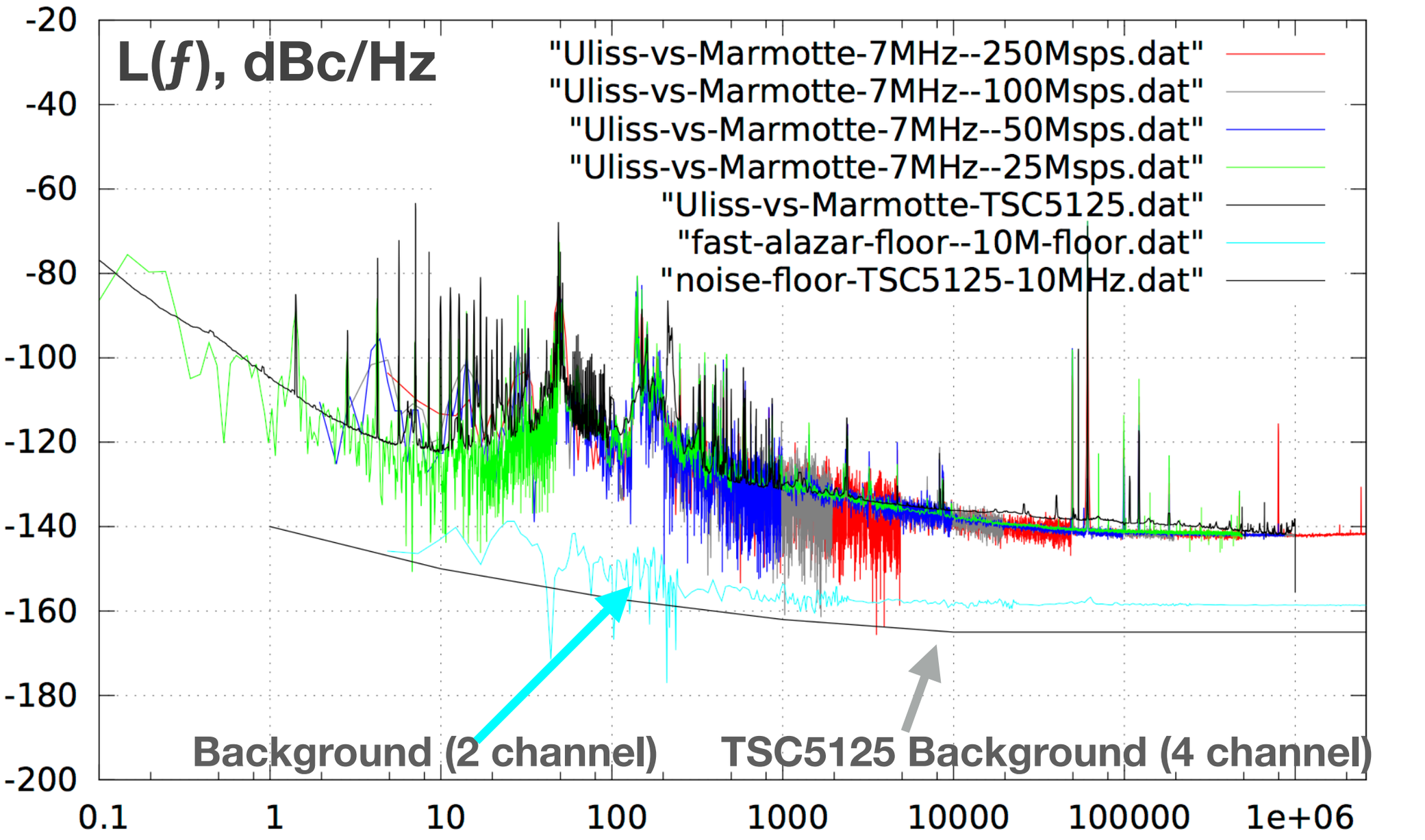
10 MHz, $V_{pp} \approx 0.95\ V_{FSR}$

Application to 10 GHz Cryogenic Oscillators



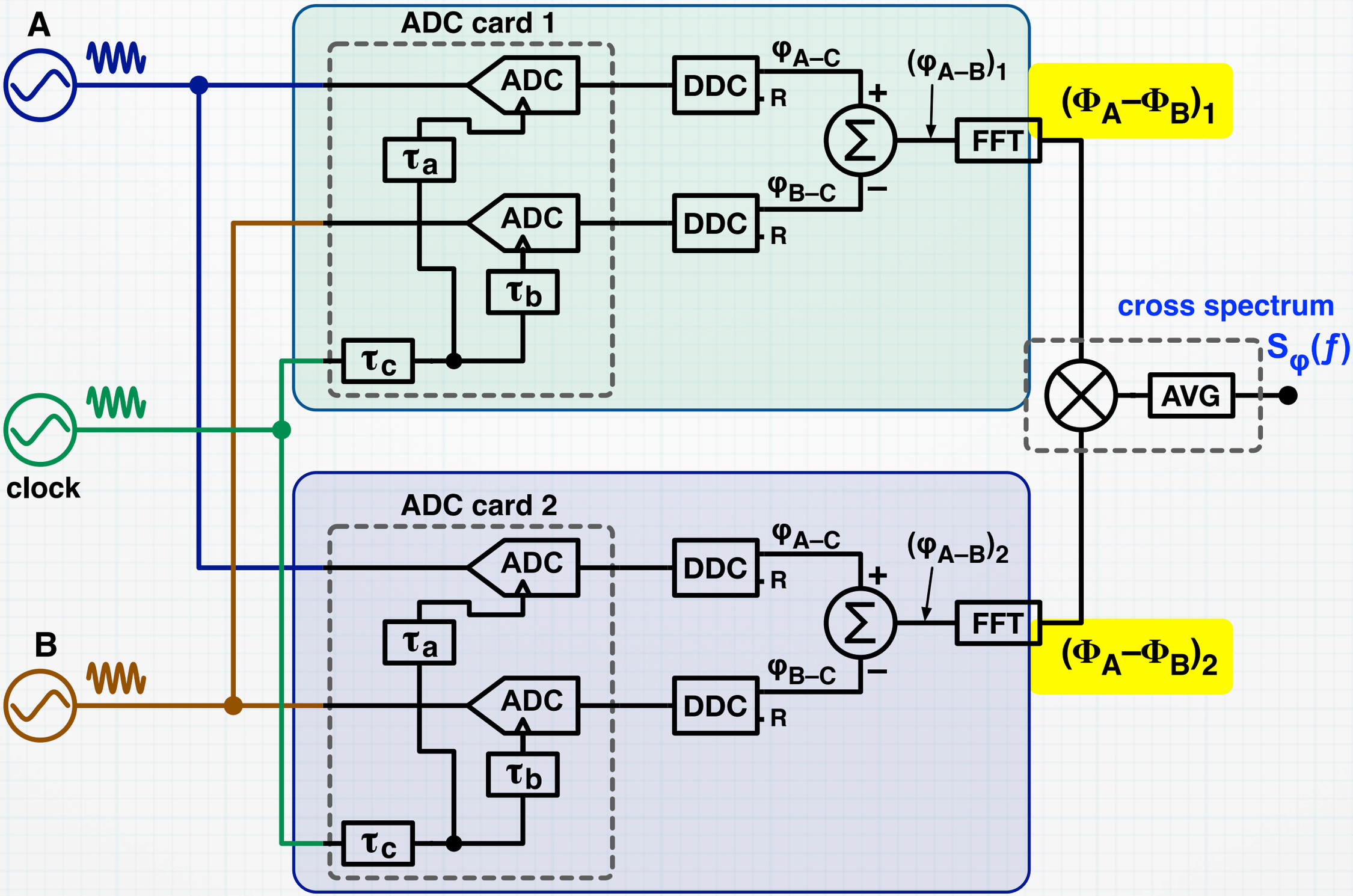
- Rejects the common-path jitter
- Takes in the differential jitter

Results

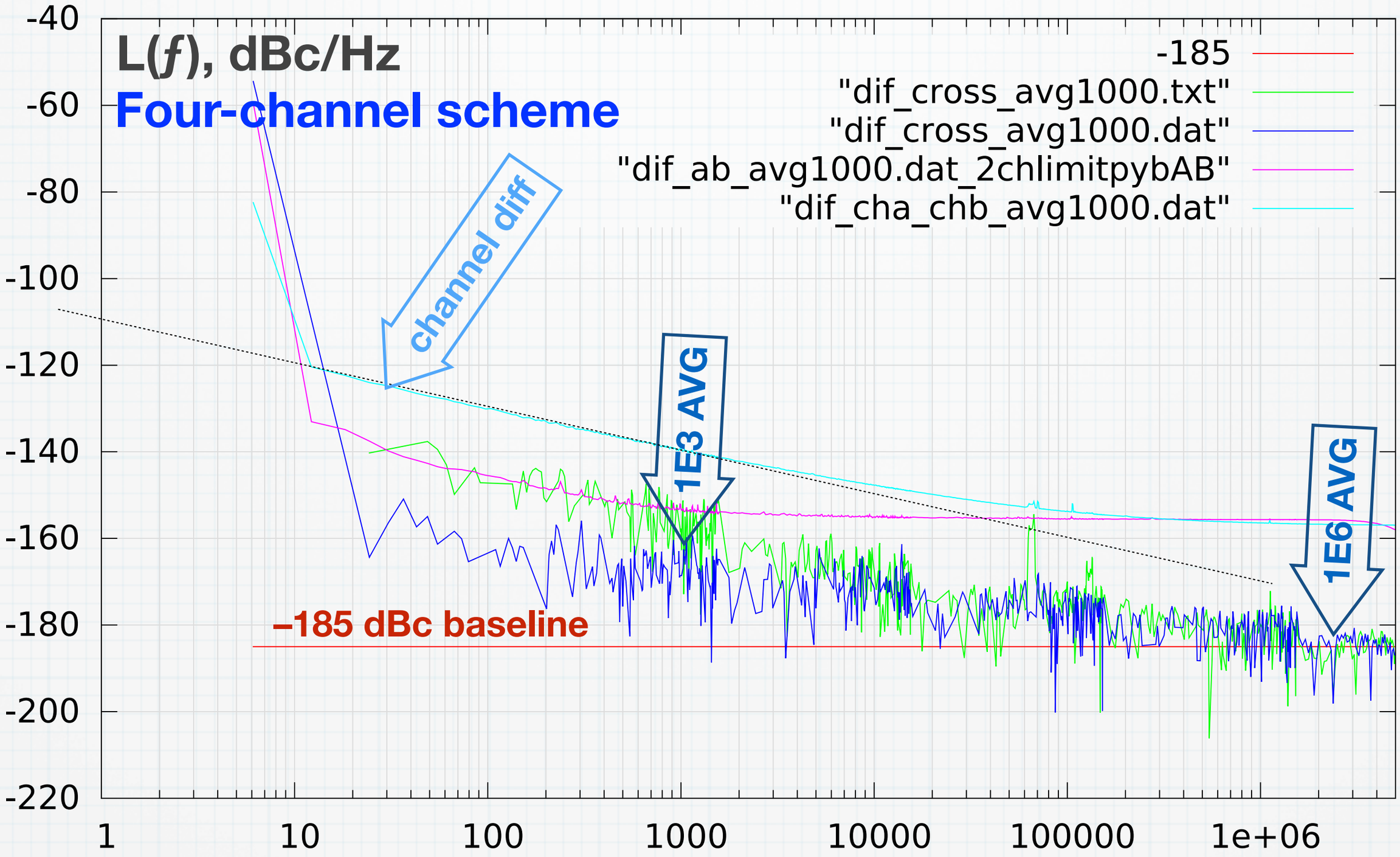


- Background noise 5–6 dB higher than that of the TSC5125
- We use 2 channel cross spectrum
- TSC5125 uses 4 channel cross spectrum

The Four-Channel Scheme

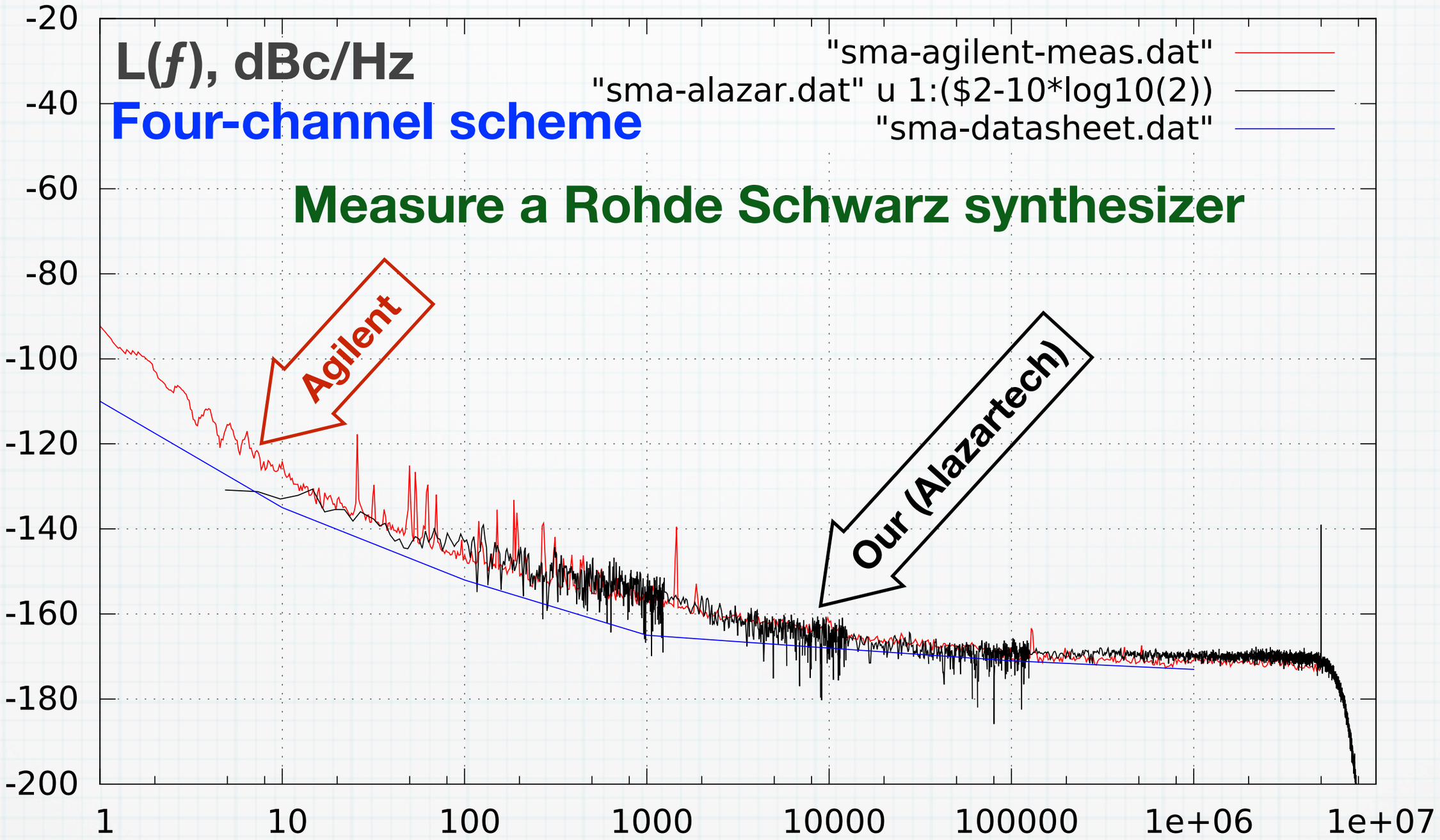


Background Noise



Compared to a Commercial Instrument

– this is done only to make sure that there is no calibration mistake –



Conclusions

- White noise
  - Depends on Fs and ENoB
  - Fits well the expectation
- Flicker –110 dBV^2/Hz best found
- First phase noise measurements, (direct & beat)
- Background –185 dBc with 4-channel scheme
- Modeling common-mode and differential jitter in progress
- Unwanted correlated effects still unknown

4 – DDSs

- Basics
- Advanced
- Experiments

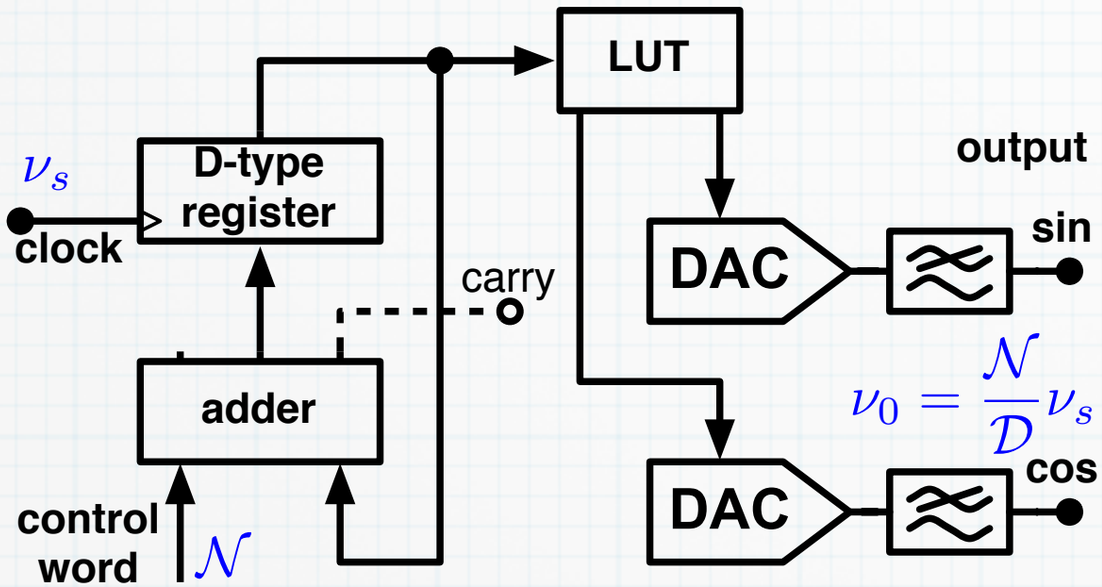
Basics

Basic DDS scheme

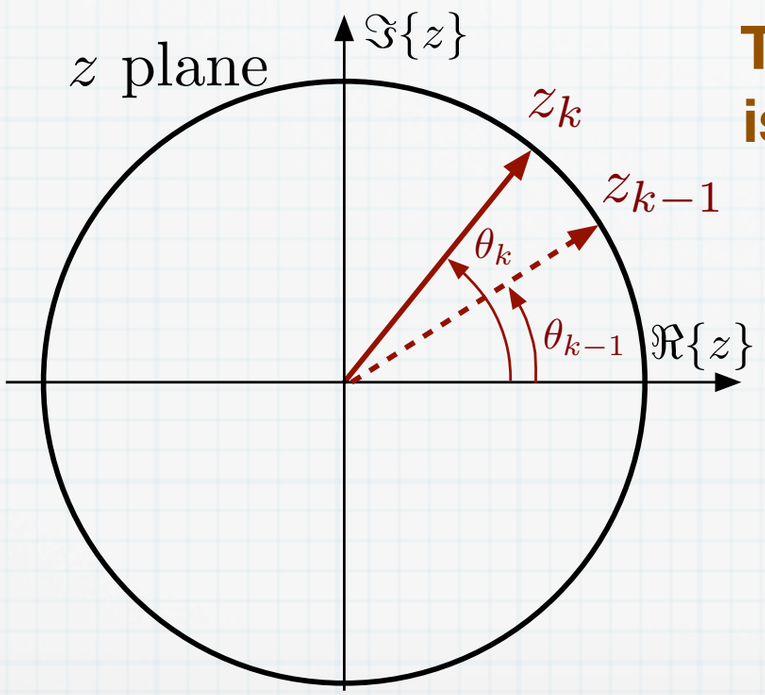
integer: $n_k = (n_{k-1} + \mathcal{N}) \bmod \mathcal{D}$

complex: $z_k = z_{k-1} \exp(j\eta)$

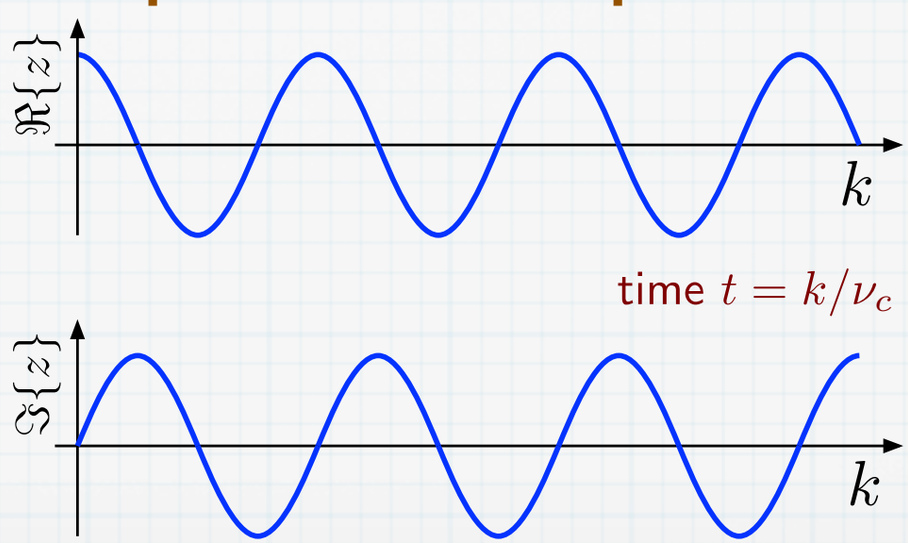
phase: $\theta_k = (\theta_{k-1} + \eta) \bmod 2\pi$



quantity	digital	analog
state variable	n	$\theta = 2\pi\dfrac{n}{\mathcal{D}}$
assoc. complex		$z = e^{j\theta}$
modulo	$\mathcal{D} = 2^m$	2π
increment	$\mathcal{N}$	$\eta = 2\pi\dfrac{\mathcal{N}}{\mathcal{D}}$
time	$k, \quad 0, 1, 2, \ldots$	$t = k/\nu_s$
clock freq. ν_s	output freq. $\nu_0 = \dfrac{\mathcal{N}}{\mathcal{D}}\nu_s$	

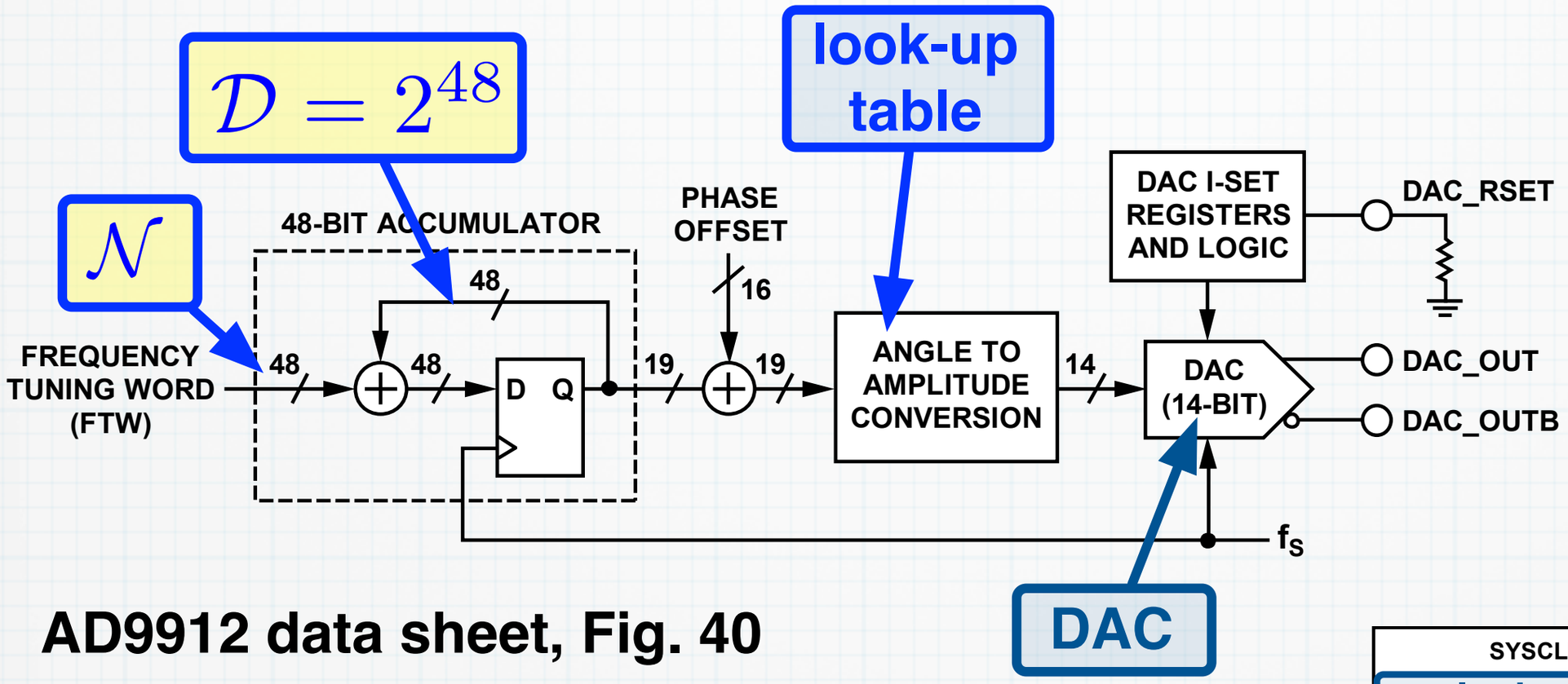


The contents *n* of the *m*-bit register is interpreted as a complex number

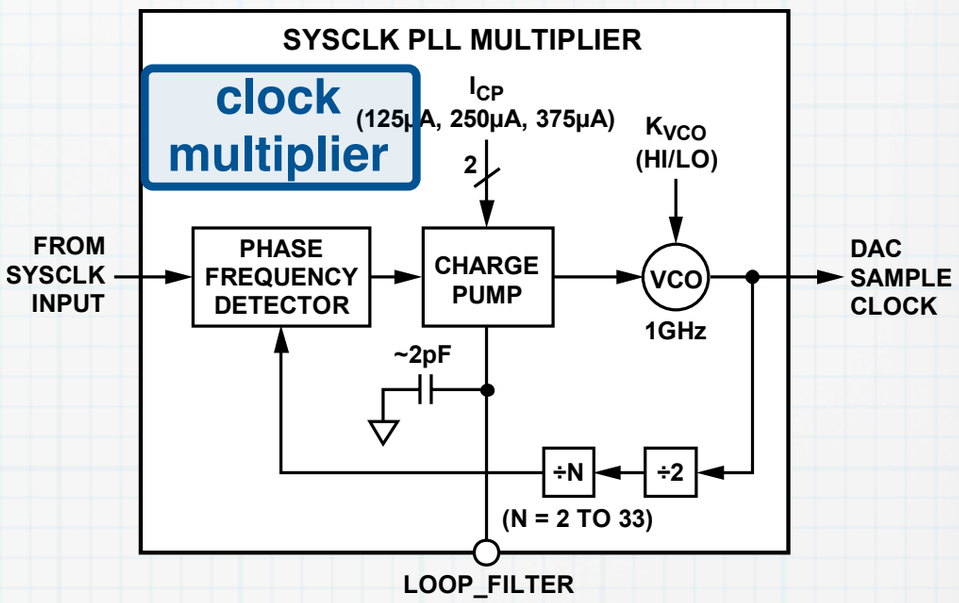


AD9912, a popular fast DDS

48 bit accumulator, 14 bit DAC, 1 GHz clock



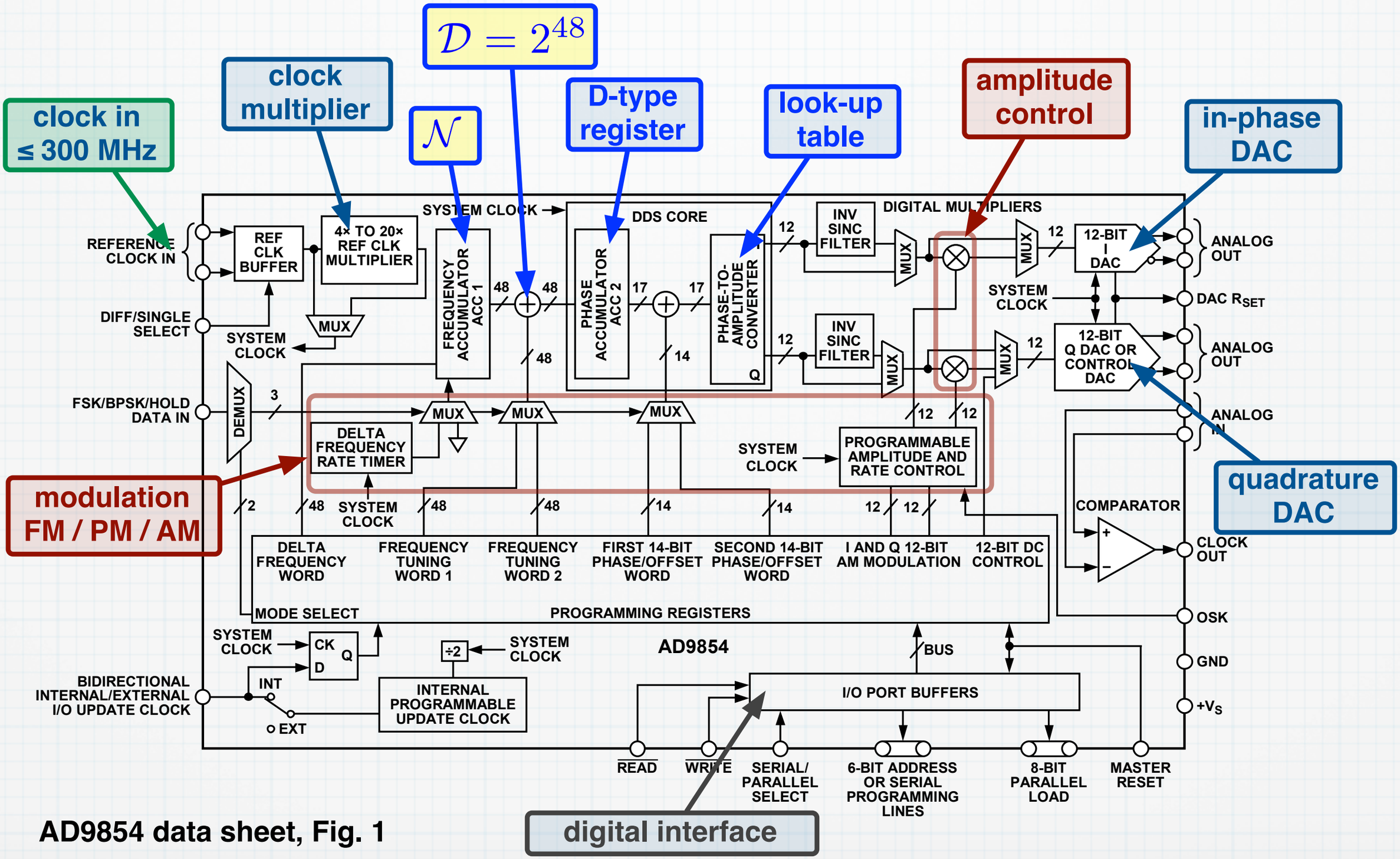
AD9912 data sheet, Fig. 40



AD9912 data sheet, Fig. 45

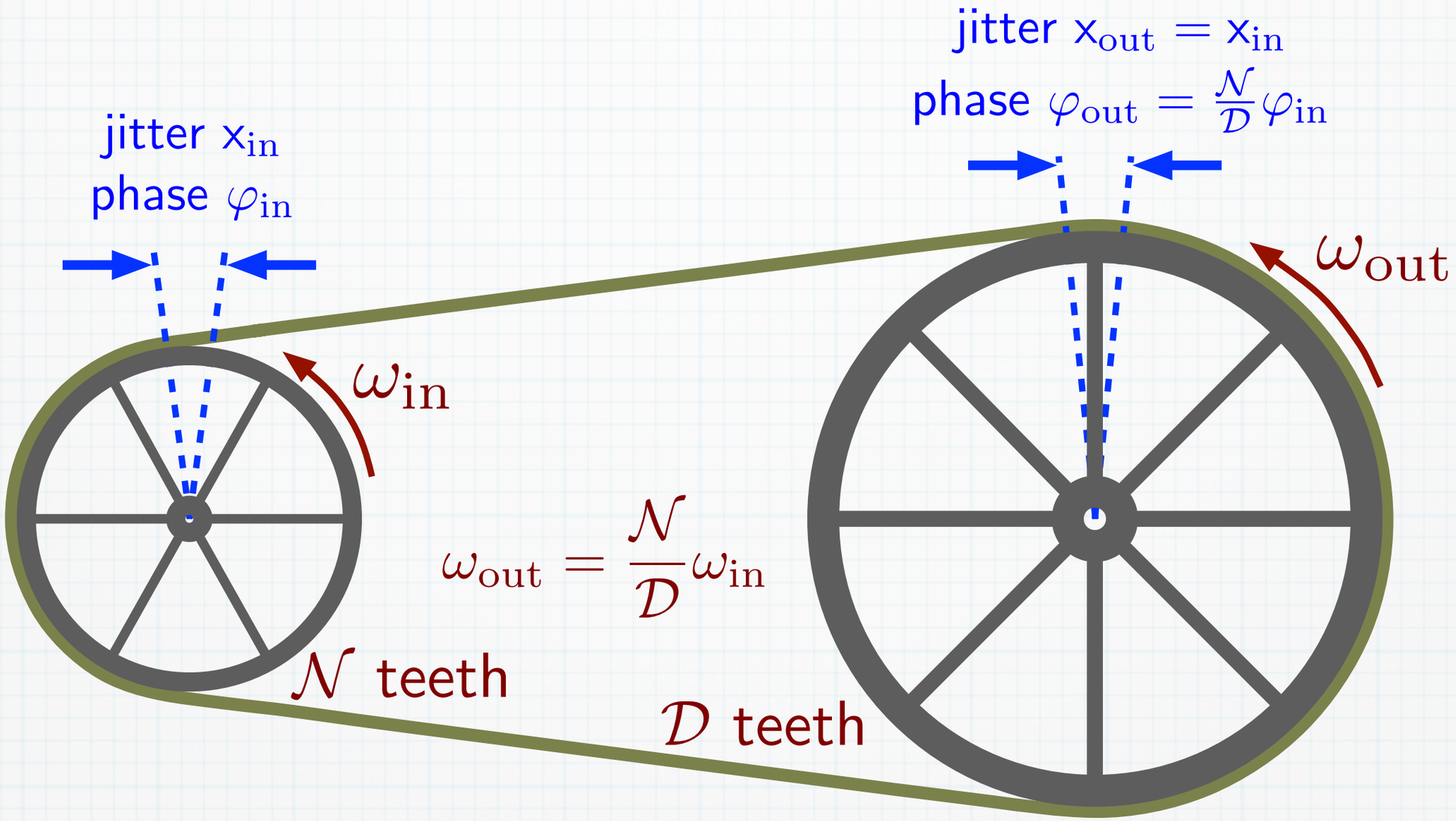
AD9854, a popular DDS

48 bit accumulator, 300 MHz clock, 12 bit DAC, I-Q output, AM/PM/FM capability



AD9854 data sheet, Fig. 1

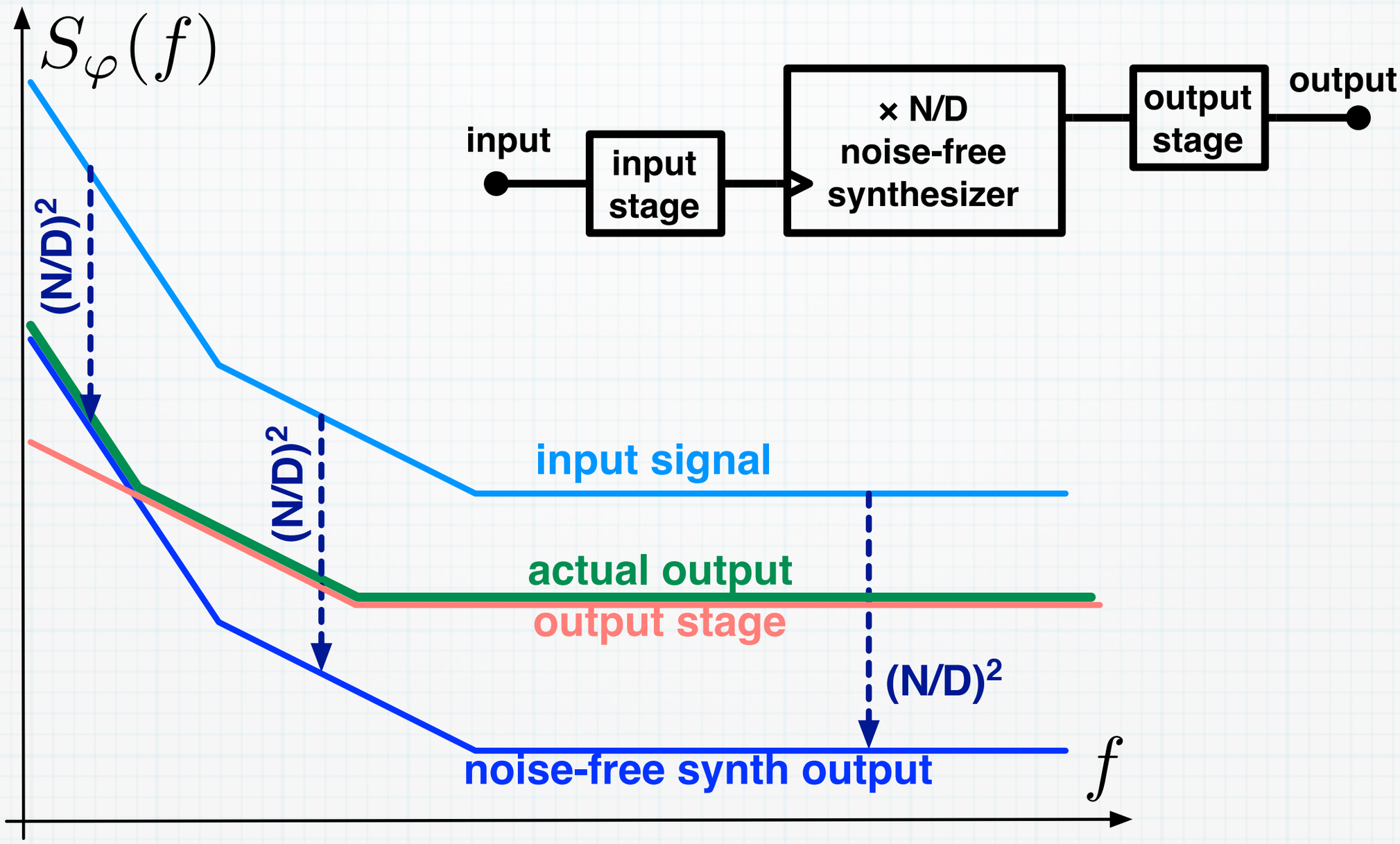
The noise-free synthesizer



- The noise-free synthesizer propagates the jitter x (phase time)
  - So, it scales the phase φ as *N*/*D*,
  - and the phase spectrum S_φ as $(N/D)^2$
- Notice the absence of sampling

The Egan model

for phase noise in frequency dividers

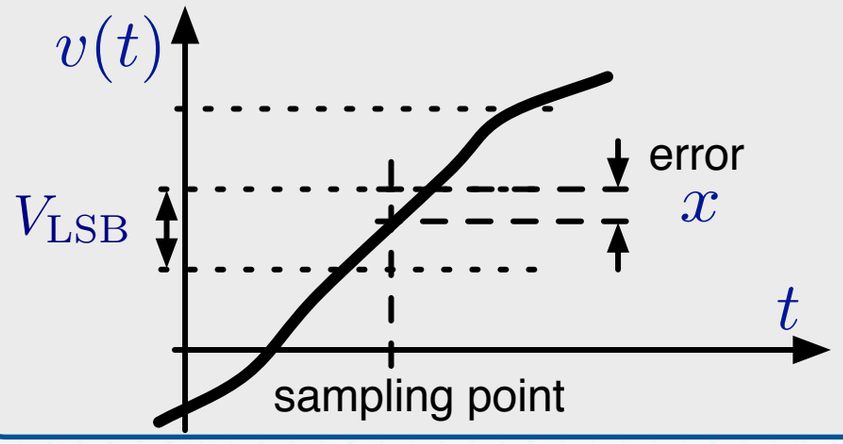


For N/D <<1, the scaled-down noise hits the output-stage limit

W.F. Egan, Modeling phase noise in frequency dividers, TUFFC 37(4), July 1990

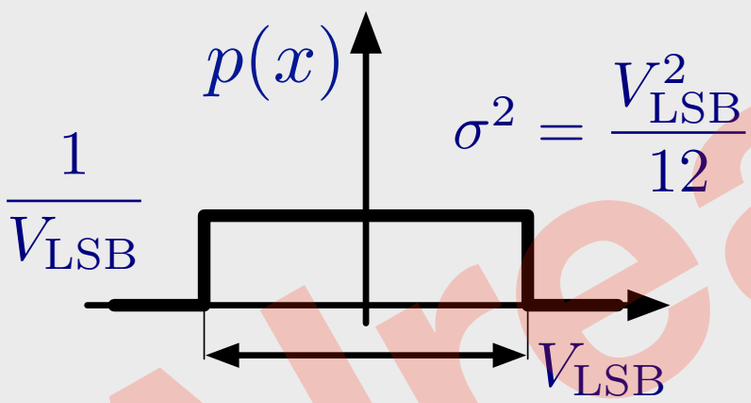
Quantization noise

W. R. Bennett, Spectra of quantized signals, Bell System Tech J. 27(4), July 1948



Analog-to-digital conversion introduces a quantization error x [$-V_{LSB}/2 \le x \le +V_{LSB}/2$]

n-bit conversion: $V_{\mathrm{LSB}} = \dfrac{V_{\mathrm{FSR}}}{2^n}$



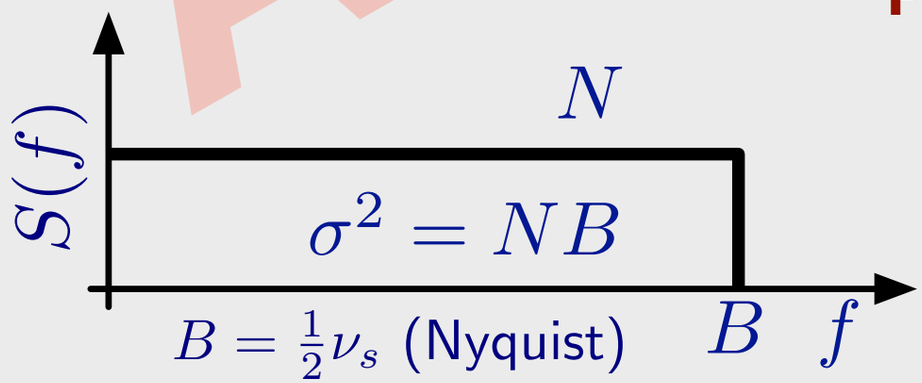
Wiener–Khintchine theorem: in ergodic systems, interchange time / ensemble

The noise can be calculated with statistics

$$\sigma^2 = \frac{V_{\mathrm{FSR}}^2}{12 \times 2^{2n}} \qquad \mathrm{V}^2$$

1/12 –> –10.8 dB

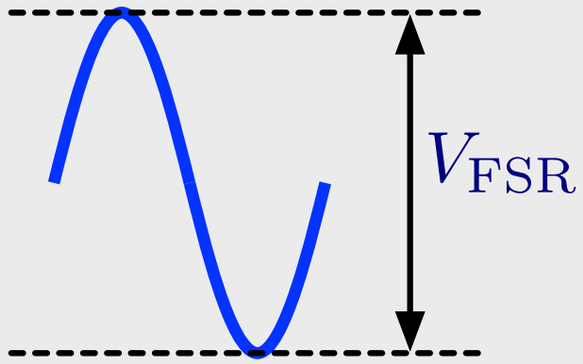
2^{2n} –> 6 dB/bit



Parseval theorem: Energy (power) calculated in time and in frequency is the same

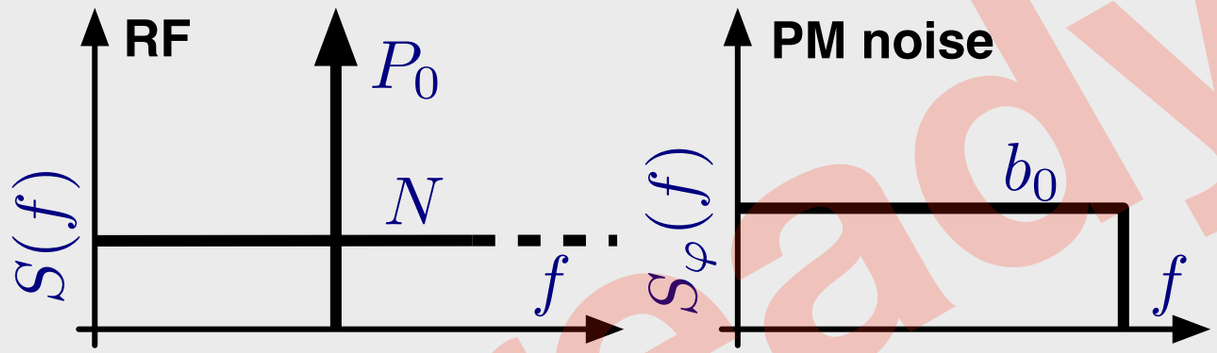
$$N = \frac{V_{\mathrm{FSR}}^2}{6 \times 2^{2n}\, \nu_s} \qquad \mathrm{V}^2/\mathrm{Hz}$$

Quantization and PM noise



The **maximum power** is

$$P_0 = \frac{1}{8} V_{\mathrm{FSR}}^2 \qquad \mathrm{V}^2$$



In the presence of white noise *N*, the **PM noise** is

$$b_0 = \frac{N}{P_0} \qquad \mathrm{rad}^2/\mathrm{Hz}$$

Recall the quantization noise

$$N = \frac{V_{\mathrm{FSR}}^2}{6 \times 2^{2n}\, \nu_s}$$

The white PM noise is

$$b_0 = \frac{4}{3}\, \frac{1}{2^{2n}\, \nu_s} \qquad \mathrm{rad}^2/\mathrm{Hz}$$

Example:

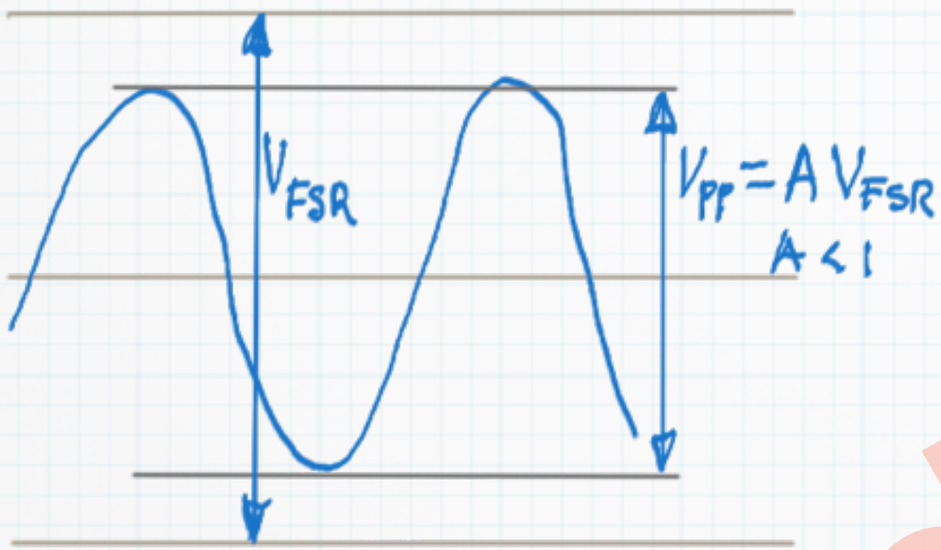
14 bit, 1 GHz –> –173 dB

14 bit , 400 MHz –> –169 dB

12 bit, 300 MHz –> –156 dB

Background noise

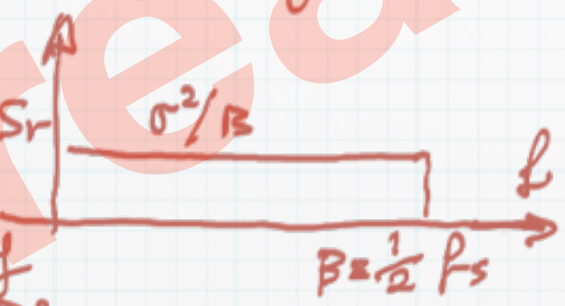
Sampling frequency f_s



Warning: We assume that the noise power is equally distributed in 0...B.

This is not true in our case because sampling and carrier are highly coherent. See Widraw-Kollar Appendix G for details.

Anyway, we temporarily accept the uniform distribution, hoping that the reality is not too far.



Signal power

$$P_0 = \frac{V_{PP}^2}{8} = \frac{A^2 V_{FSR}^2}{8}$$

Noise power

$$\sigma^2 = \frac{V_{LSB}^2}{12}$$

Parseval theorem

$$S_V = \frac{\sigma^2}{B} \quad B = 1/2\, f_s \Rightarrow S_V = \frac{V_{LSB}^2}{6 f_s}$$

Phase noise $S_\varphi = b_0$ (white)

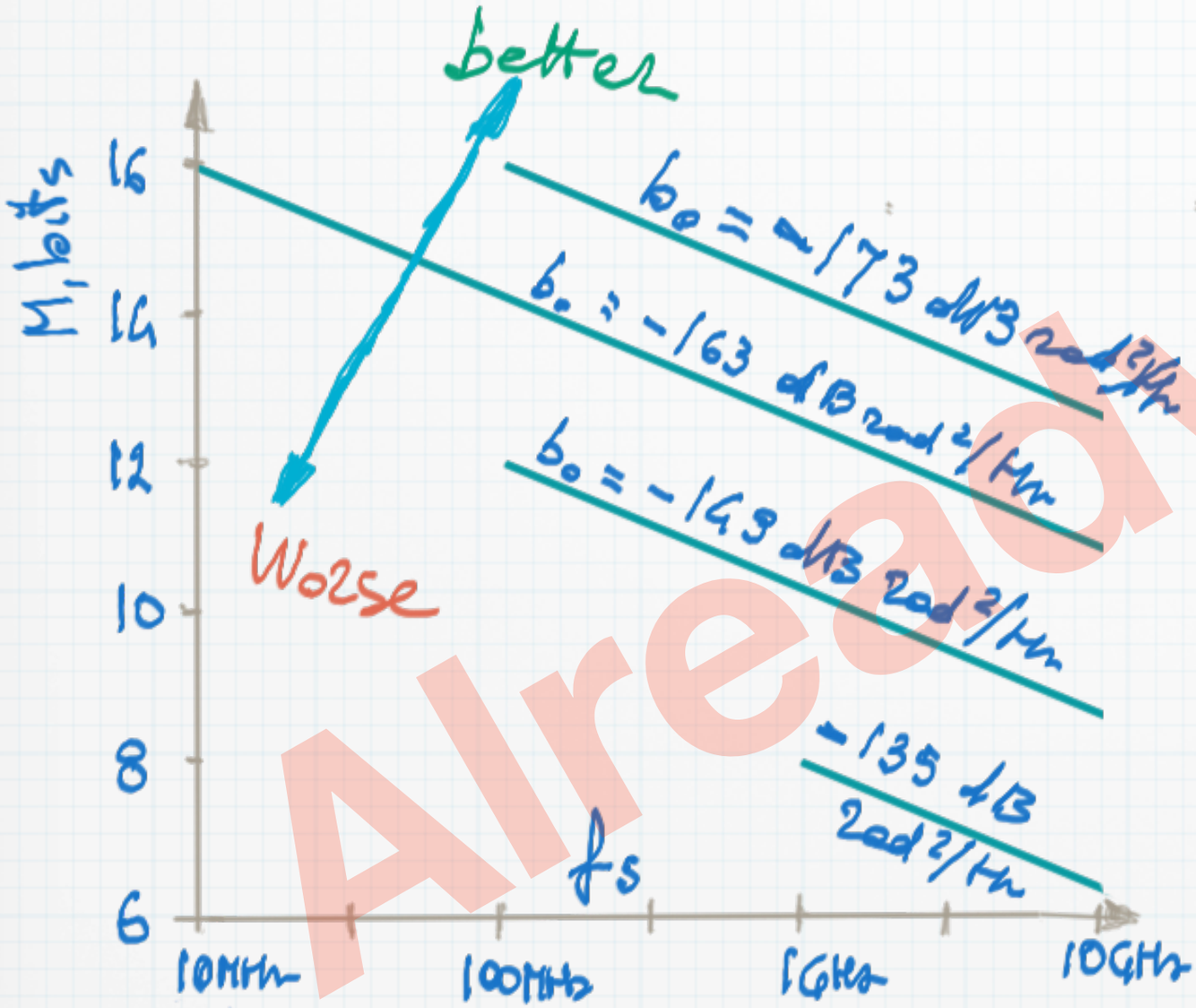
$$b_0 = \frac{S_V}{P_0} \qquad b_0 = \frac{V_{LSB}^2}{V_{FSR}^2} \cdot \frac{4}{3A^2 f_s}$$

$$b_0 = \frac{1}{(2^M)^2} \cdot \frac{4}{3A^2 f_s}$$

Approximation (fairly large V_P)

$A^2 = 2/3$ (-1.8 dB) $\Rightarrow b_0 \approx \frac{1}{(2^M)^2} \cdot \frac{2}{f_s}$

Background noise



$$b_0 = \frac{1}{(2^M)^2}\,\frac{4}{3A^2 f_s}$$

$$b_0 \propto \frac{1}{(2^M)^2}\,\frac{2}{f_s}$$

Cost of 6 dB improvement

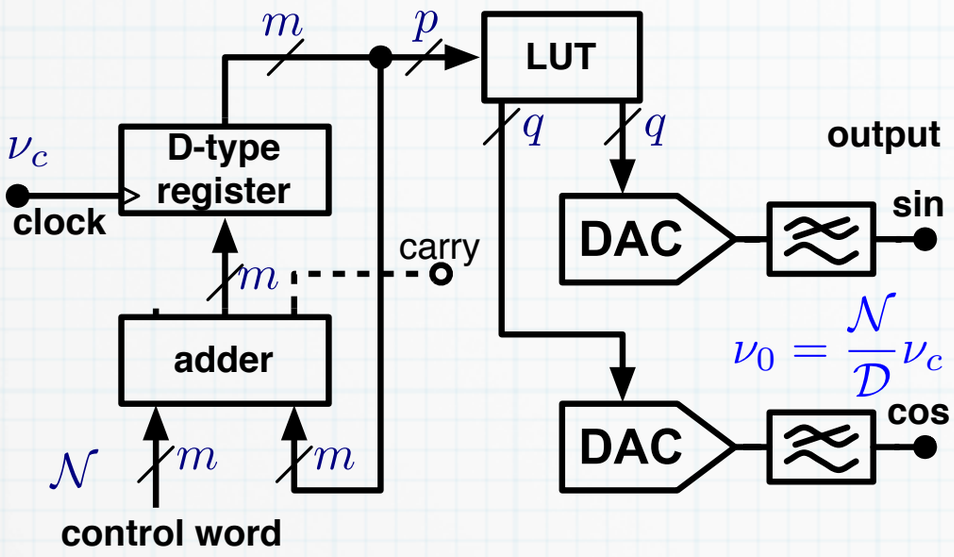
- 1 bit
- factor-of-4 f_s

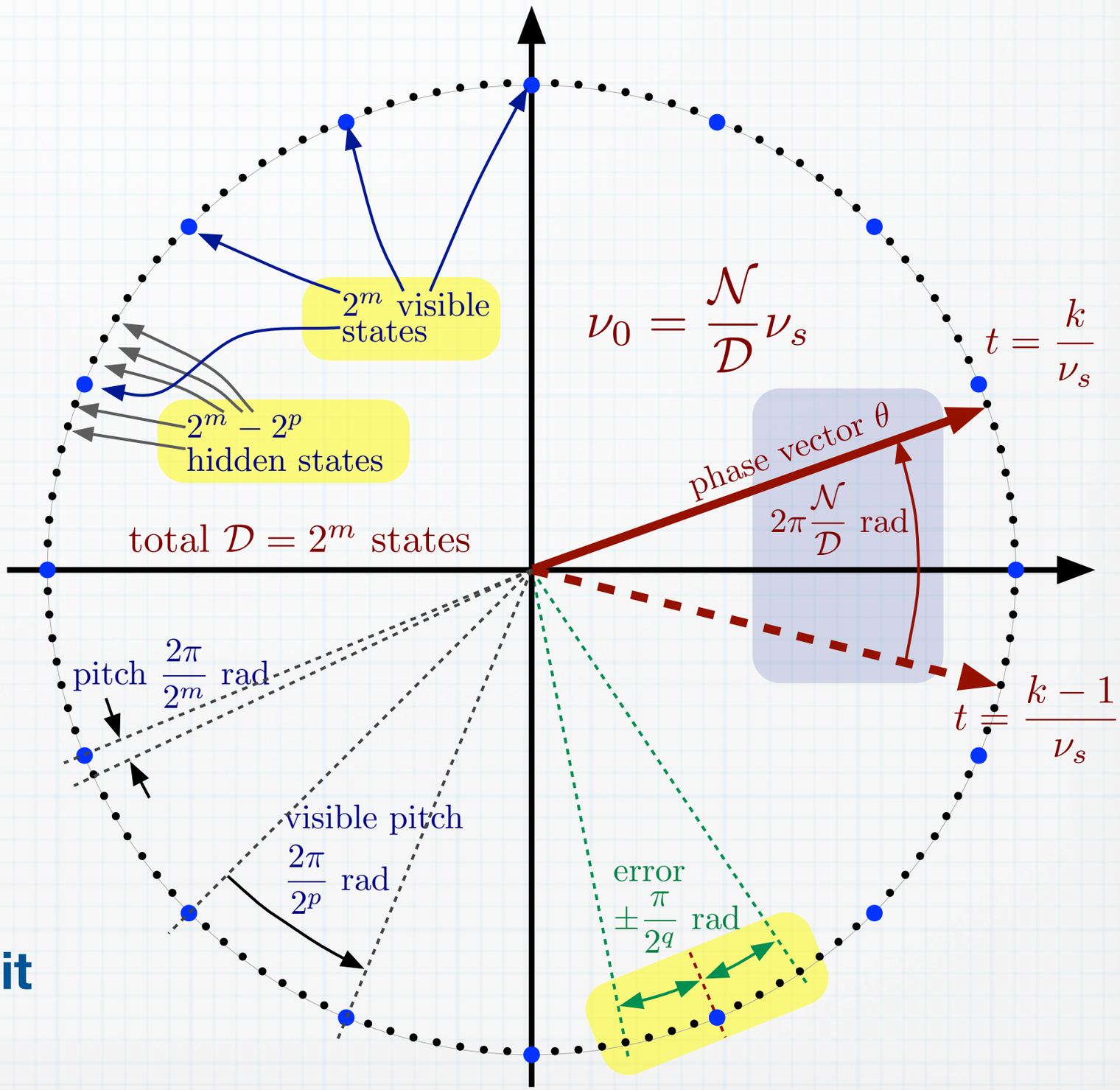
Obvious conclusion: practical ADCs feature lower b_0 at low f_s because of the higher no. of bits

Advanced

State-variable truncation

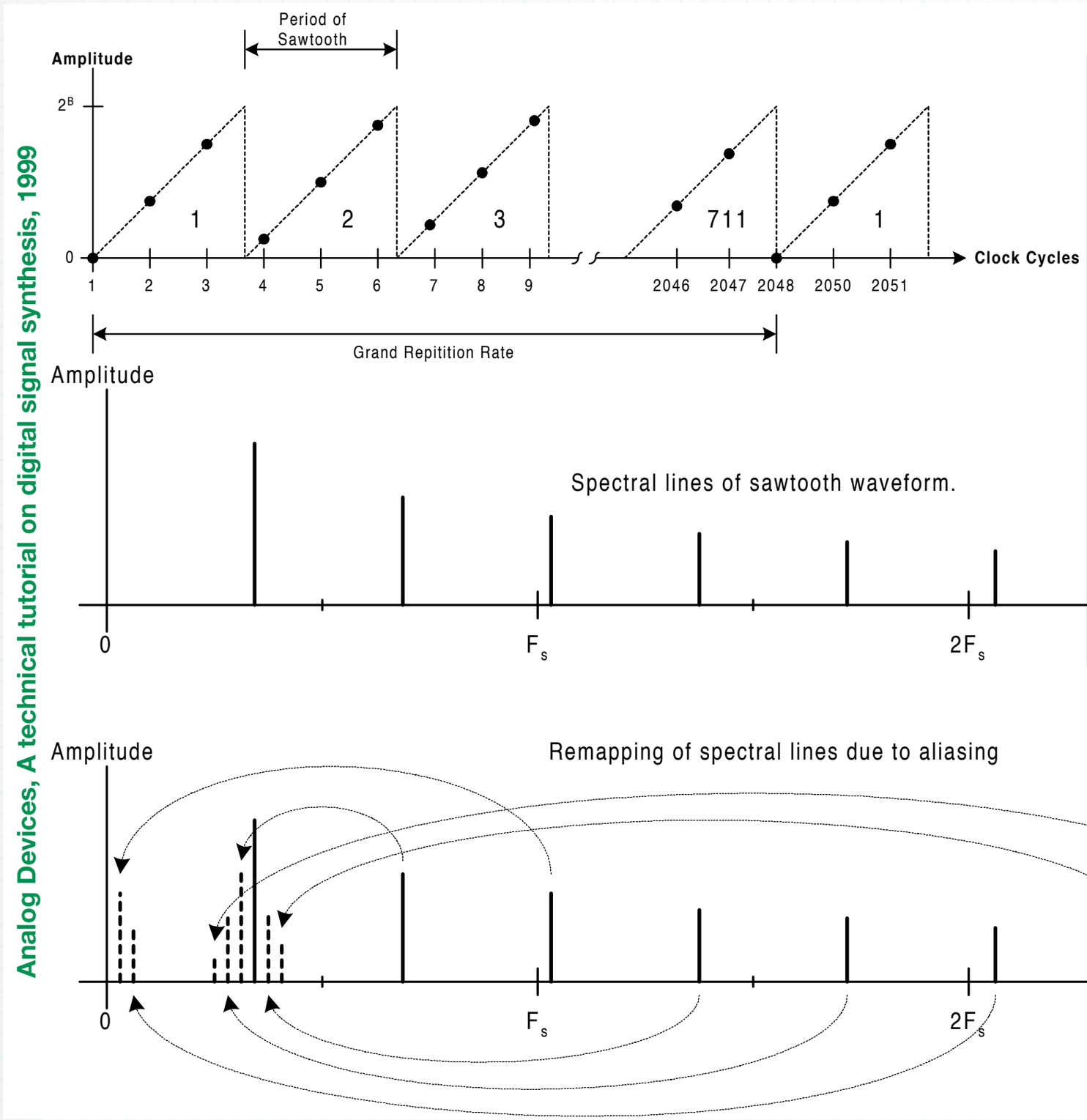
$$n_k = (n_{k-1} + \mathcal{N}) \bmod \mathcal{D}, \quad \mathcal{D} = 2^m$$

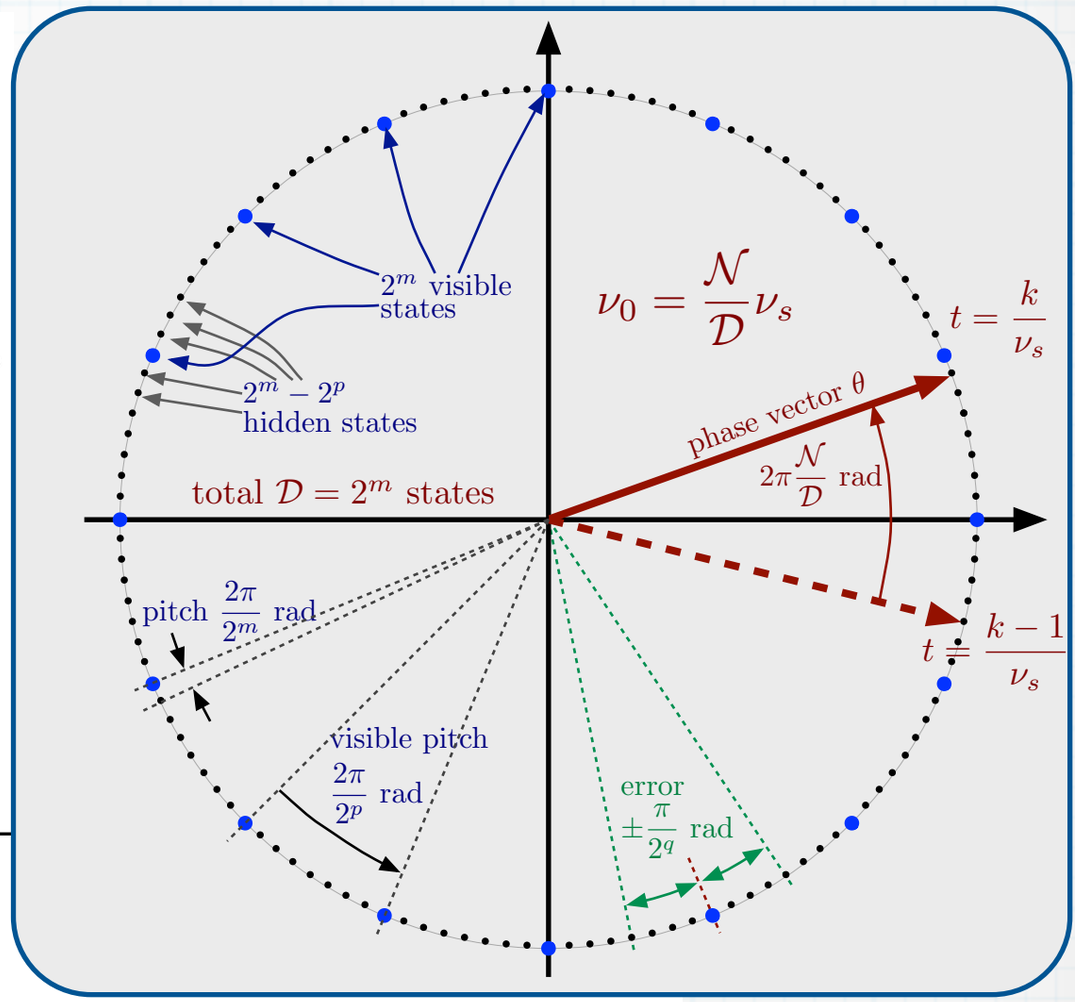




- **Only quantization shows up with full m-bit conversion**
- **Technology –> q max**
- **Why p > q**
- **Slow pseudorandom beat, 3d 6h 11m 15s @ 1 GHz, 48 bit**
- **Spurs –> next**

Truncation generates spurs

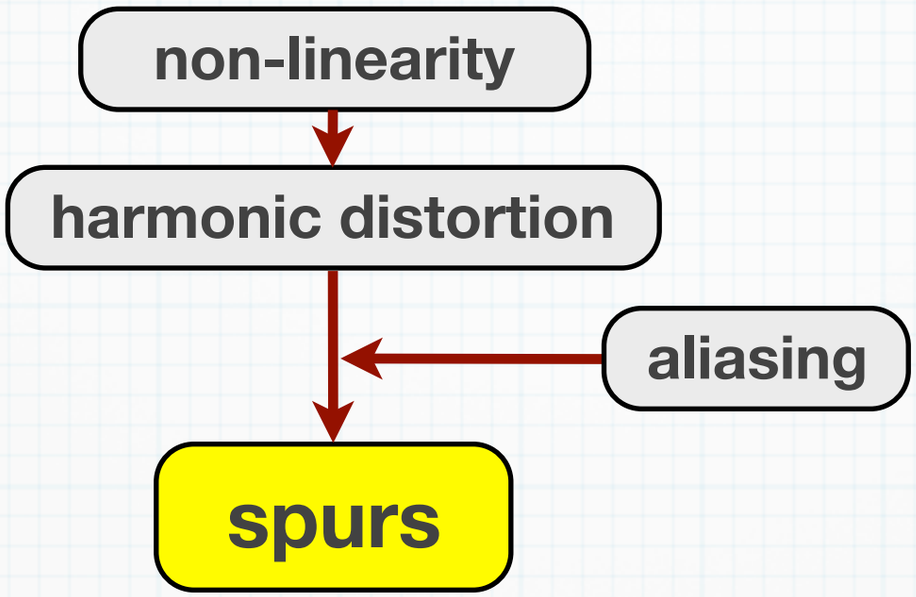


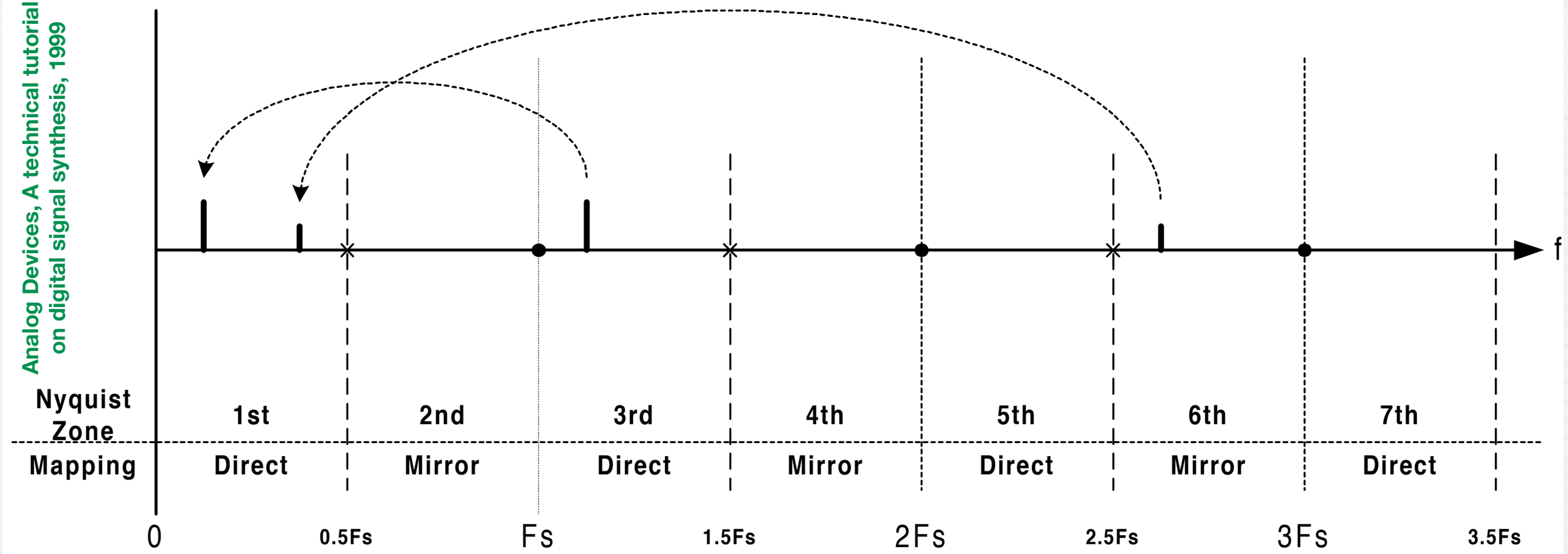


Analog Devices, A technical tutorial on digital signal synthesis, 1999

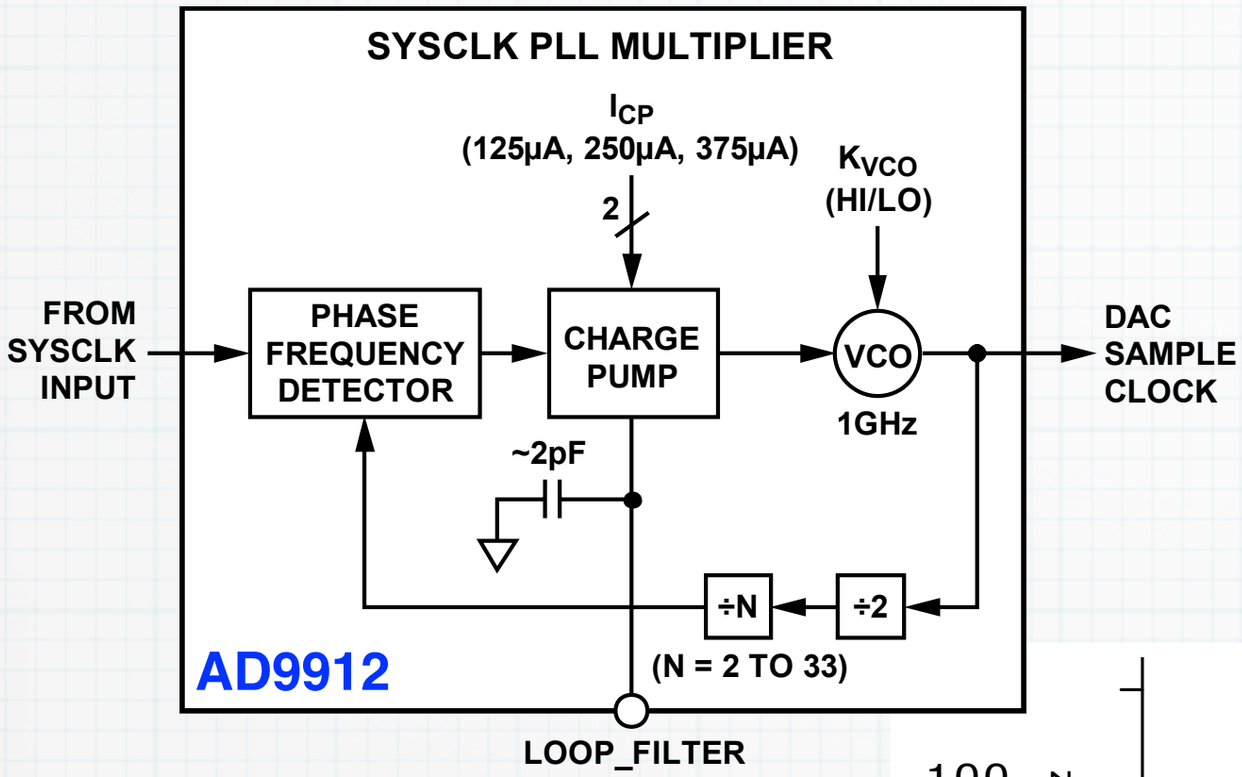
The power of spurs comes at expenses of white noise – yet not as one-to-one

Nonlinearity generates spurs



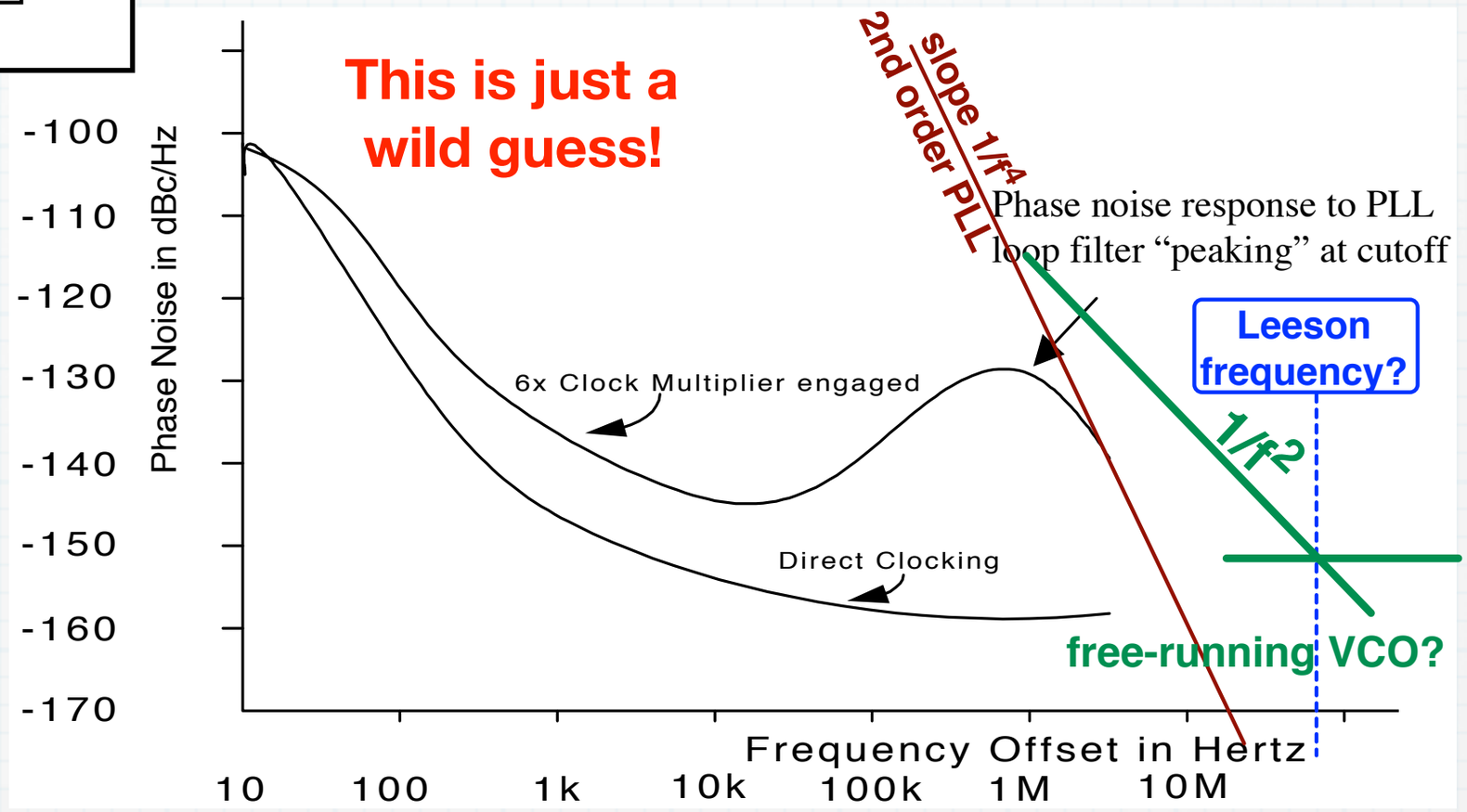


PLL clock multiplier



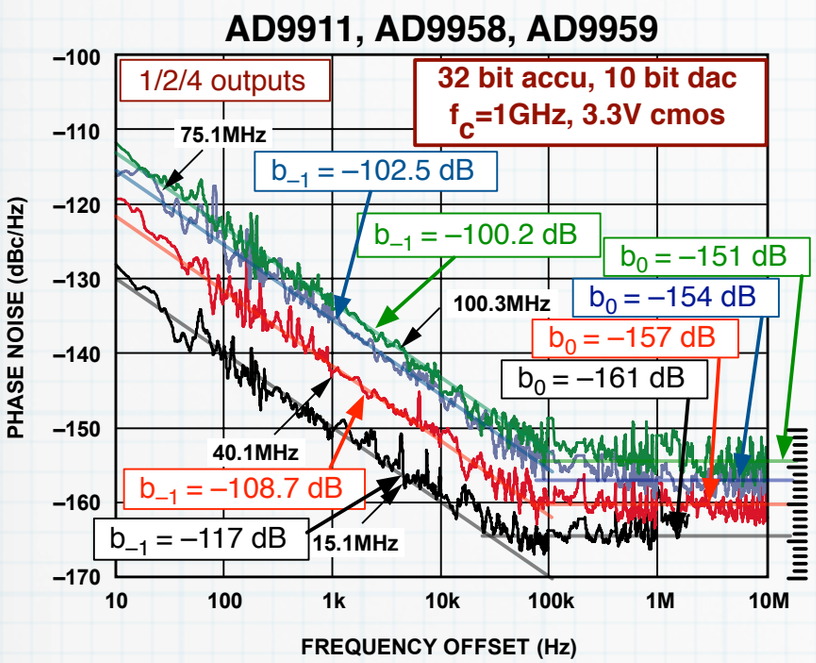
- On-Silicon LC oscillator
  - (also used in other AD devices)
- Literature suggests Q ≈ 5…10
  - Leeson f_L = 50–100 MHz
- Tight PLL is needed
- Divider noise
- No data from the manufacturer

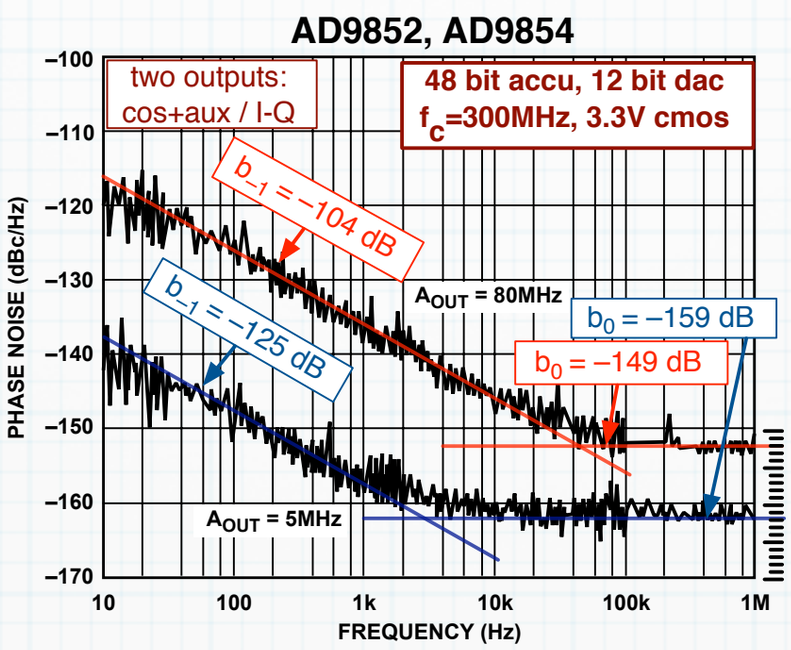
The AD 9854 is likely similar, yet the VCO frequency is 300 MHz

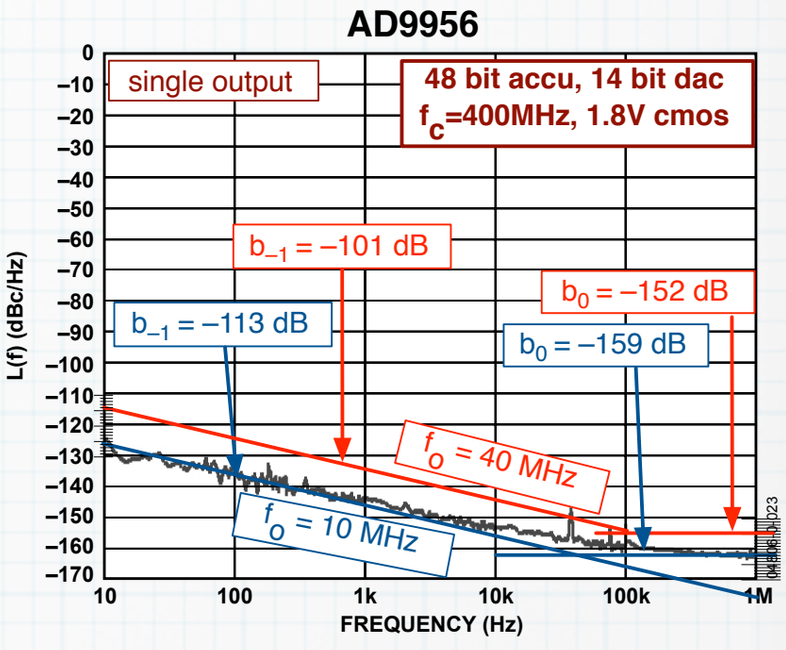


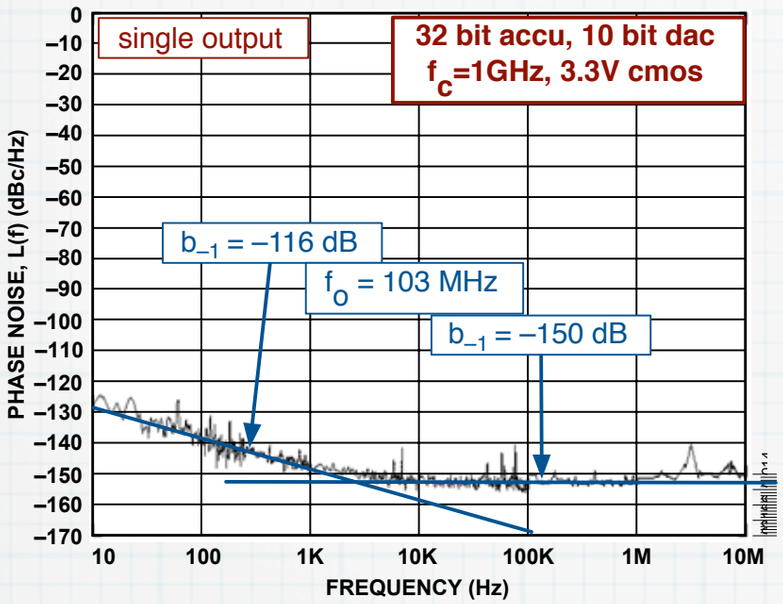
3.3 V: lower PM noise than 1.8 V

Probably related to the cell size and to the dynamic range









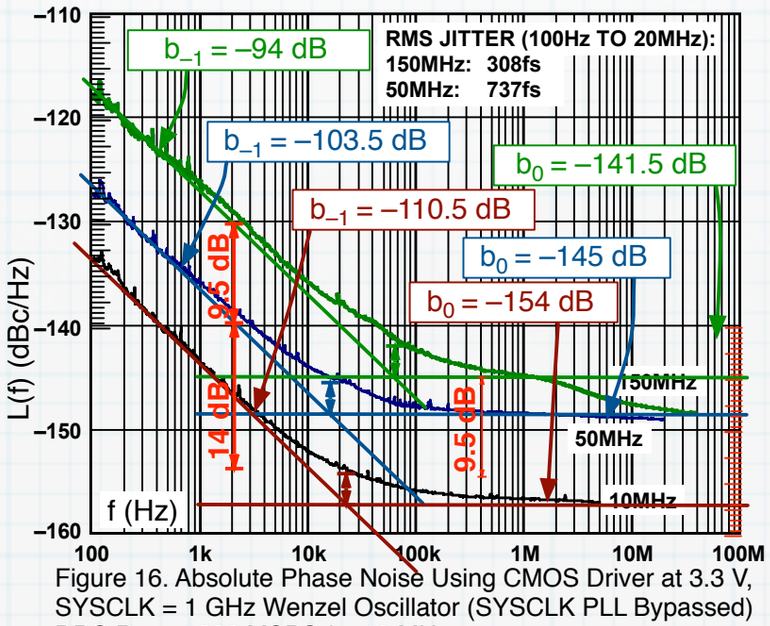
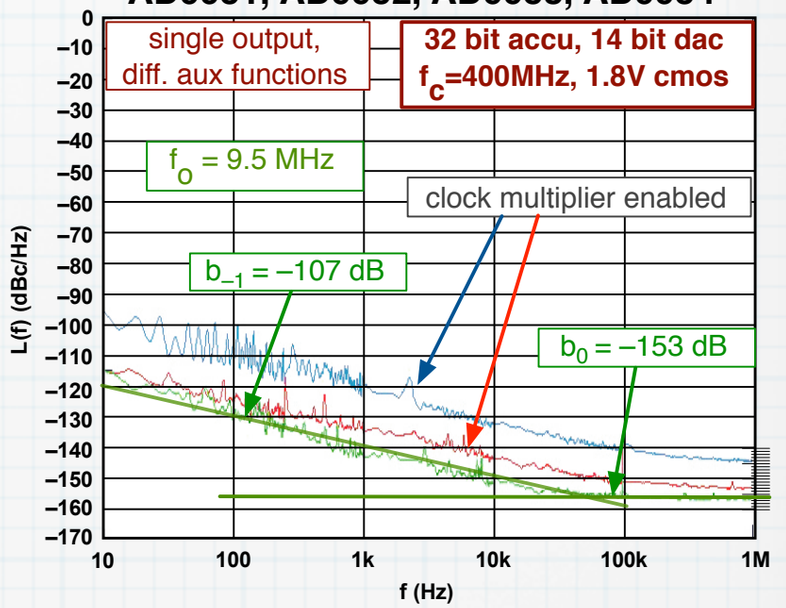


Figure 16. Absolute Phase Noise Using CMOS Driver at 3.3 V, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed) DDS Run at 200 MSPS for 10 MHz

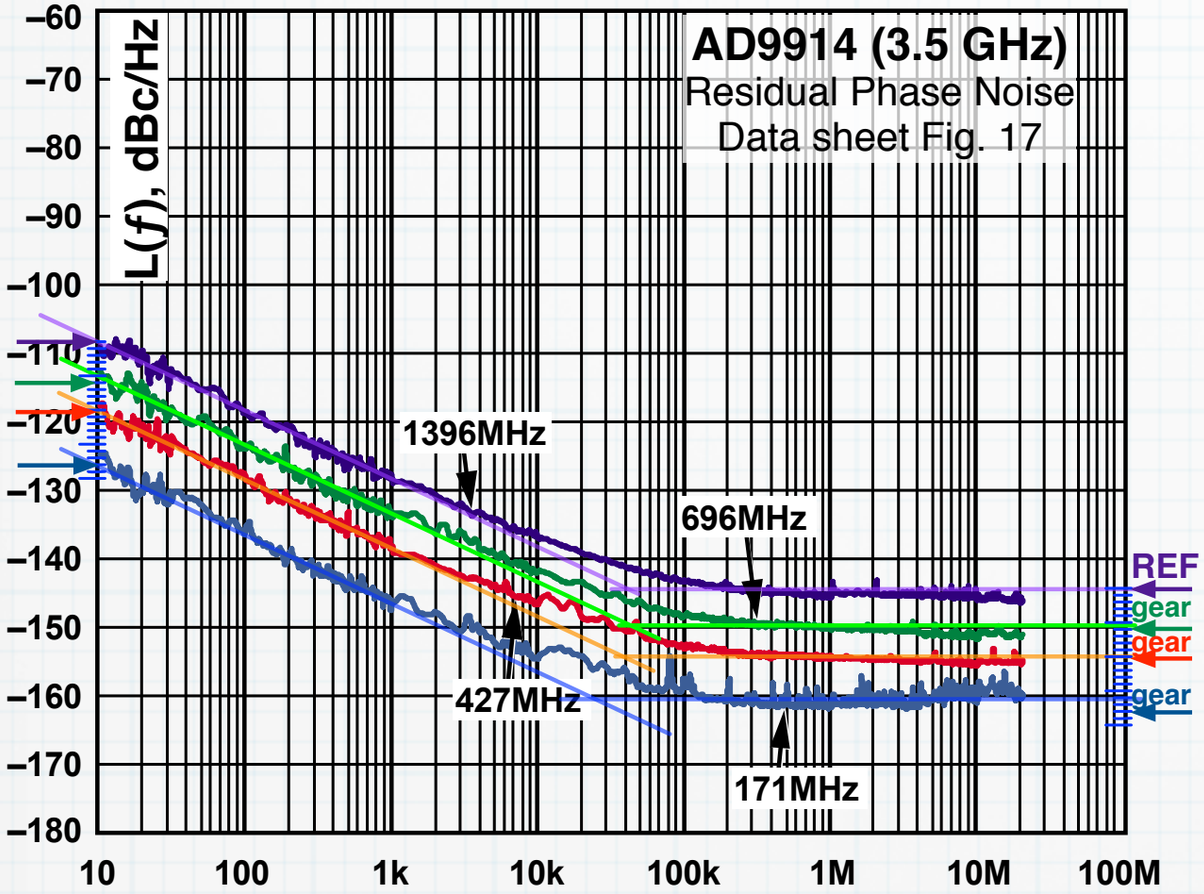


E. Rubiola, Mar 2007 (adapted from the Analog Devices data sheets)

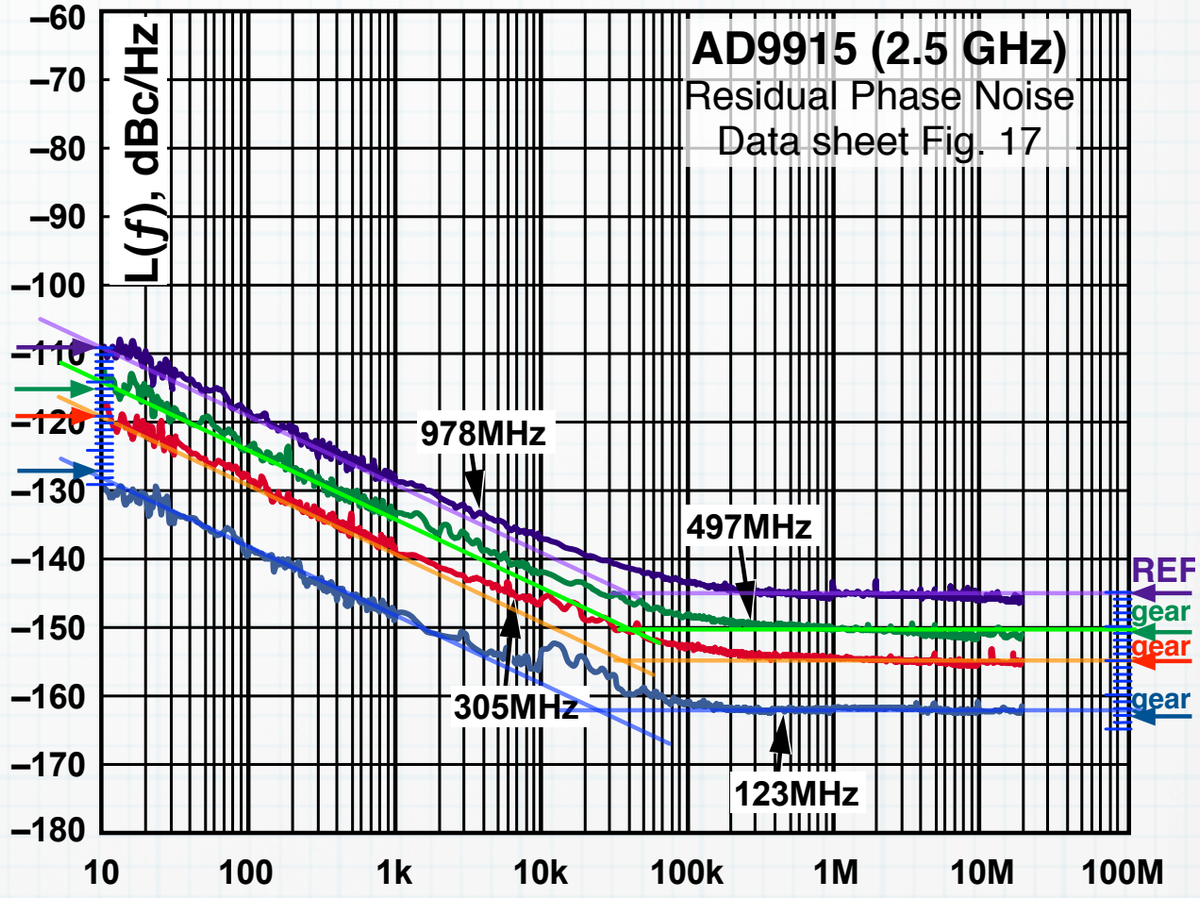
Plots originally used to extract the noise parameters

High-Frequency DDSs

AD9914 12 bit, 3.5 GHz
64 bit accumulator (190 pHz res)



AD9915 12 bit, 2.5 GHz
64 bit accumulator (135 pHz res)



Residual noise is close to that of the gear-box model

Plots are from the manufacturer data sheet

Whether spurs are removed or not, is not said

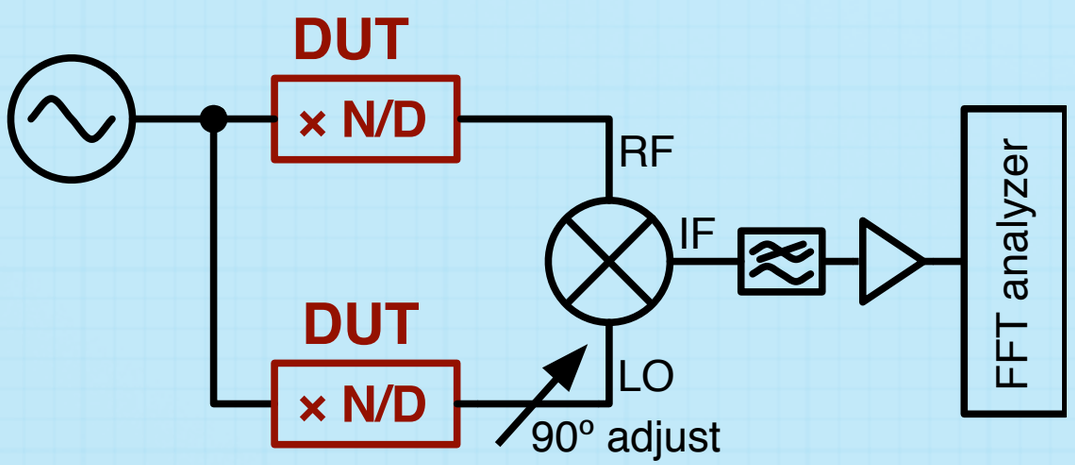
Experiments

- AD9912 demo board
- AD9854 (9914) demo board
- Claudio's AD9854 board
  - V1 – Current feedback OPA output stage
    - 25Ω input impedance, 8 nV/√Hz noise, kHz coupled
  - V2 – Balun and MAV-11 RF output amplifier
    - F = 3.6 dB, AC coupled (≥1–2) MHz
      - Specified above 50 MHz, yet works well below

Experimental method (PM noise)

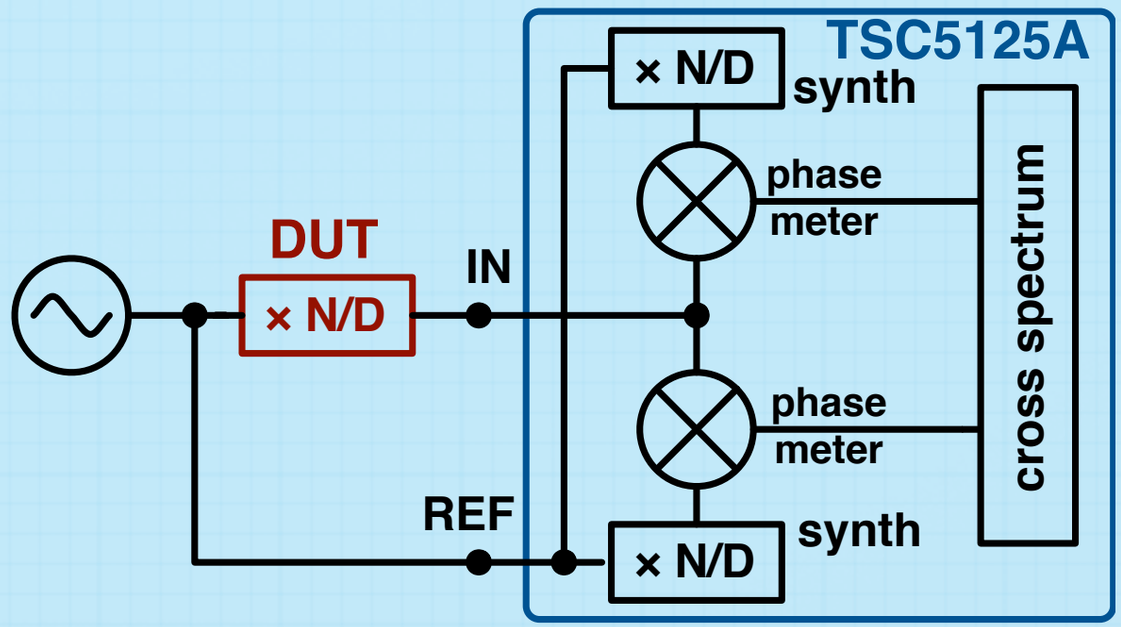
- Pseudorandom noise, slow beat (days)
- The probability that two accumulators are in phase is ≈ 0
- Two separate DDS driven by the same clock have a random and constant delay
- The delay de-correlates the two realizations, which makes the phase measurement possible

Single channel

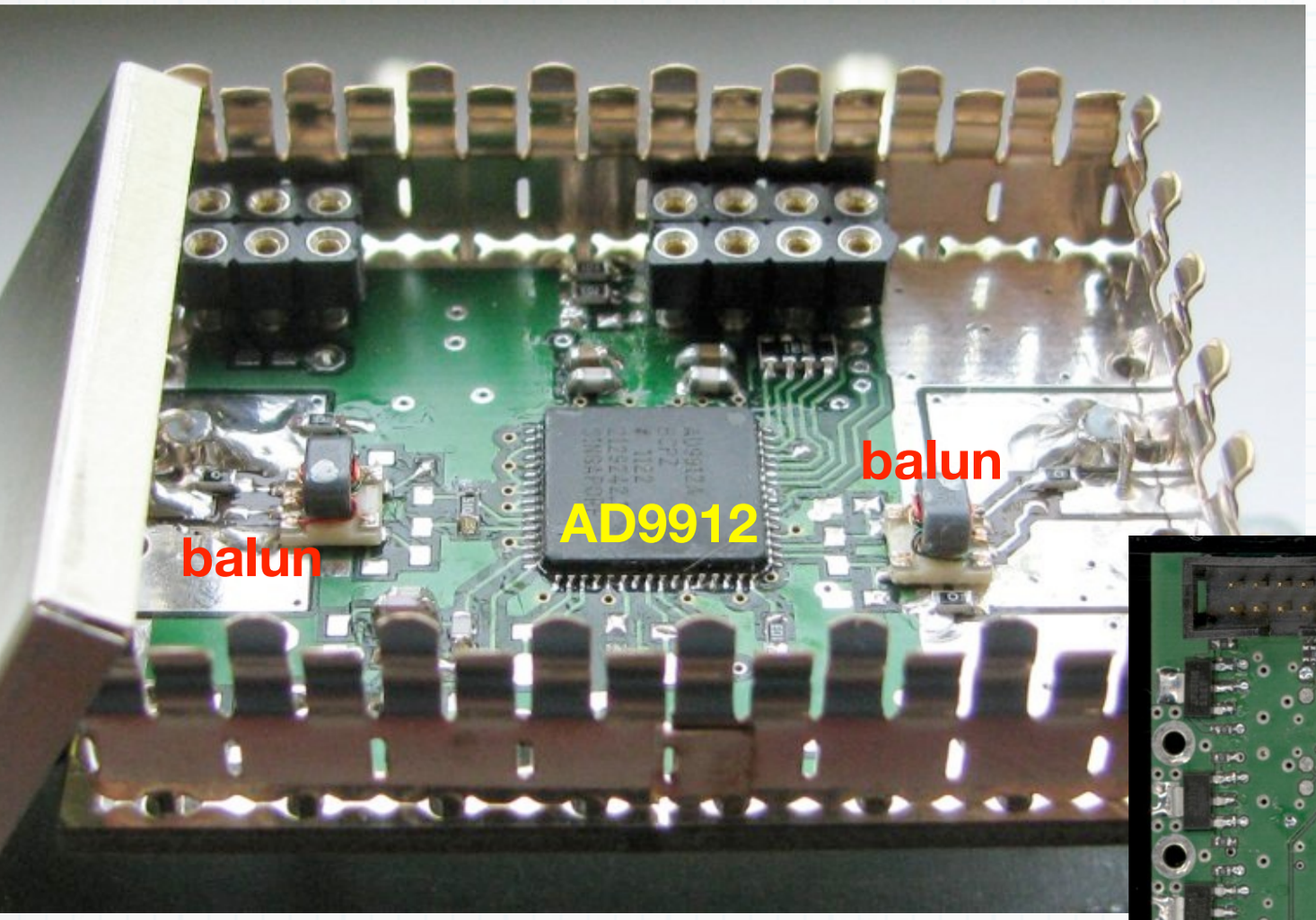


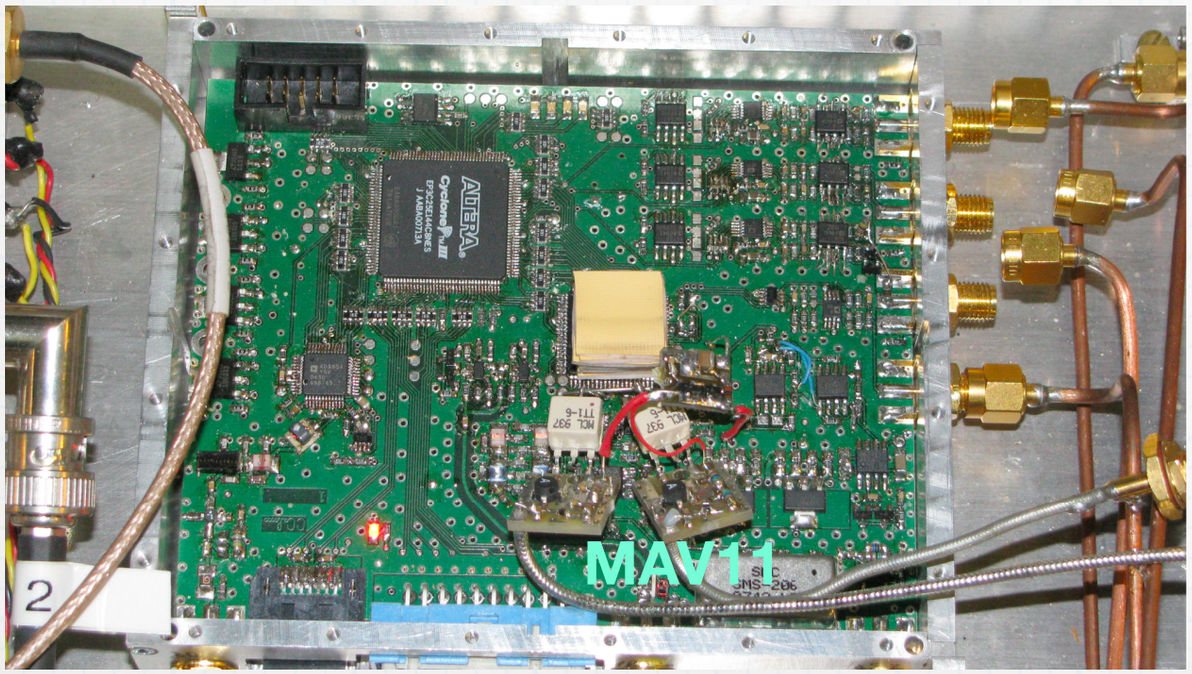
Dual channel

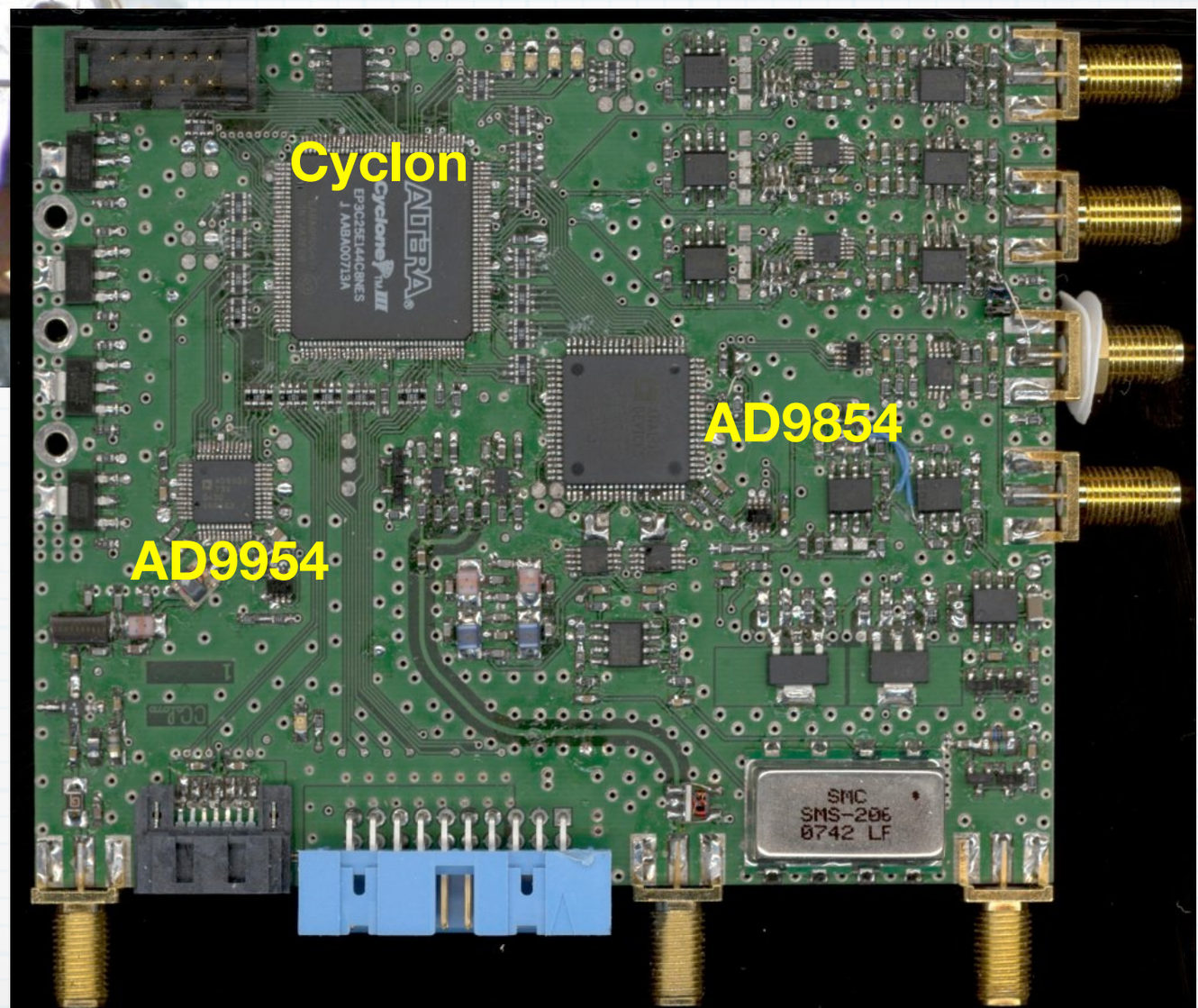
kind of virtual mixer, after (sub)sampling & direct ADC



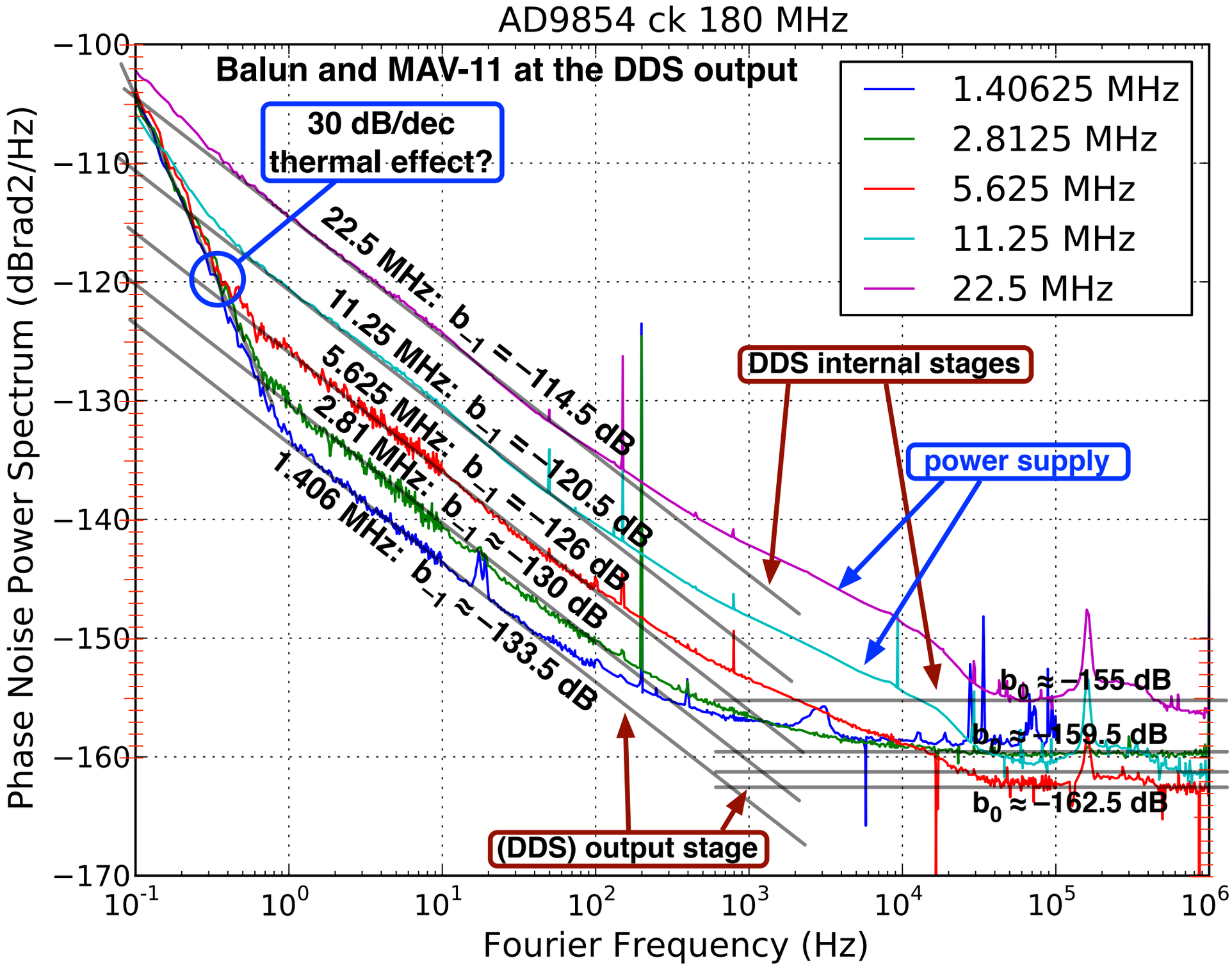
Claudio's prototypes





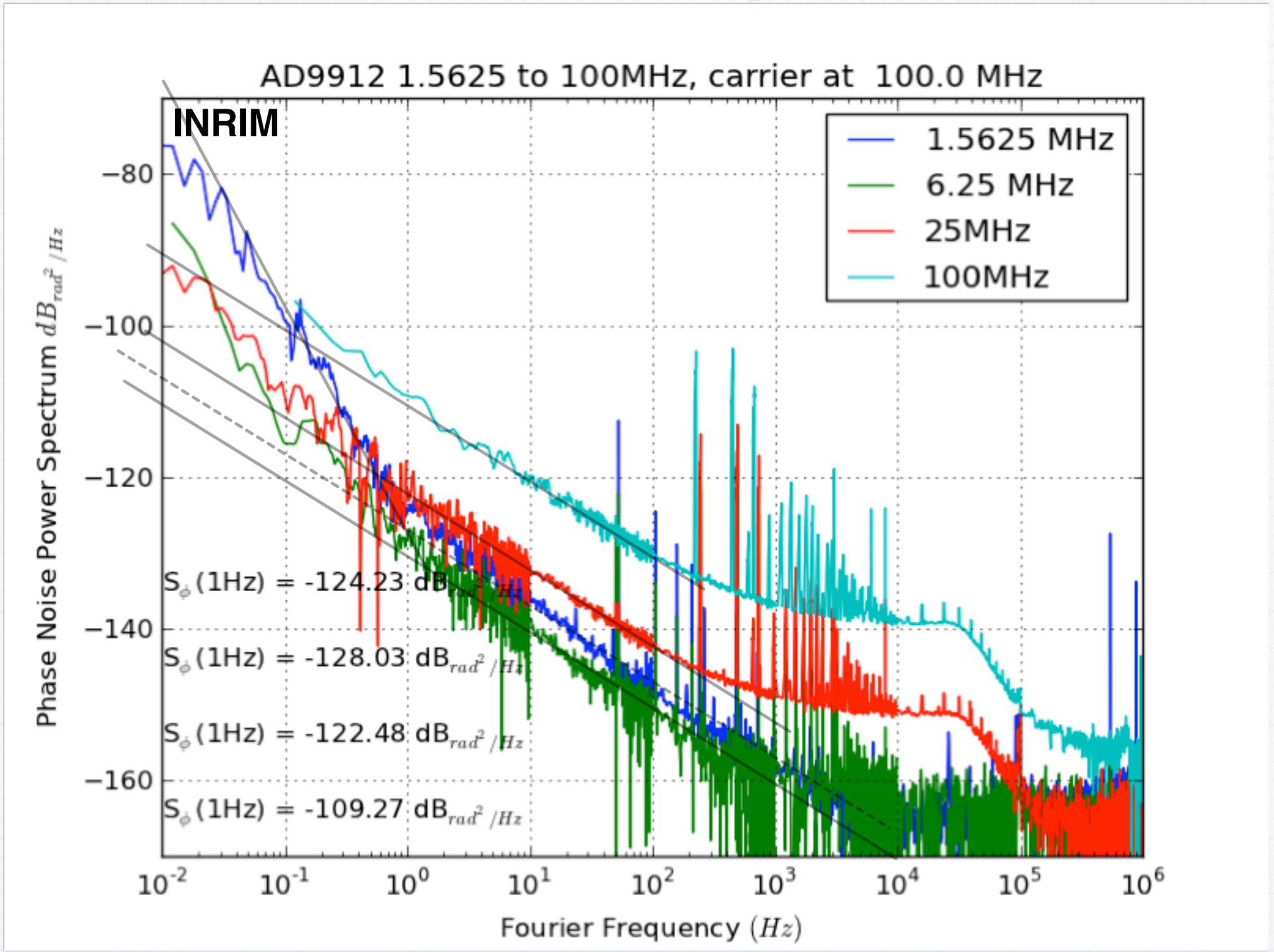


PM noise vs. output frequency

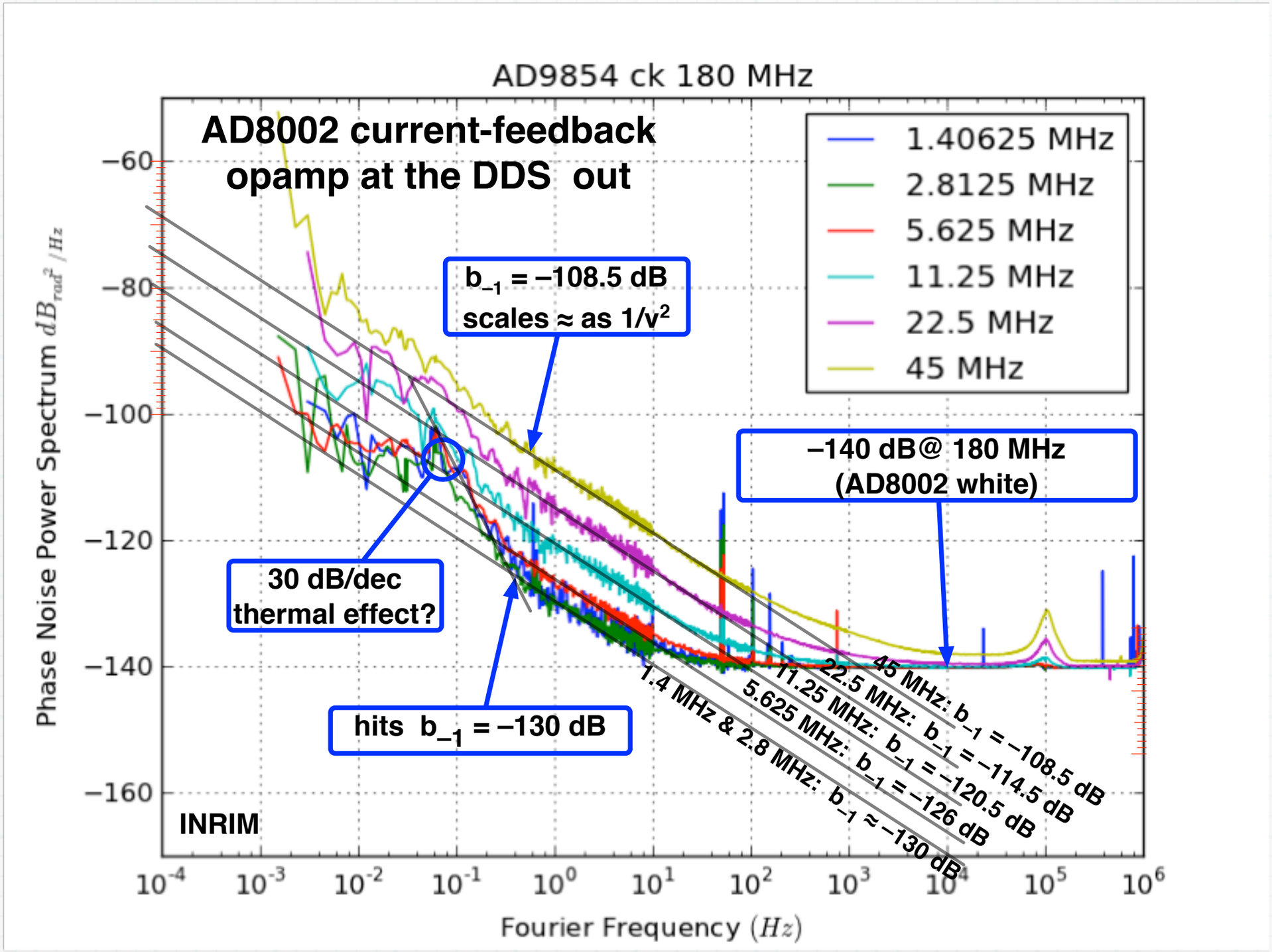


AD9912 noise vs. out frequency

– low Fourier frequencies –

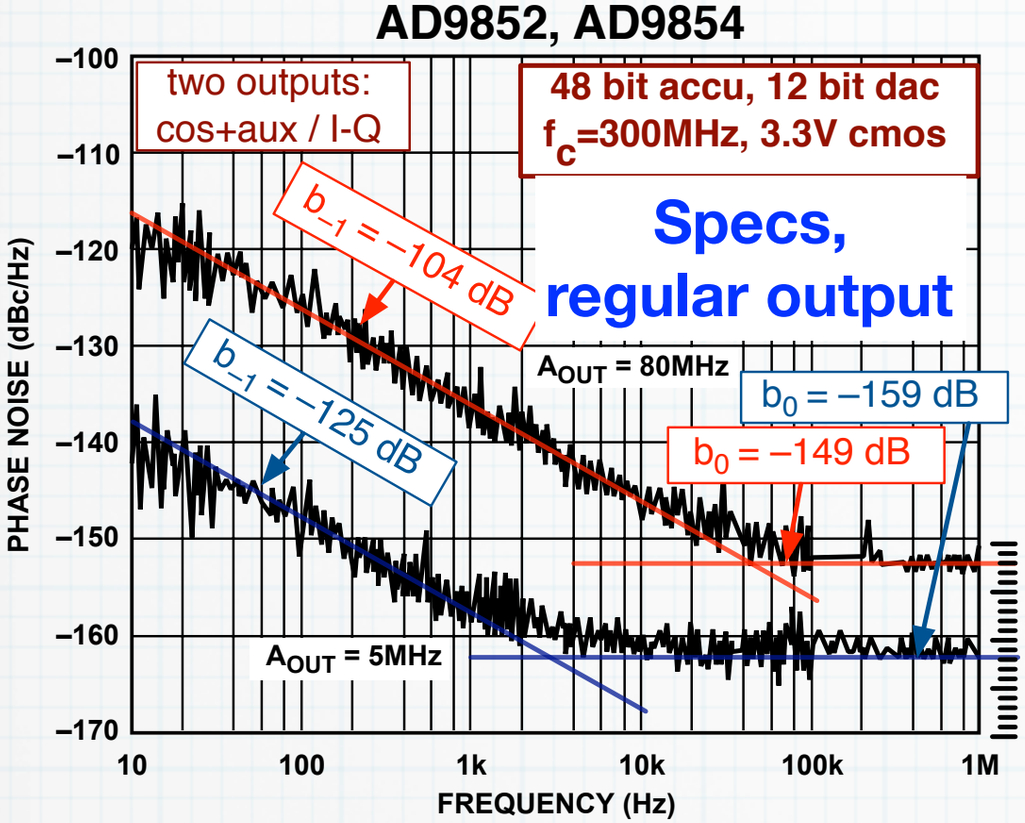


PM noise vs. output frequency



- The –140 dB floor is due to AD8002 at the DDS output
- The flicker is unchanged (comes from the DDS)

AD9854 noise



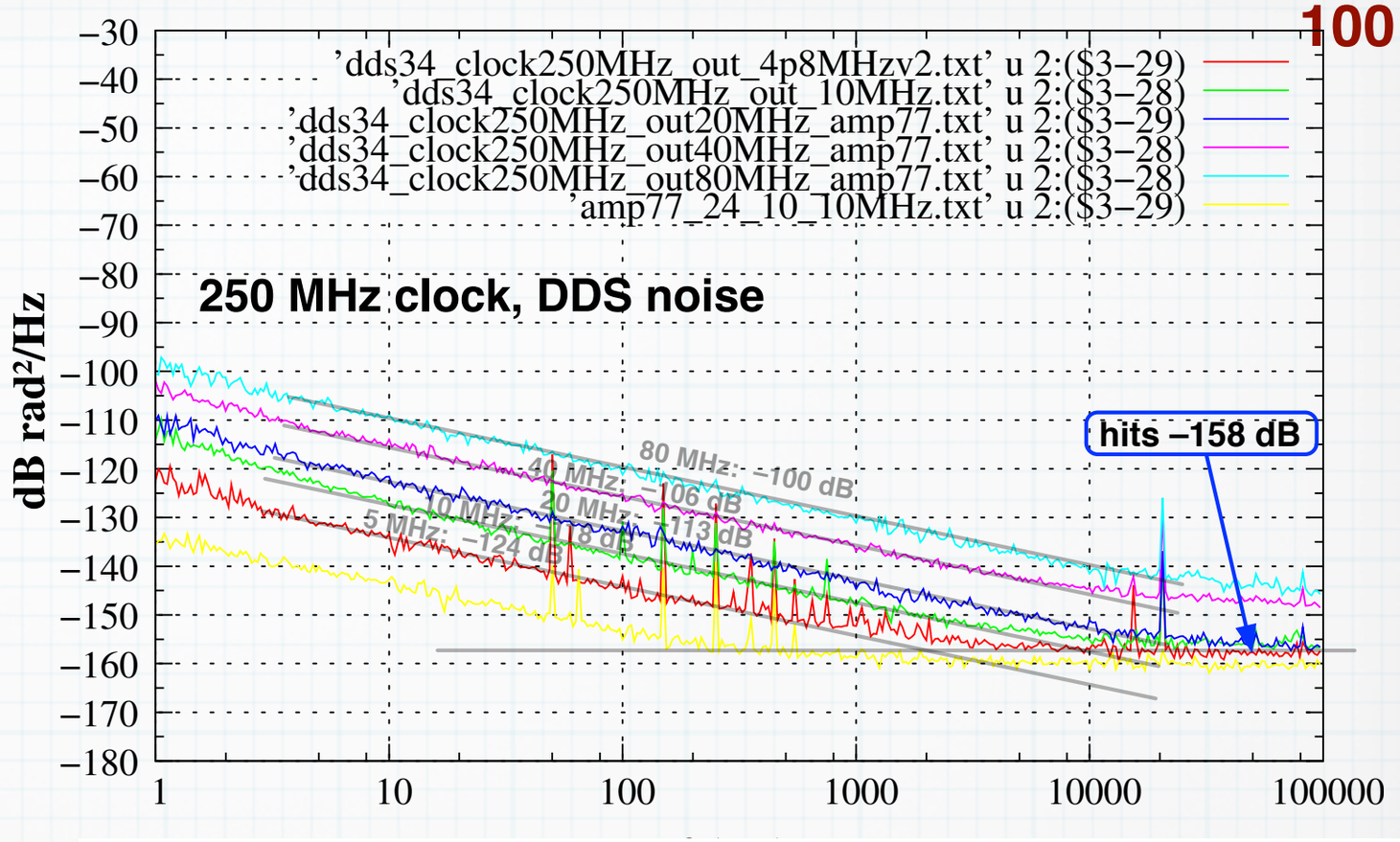
Flicker is in fair agreement

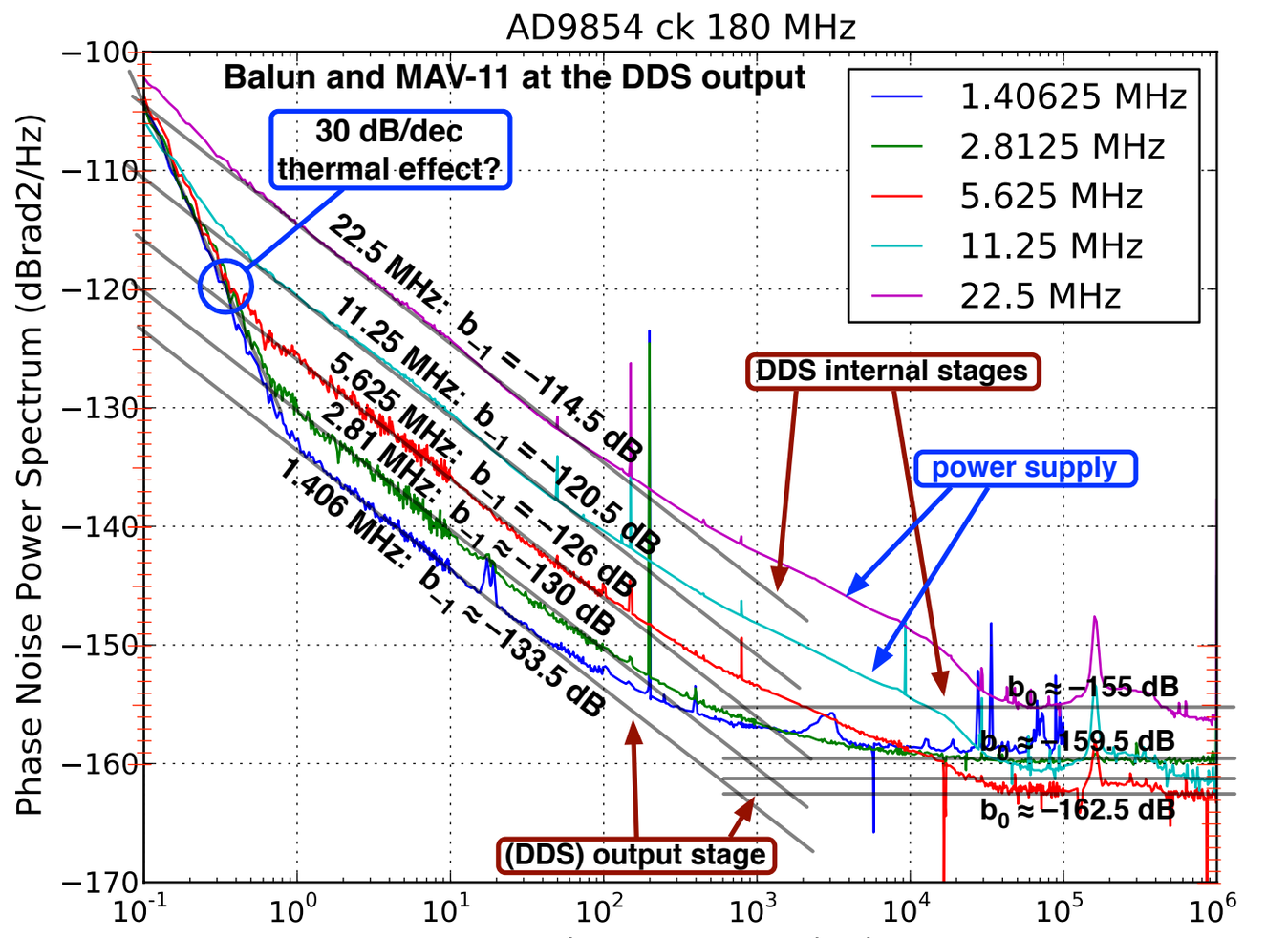
White is made low by spurs

Basic formula for white noise

$$b_0 = \frac{4}{3}\,\frac{1}{2^{2n}\,\nu_s} \quad \mathrm{rad}^2/\mathrm{Hz}$$

who	meas, dB	math, dB	clock, MHz
specs	–159	–155.8	300
YG	–158	–155.0	250
CC	–162.5	–153.6	180

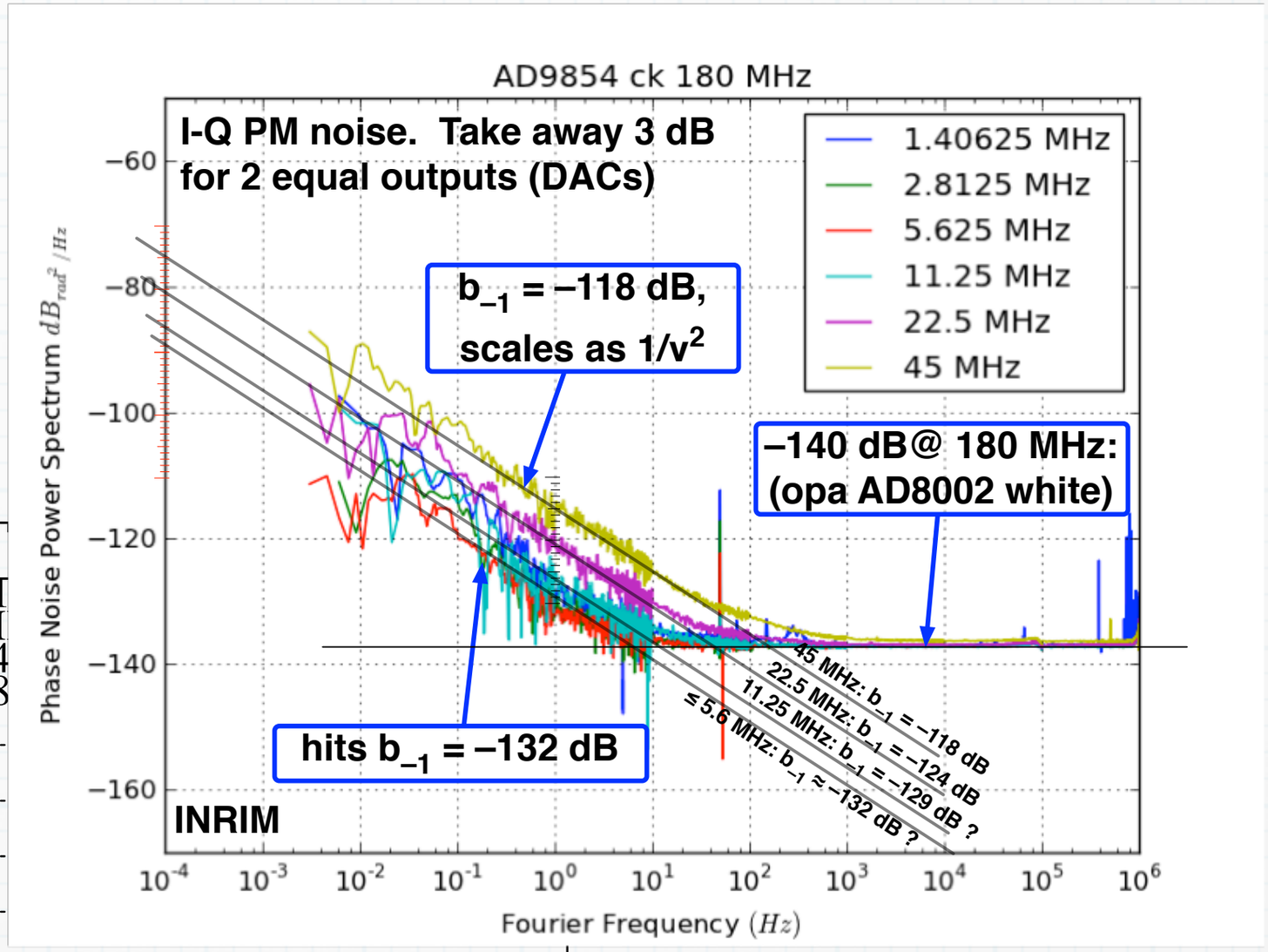


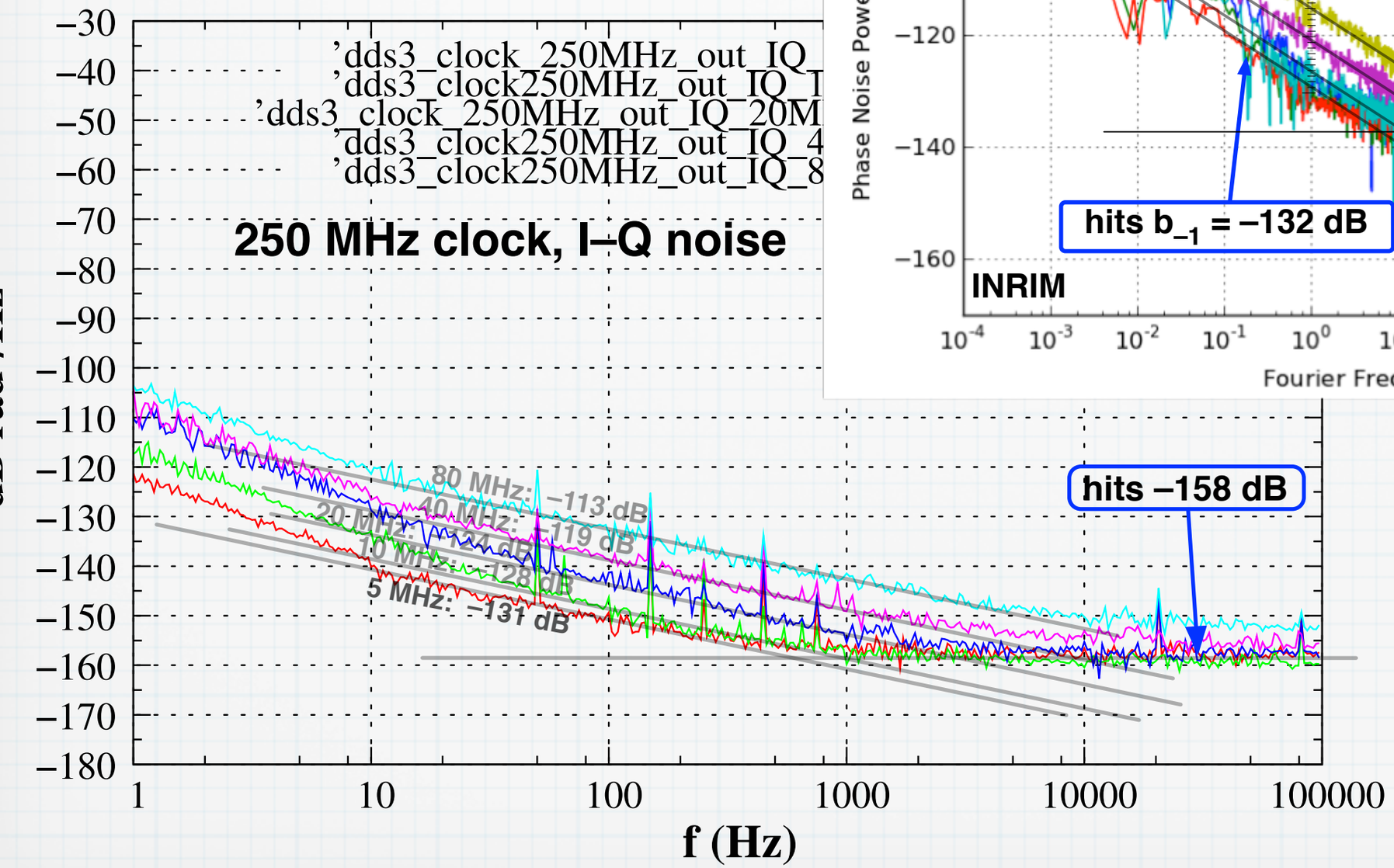


AD9854 I–Q noise

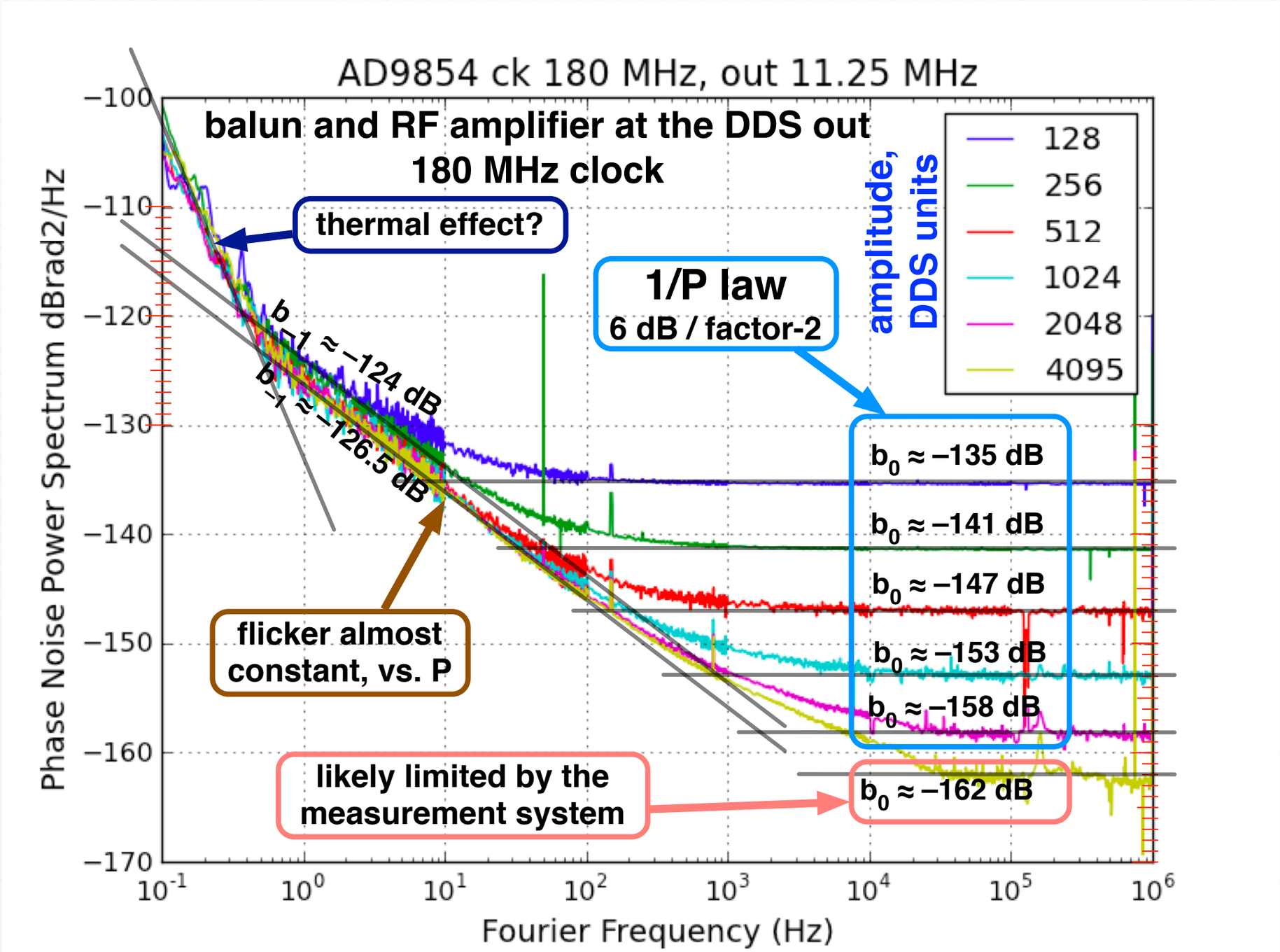
Flicker is in quite a good agreement between YG and CC

I–Q spectra cannot be compared to specs





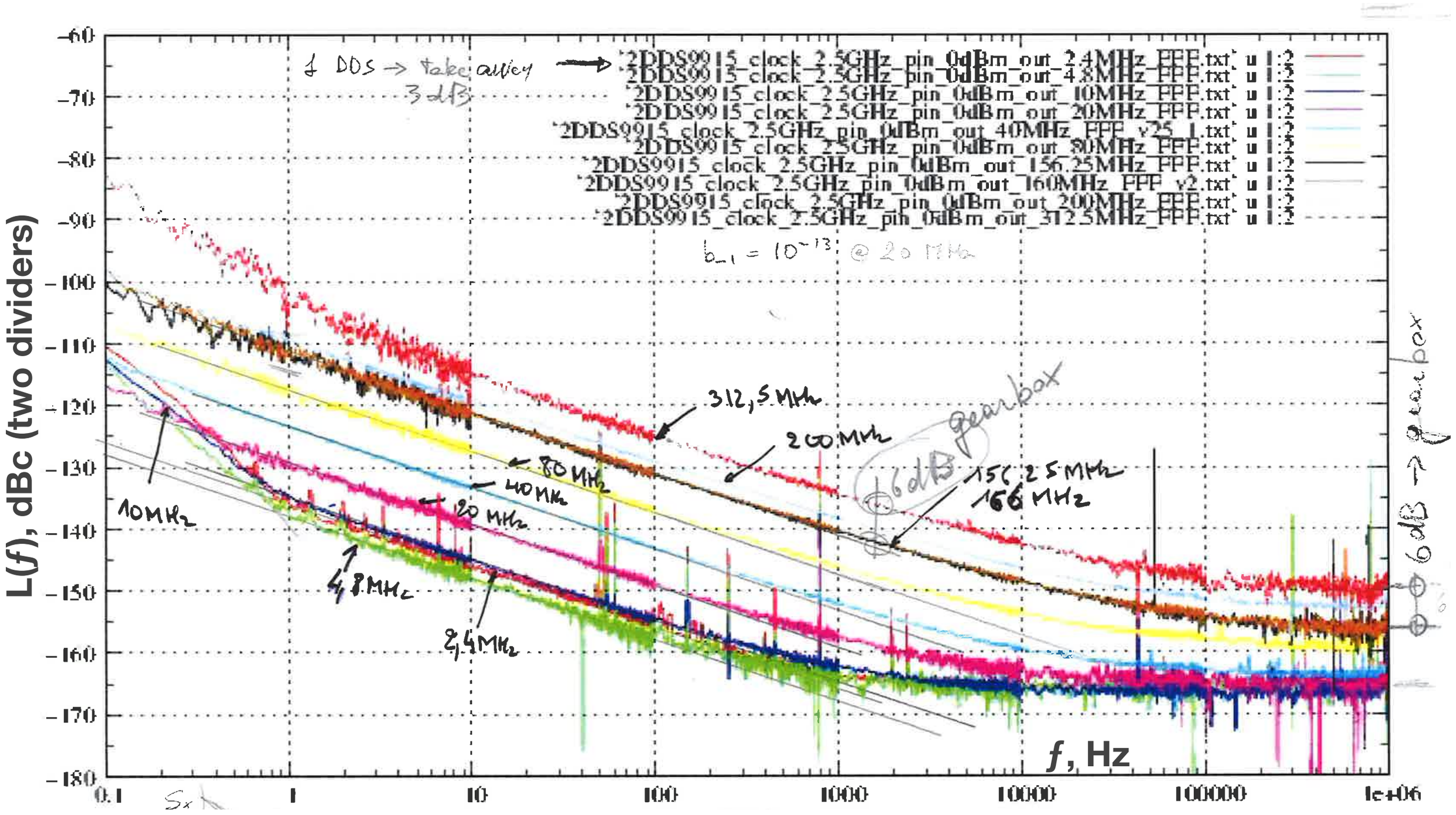
PM noise vs. output amplitude



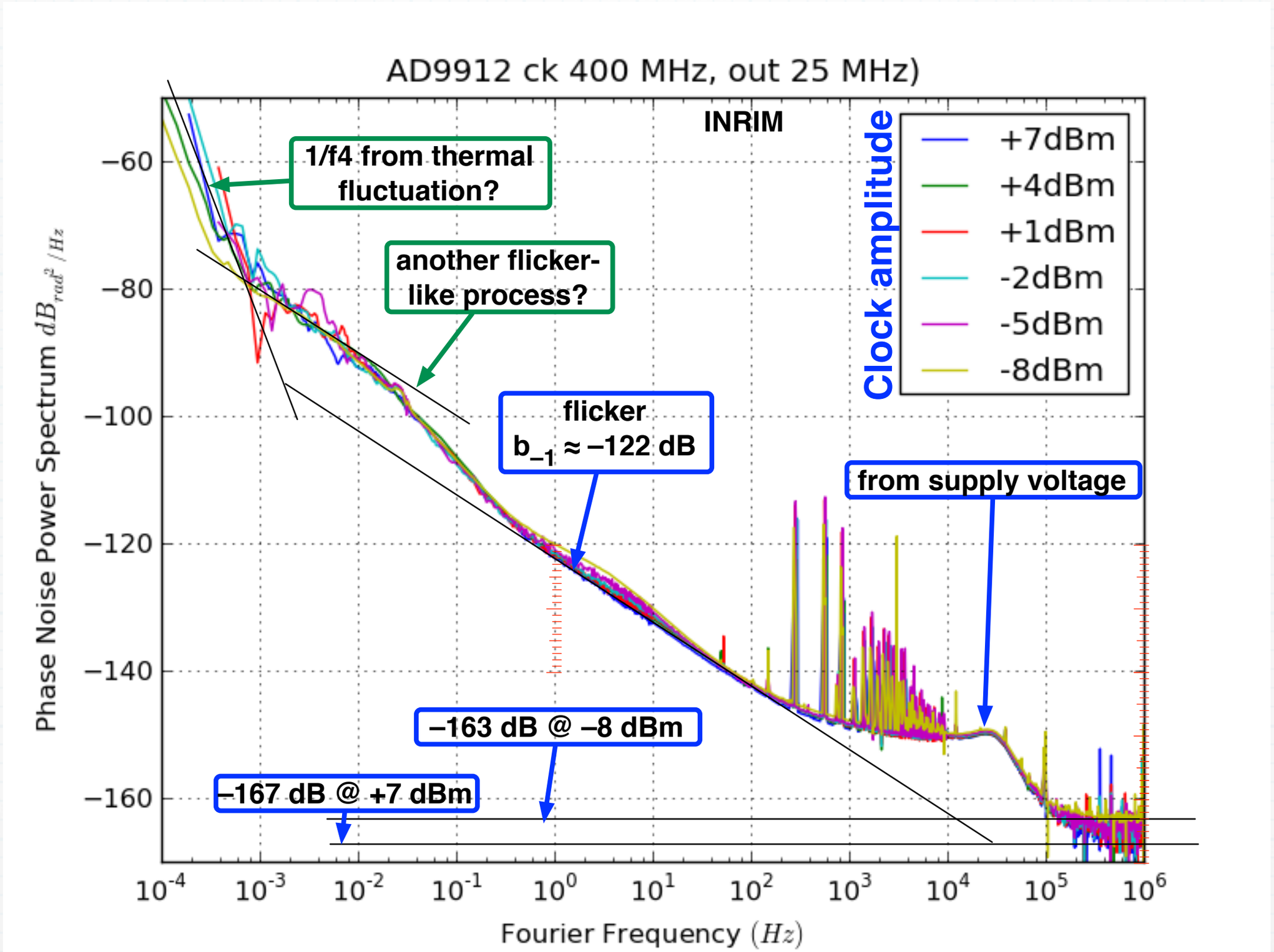
- PM noise scales 6 dB per factor-of-two output amplitude
- Signature of digital multiplication: lower amplitude is obtained by reducing the integer number at the DAC input

High-frequency DDSs

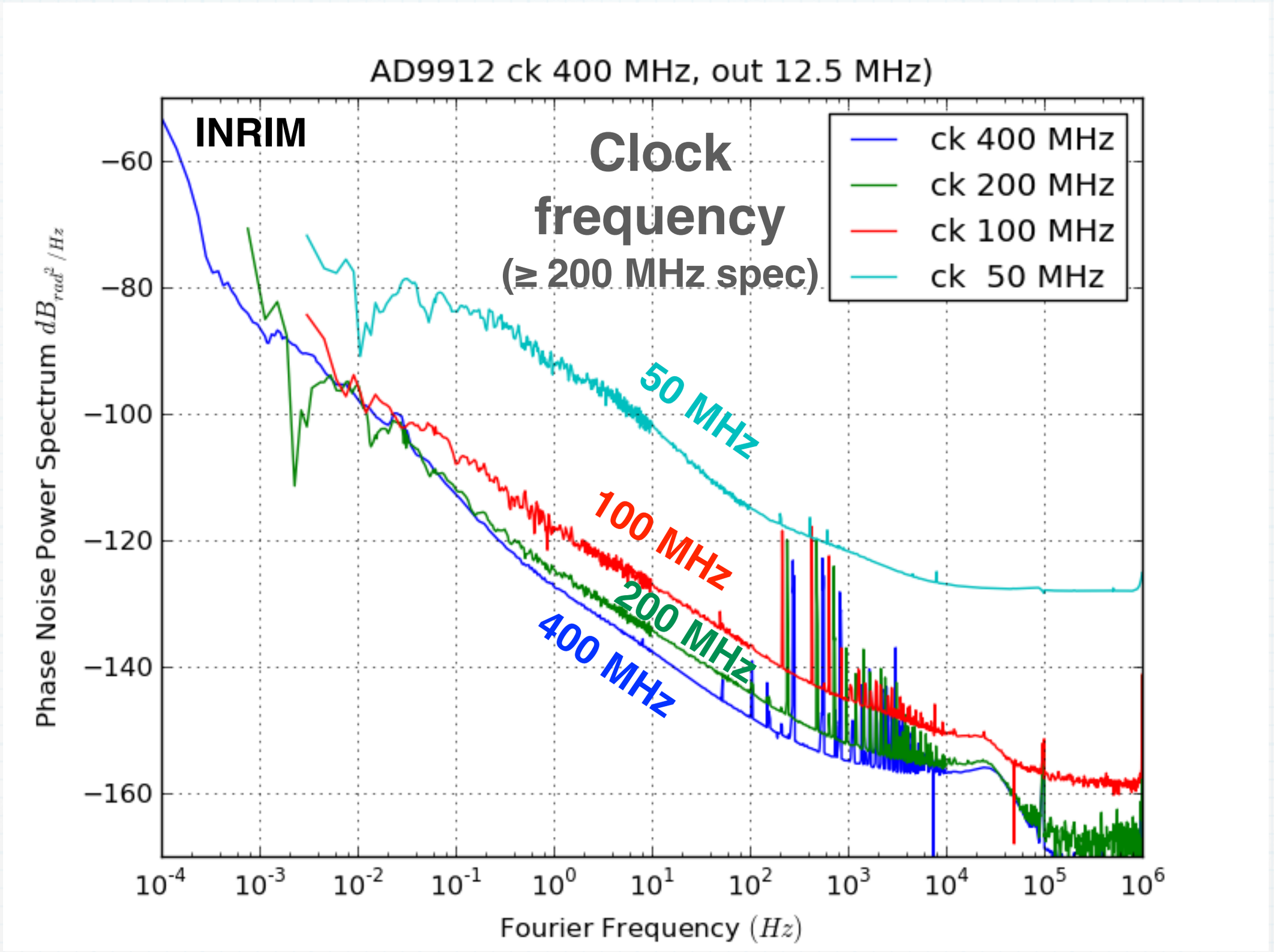
AD9915 12 bit, 2.5 GHz
64 bit accumulator (135 pHz res)



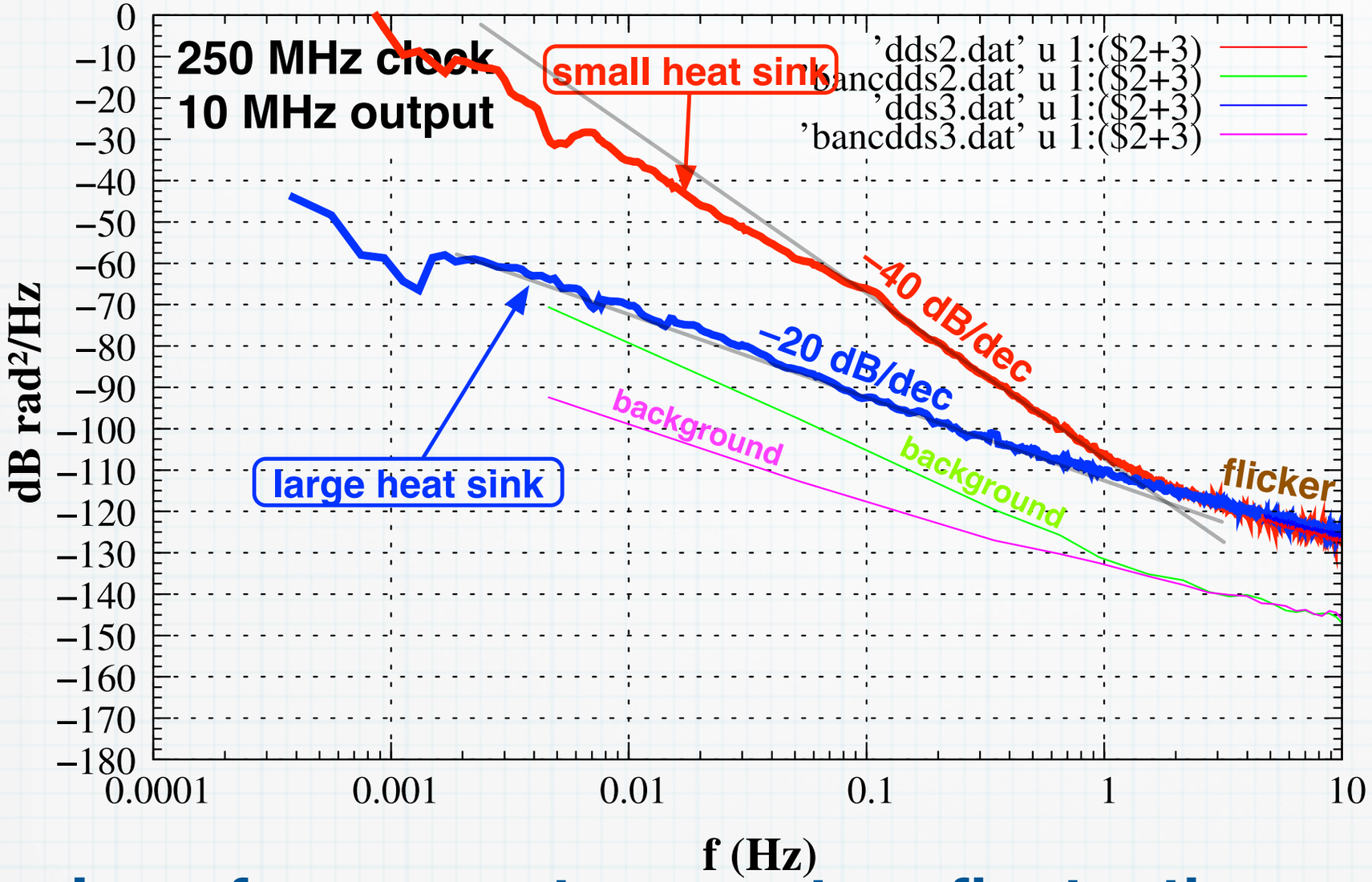
PM noise vs. clock amplitude



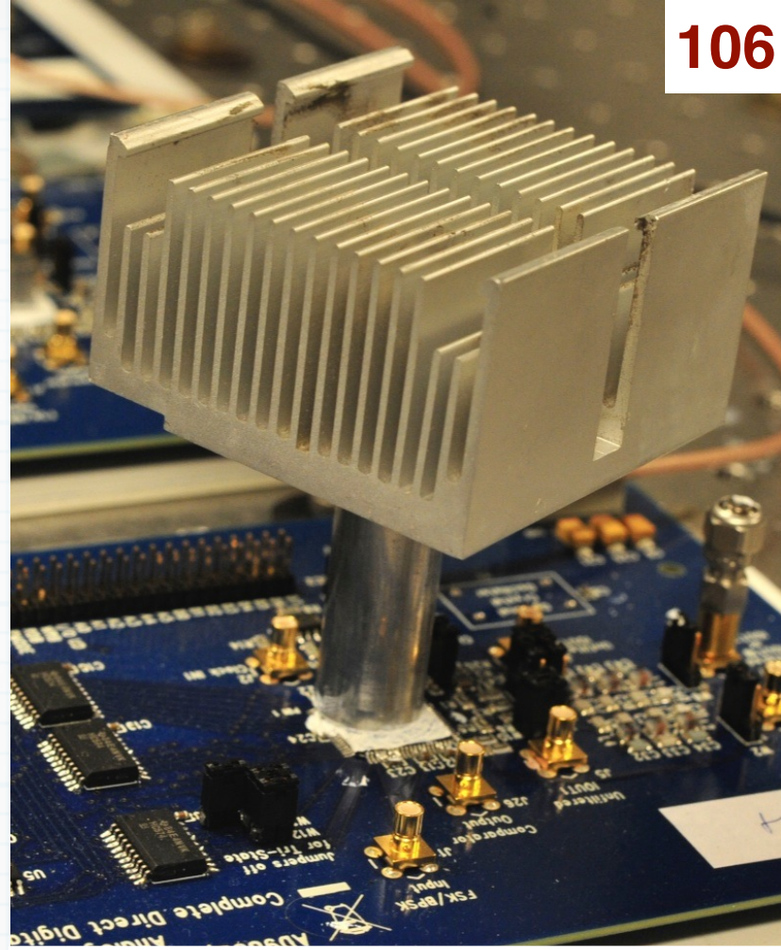
The effect of the clock frequency

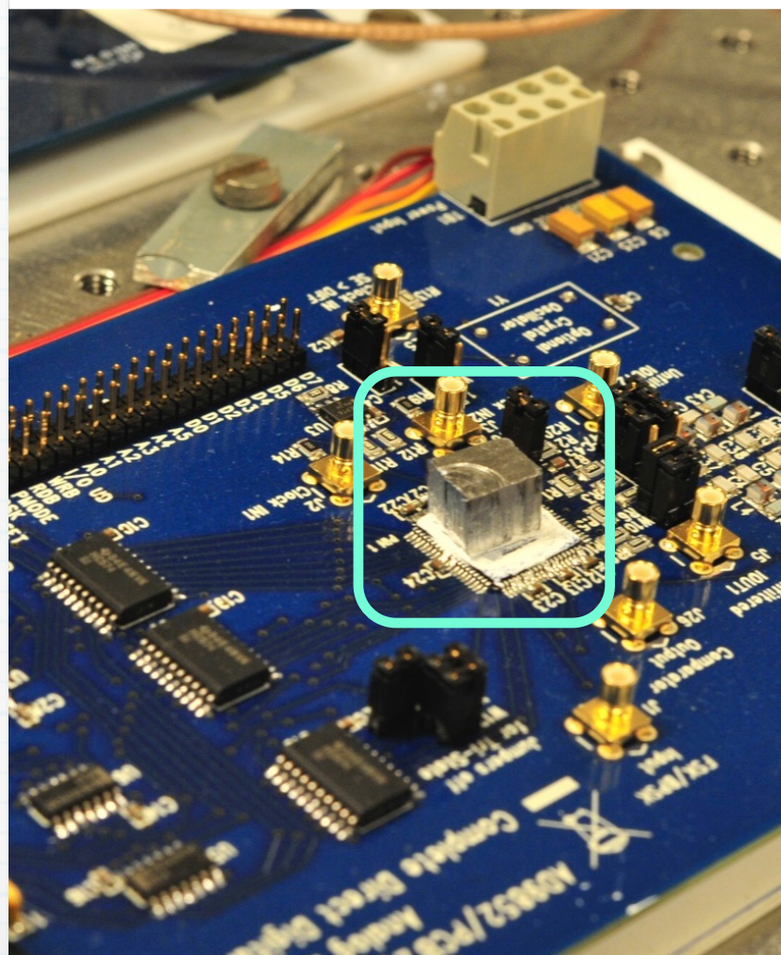


Thermal effects

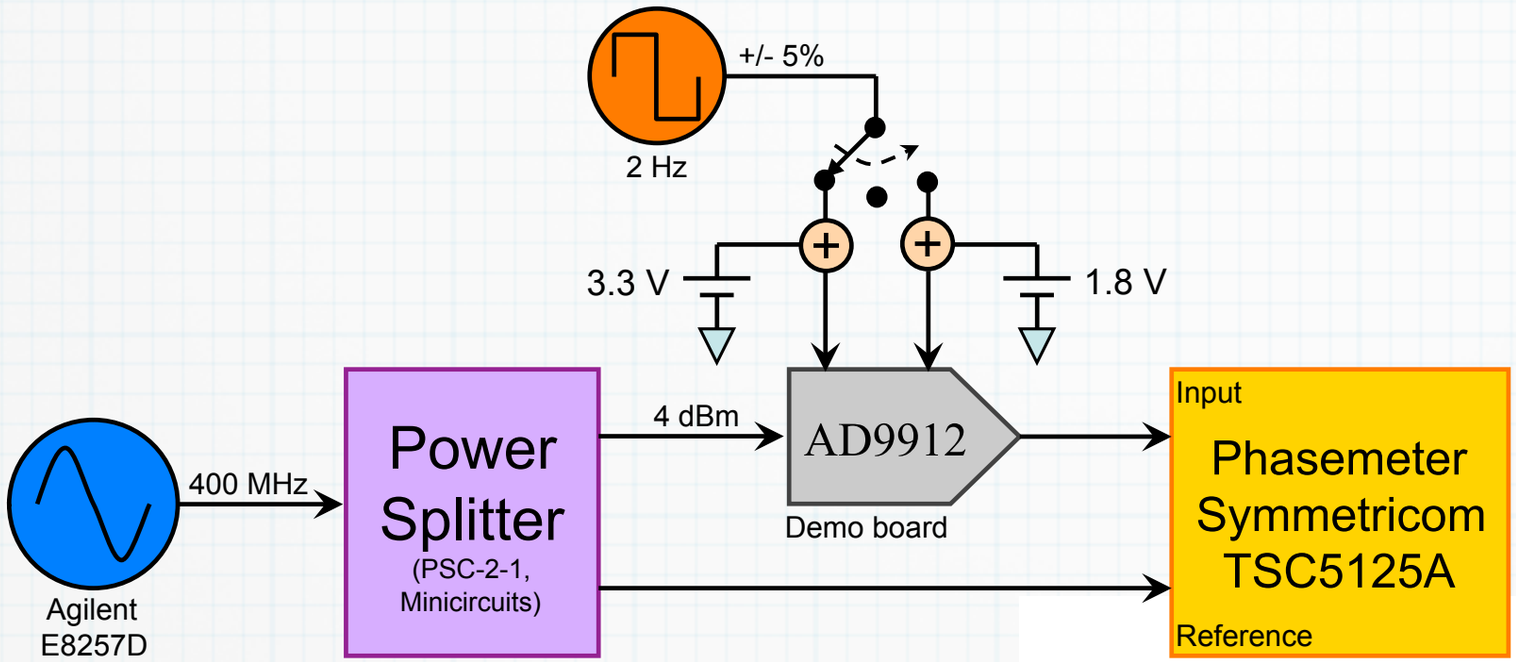


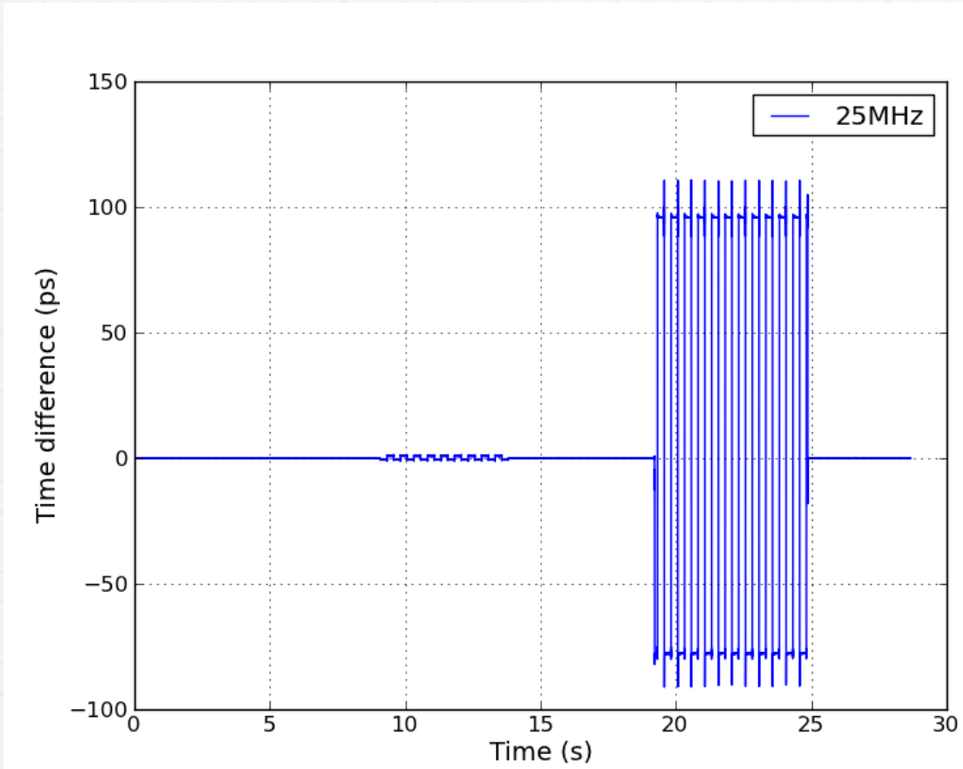
- Low-frequency temperature fluctuations induce phase noise
- A large thermal mass helps

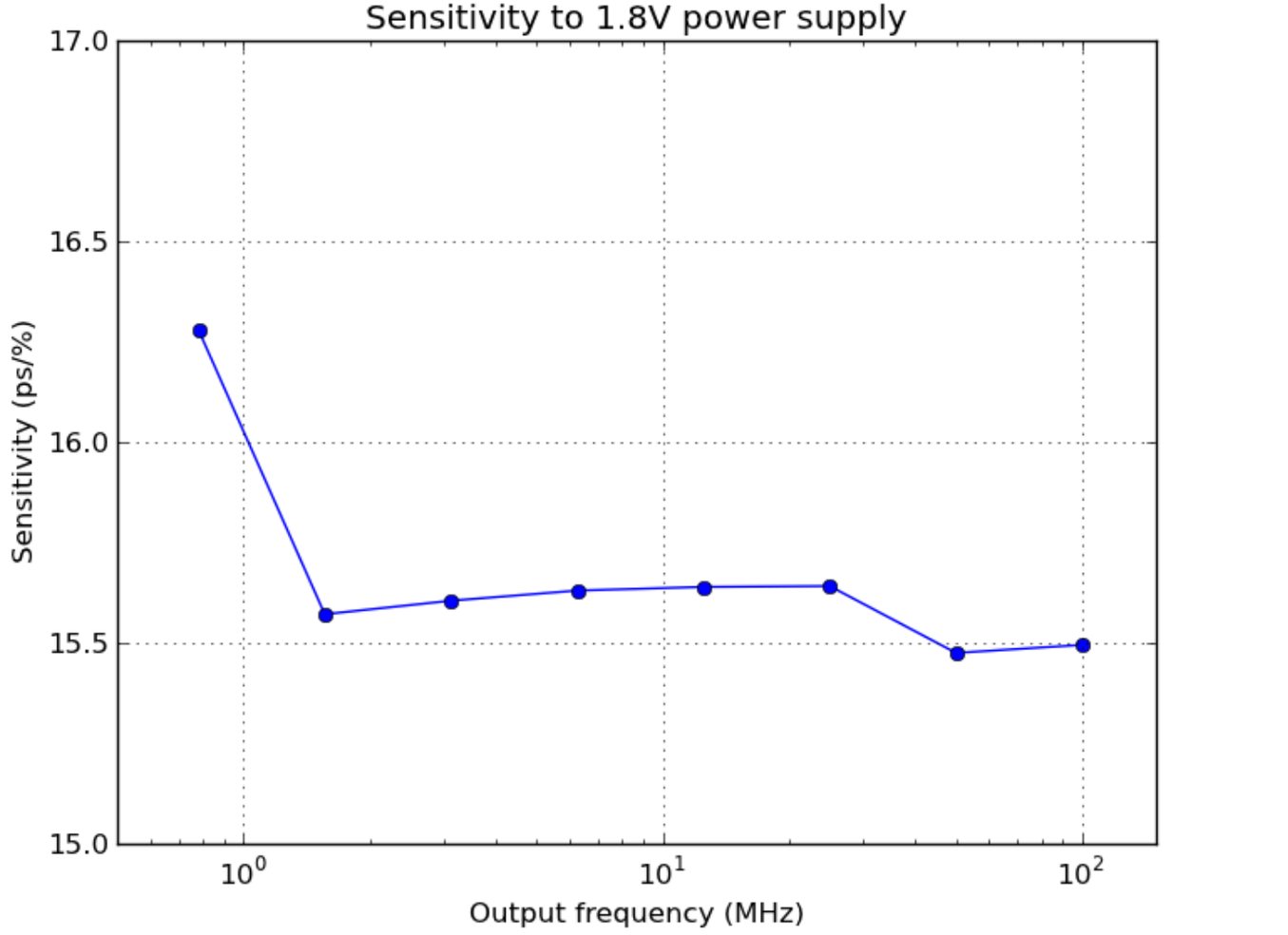




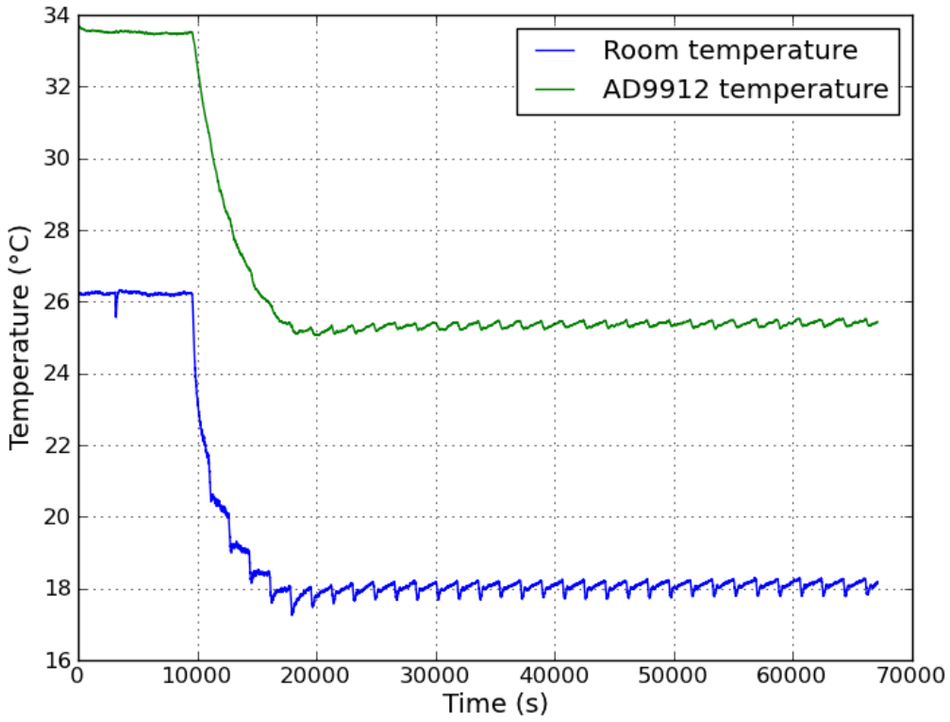
AD9912 Voltage sensitivity

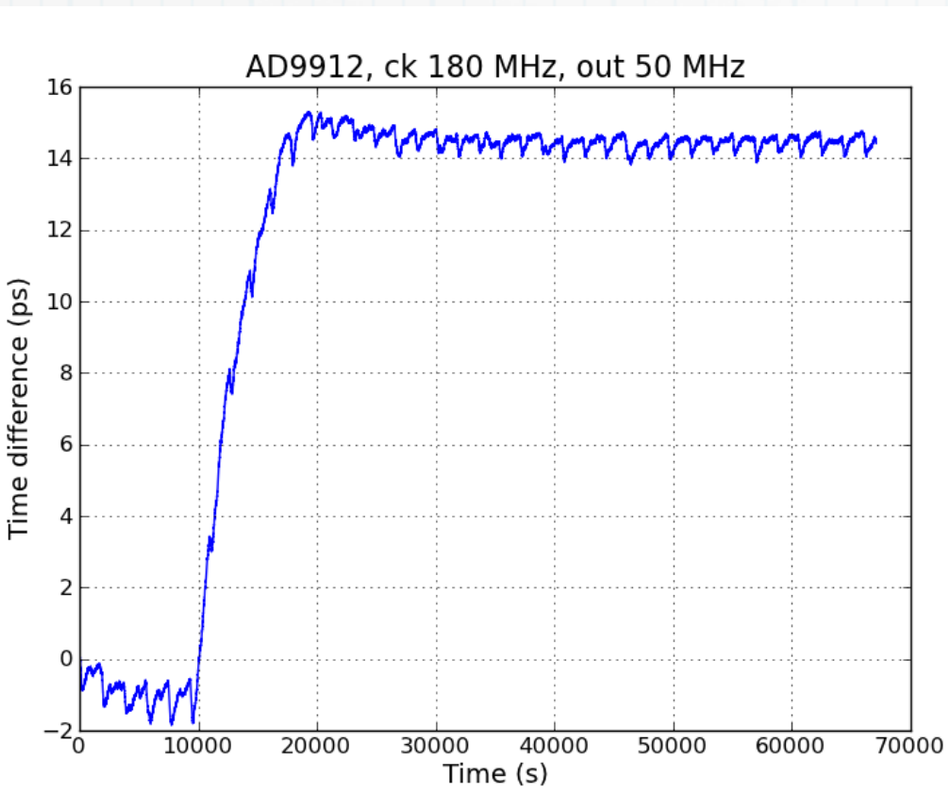






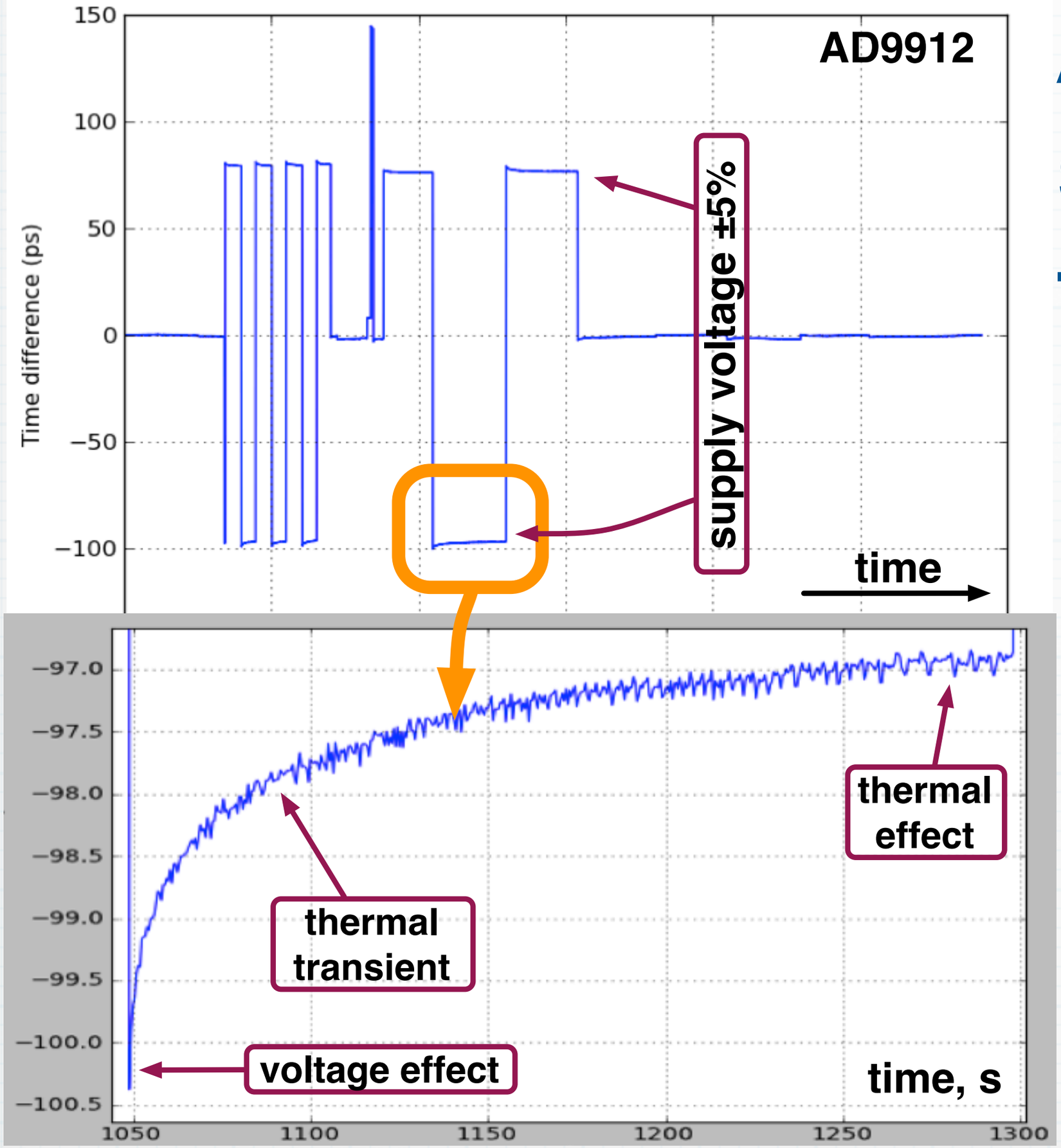
AD9912 temperature sensitivity



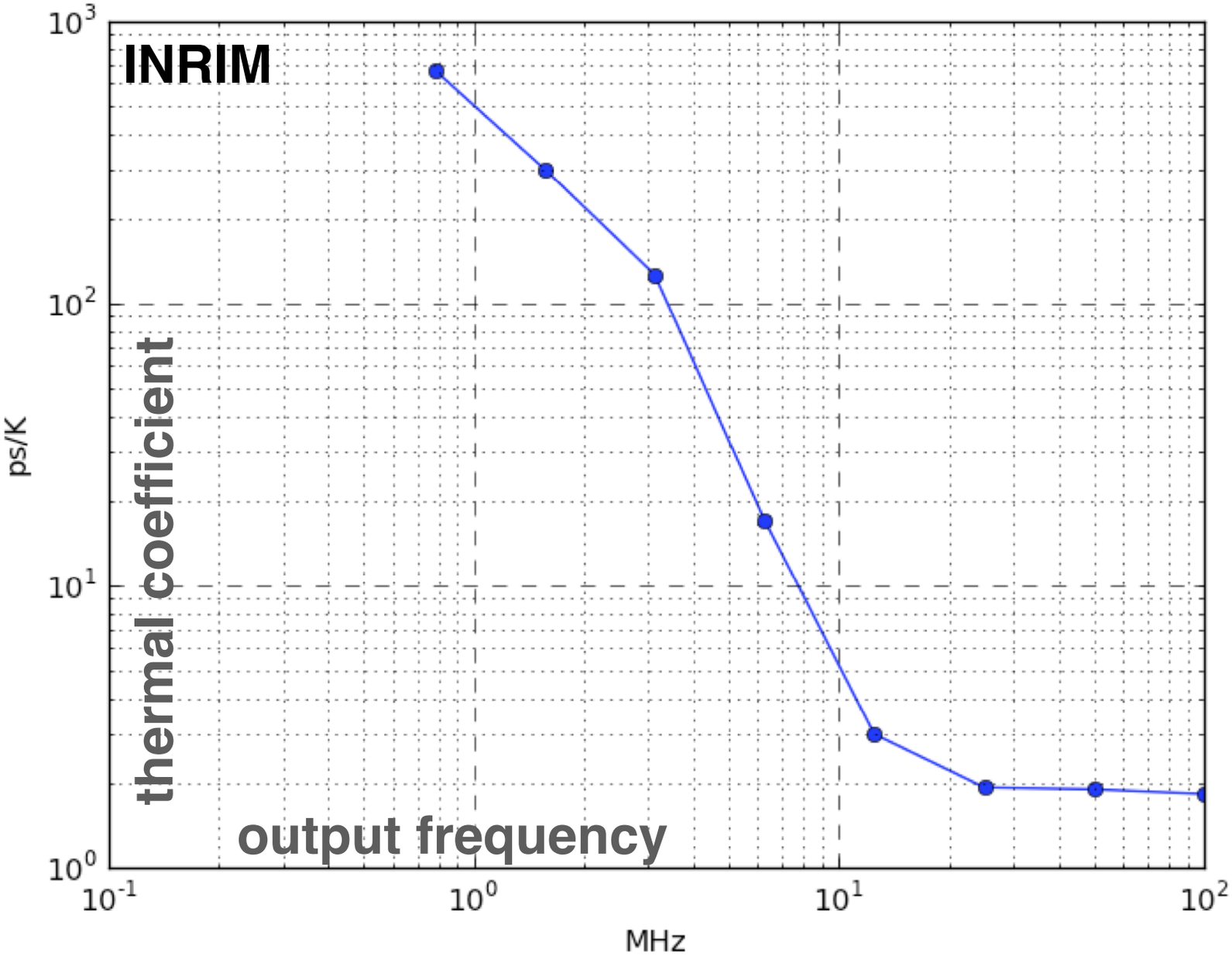


- Temperature control (chamber)
- Measured: –2 ps/K
- Includes cables, baluns etc

AD9912 sensitivity to temperature (alternate)



AD9912 temperature sensitivity



- **High frequency: –2 ps/K, constant**
- **Low frequency: $1/\nu^3$ law**

PM noise of the AD 9912

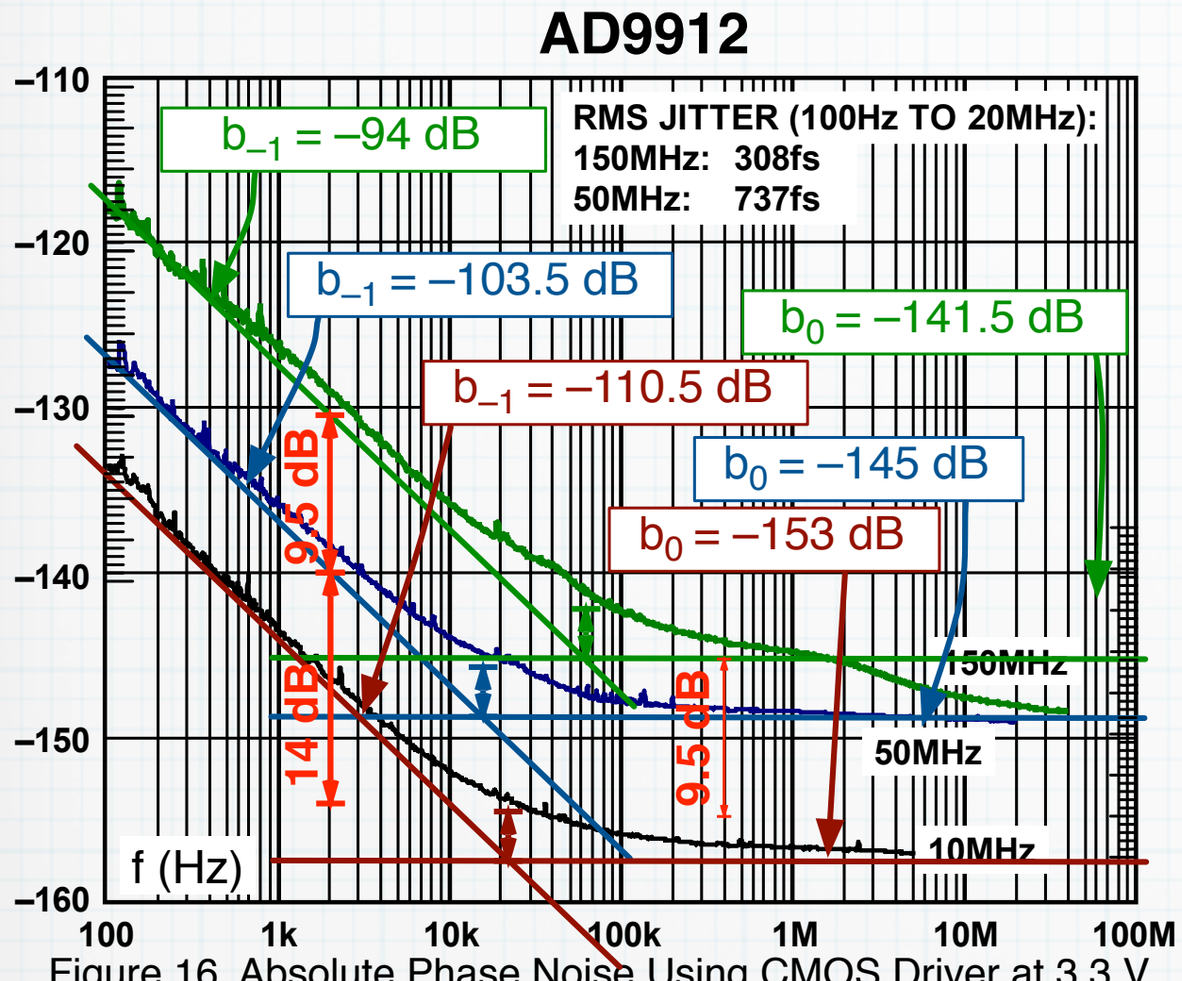
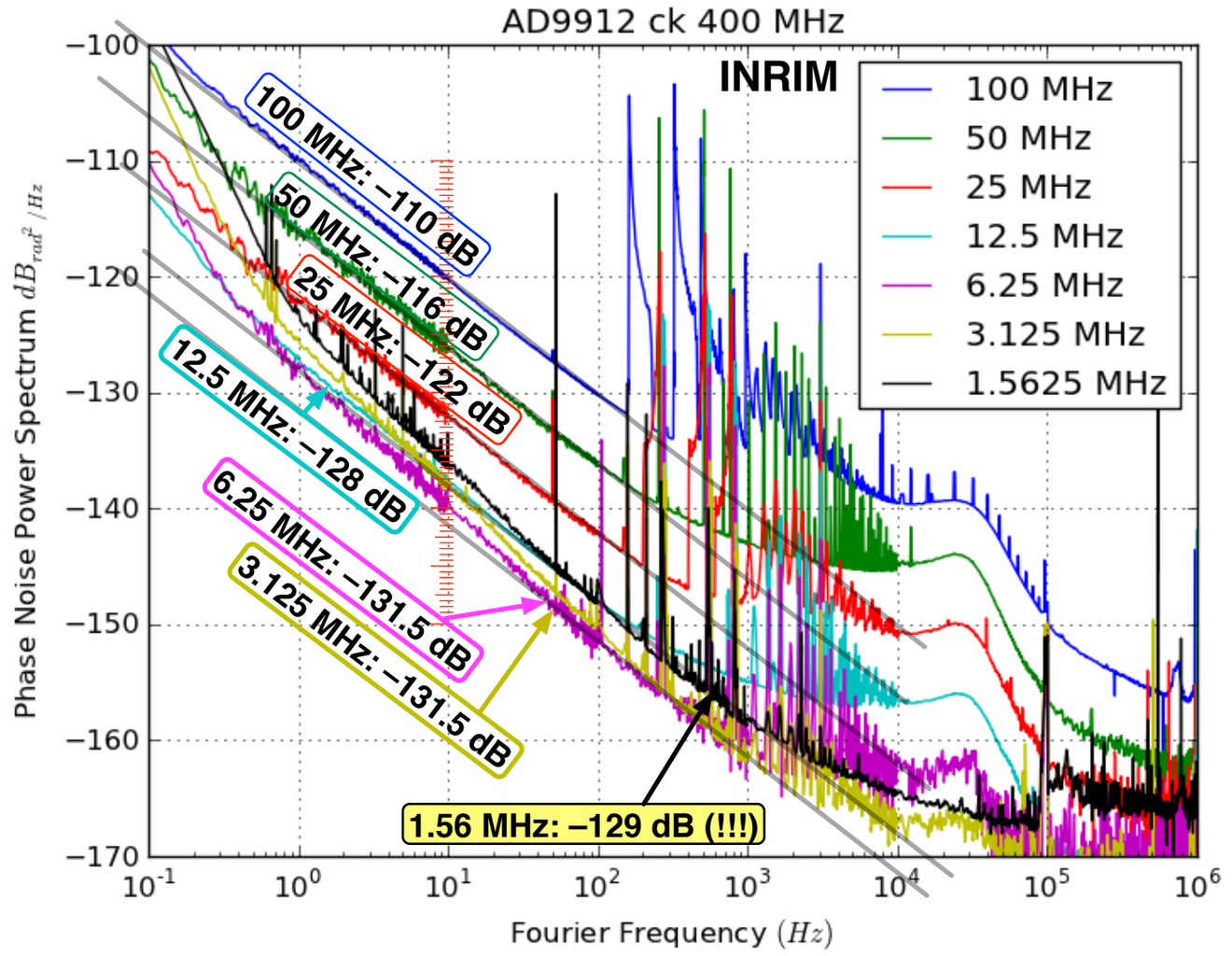
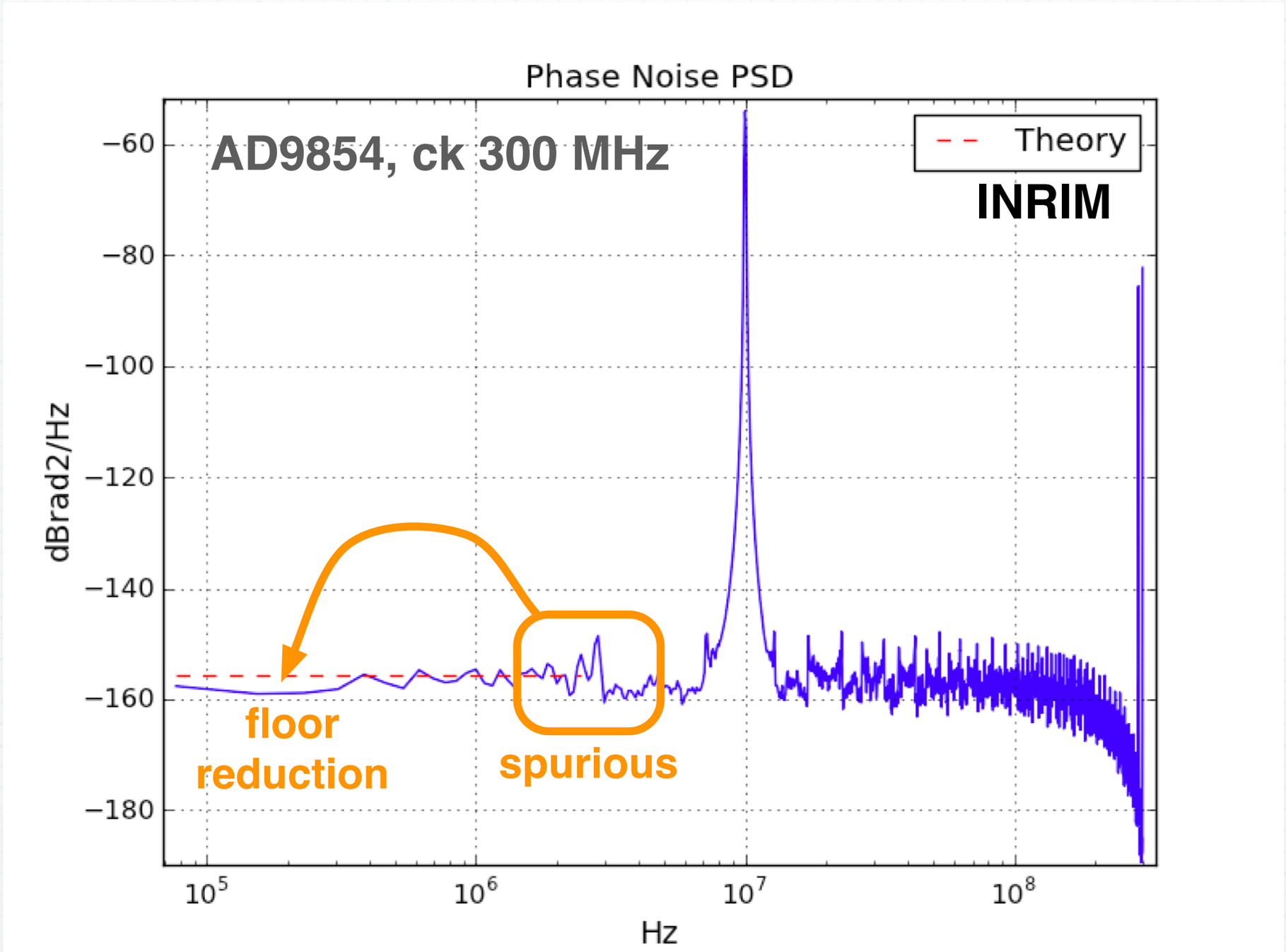


Figure 16. Absolute Phase Noise Using CMOS Driver at 3.3 V, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed) DDS Run at 200 MSPS for 10 MHz

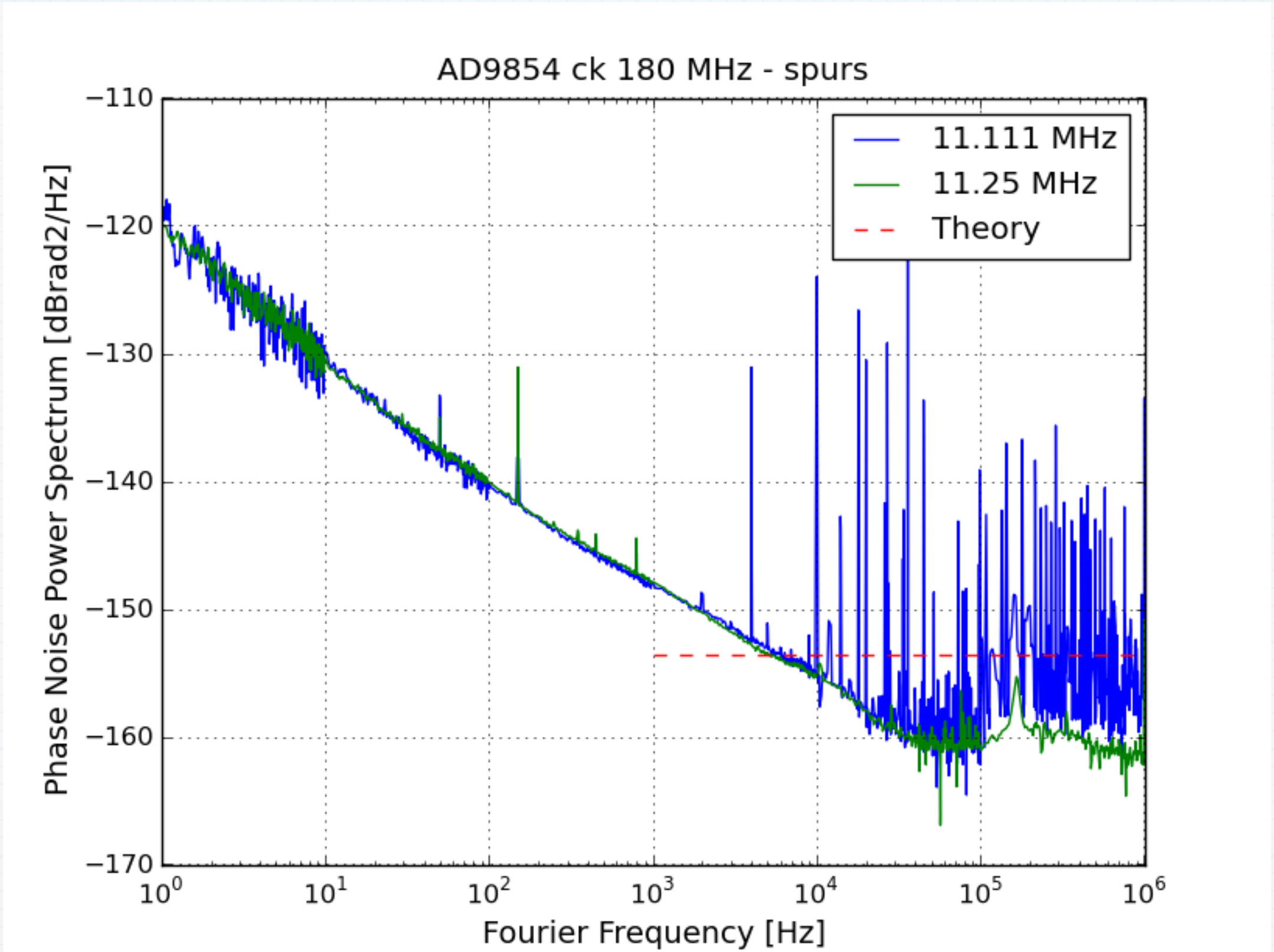


- **At 50 MHz and 10/12.5 MHz we get ≈15 dB lower flicker than the data-sheet spectrum**
- **Experimental conditions unclear in the data sheets**

Spurs reduce the white noise

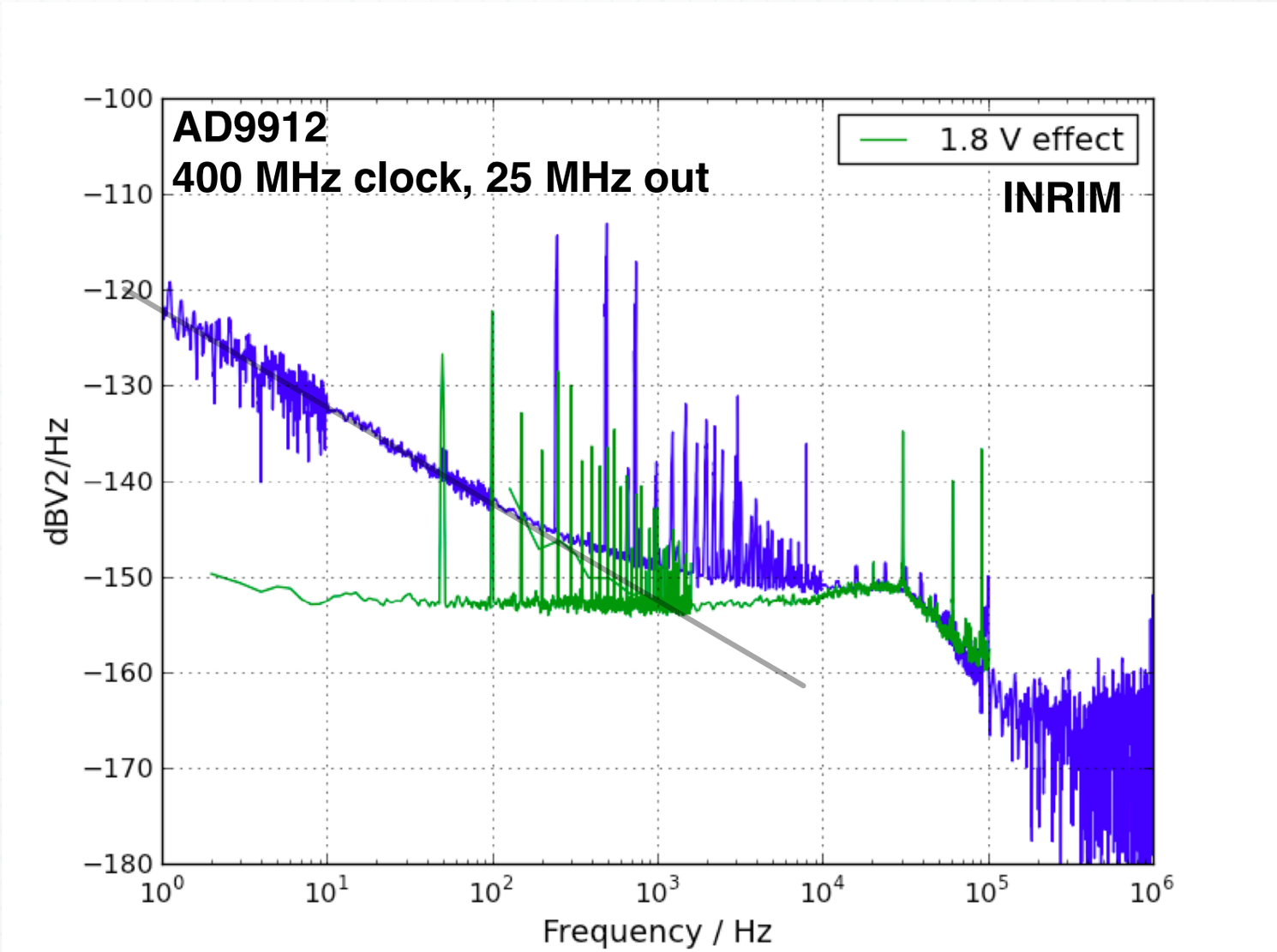


Spurs can be amazing



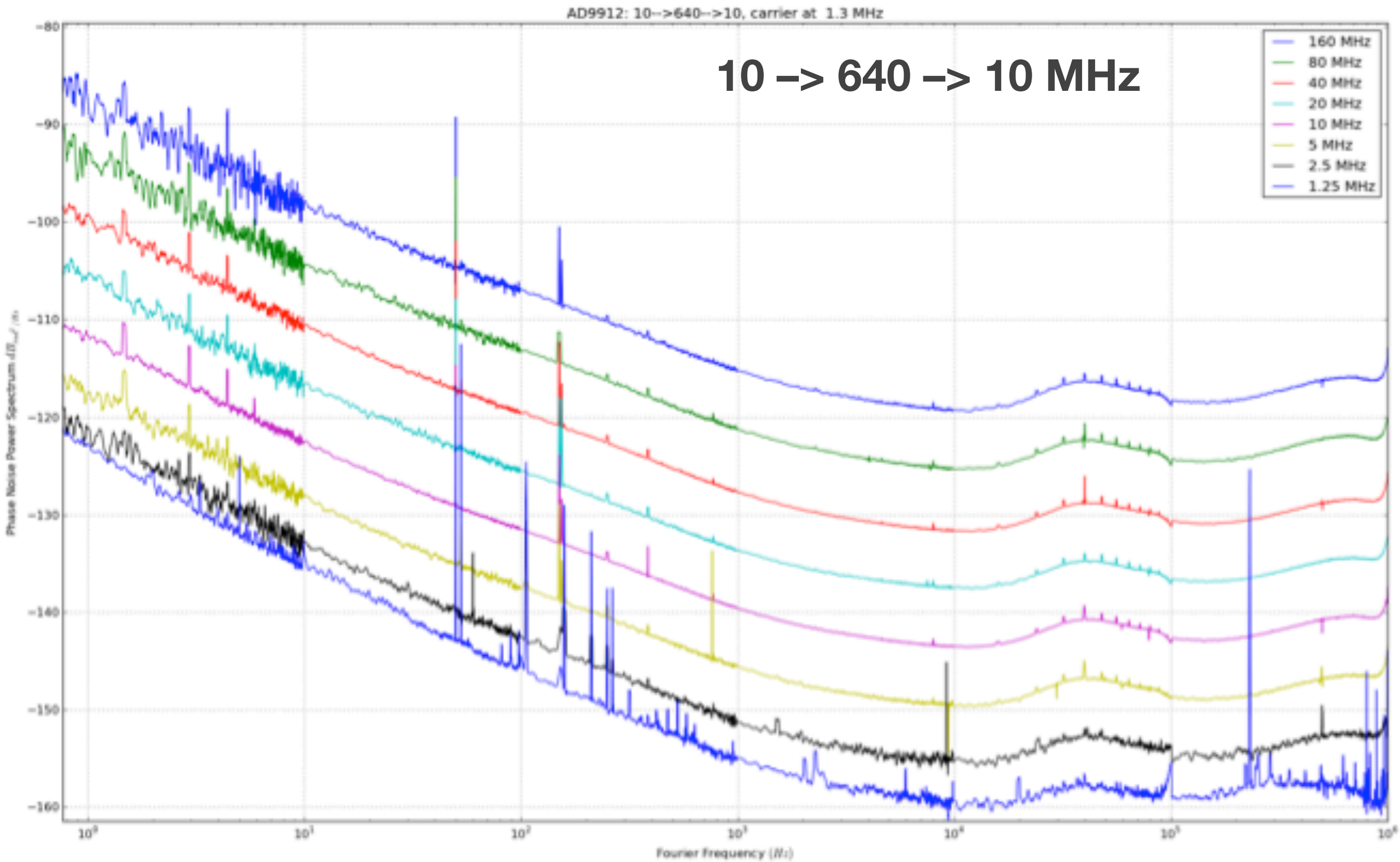
More about a PM-noise bump

- Low PSRR (power-supply rejection ratio) of PM noise
- For instance The AD9912 at 25 MHz out has 15 ps/% supply-voltage sensitivity
- No bump at 10^3–10^5 Hz is seen in the data-sheet spectra
- DC regulator may show a similar bump, alone or or with the output capacitor

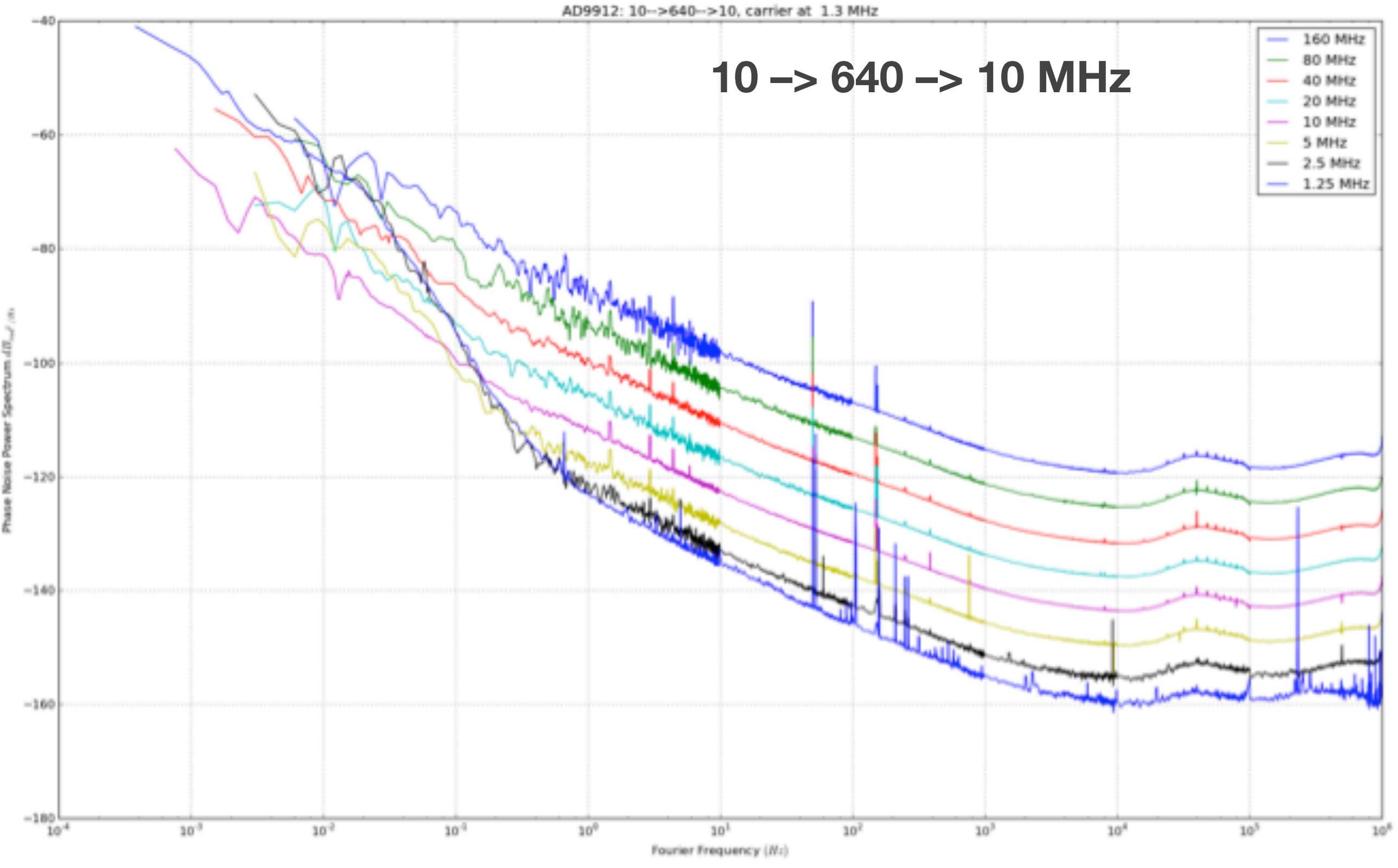


X7R SMD capacitor shows low ESR (≤5 mΩ)

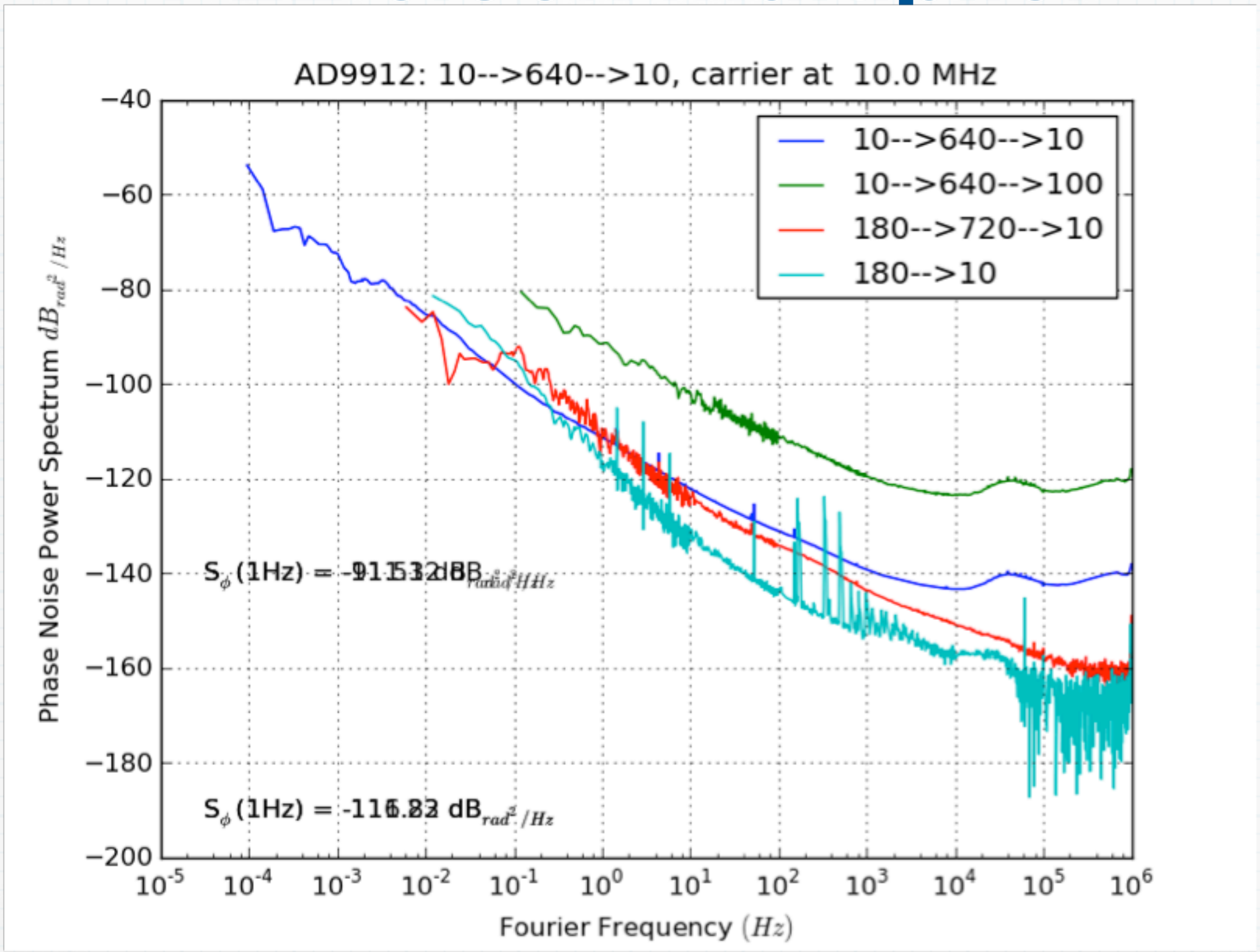
PLL clock multiplier



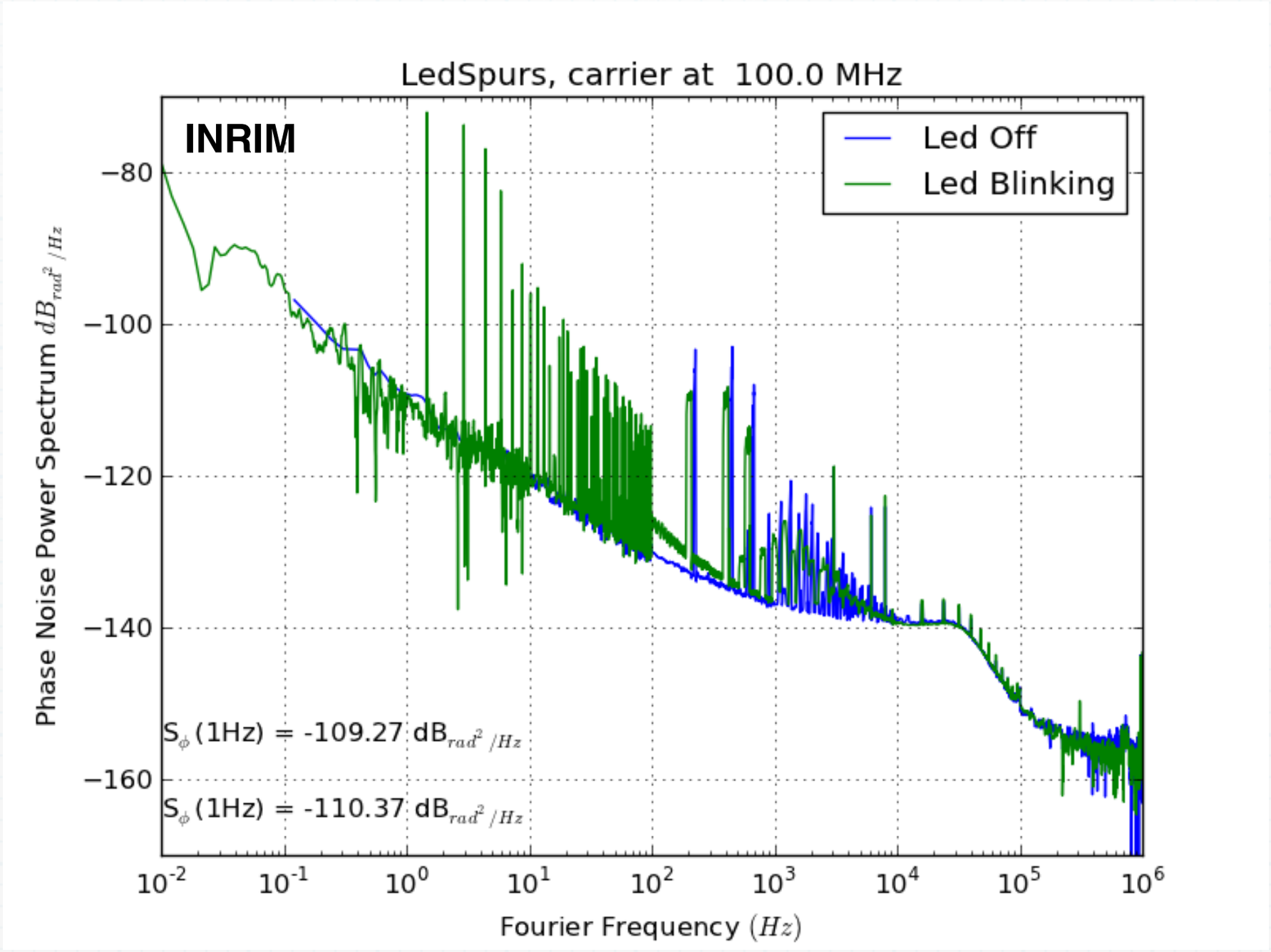
PLL clock multiplier



PLL clock multiplier

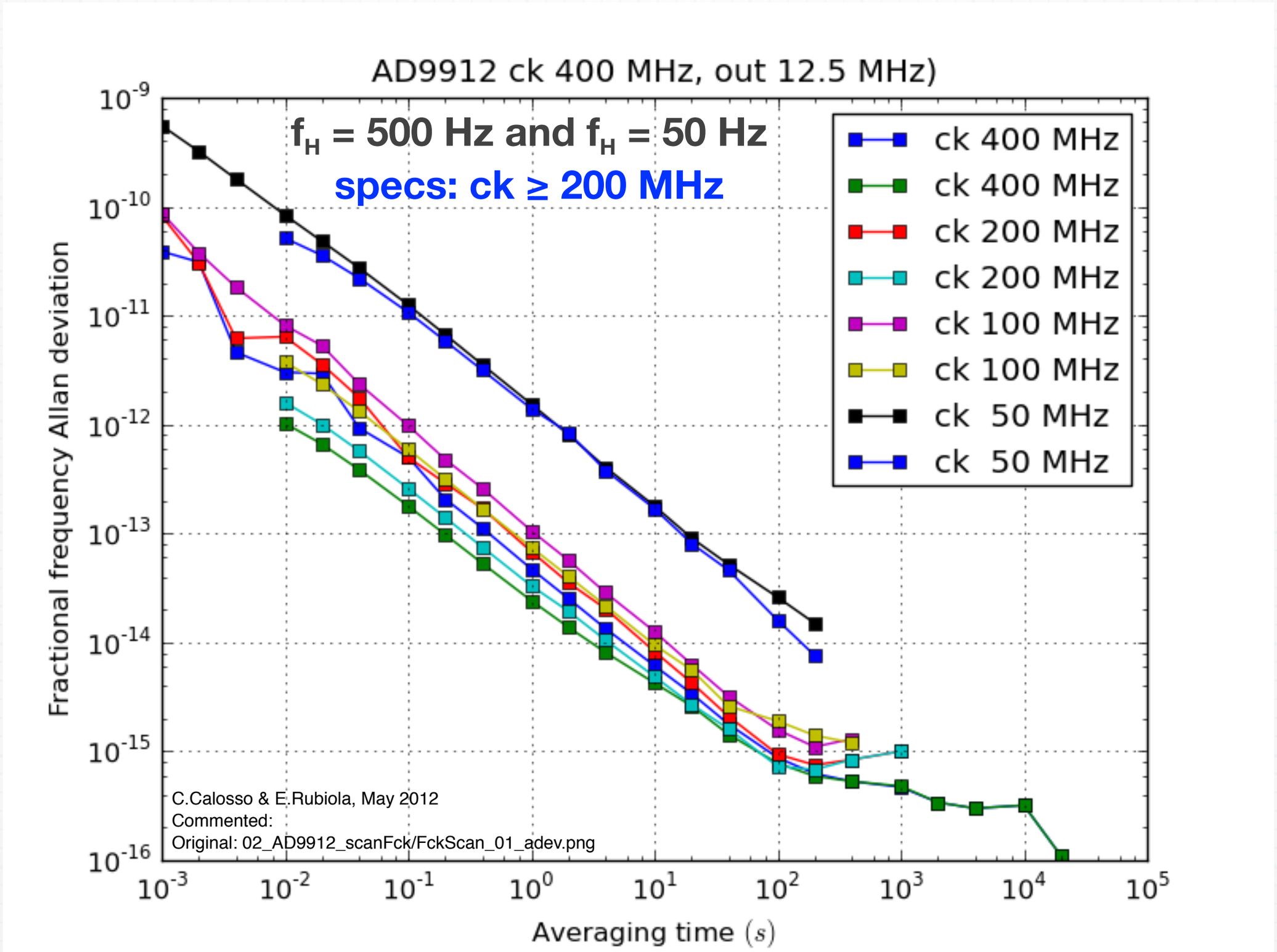


Effect of other parts on the PCB

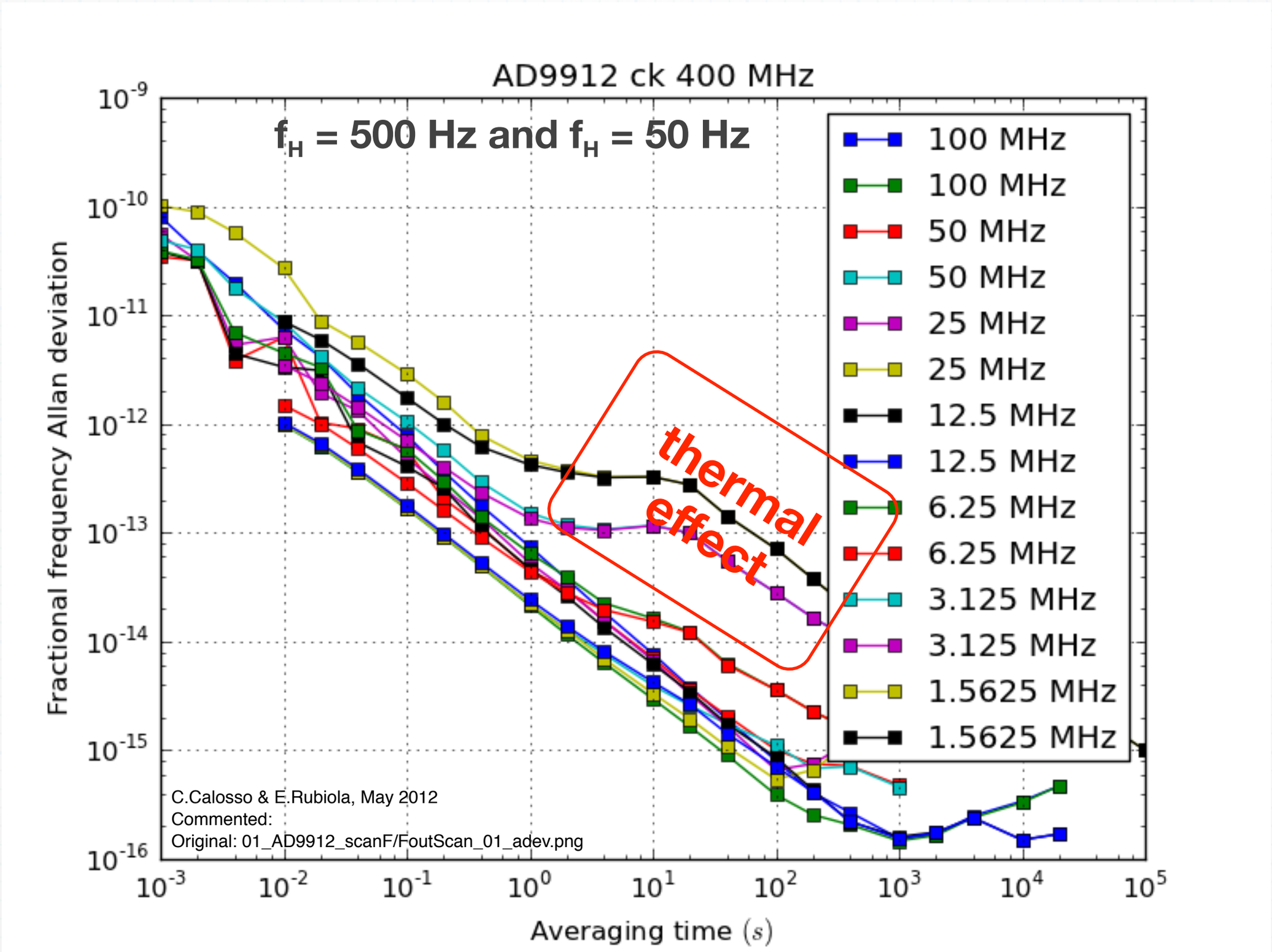


A blinking LED somewhere on the PCB spoils the output spectrum

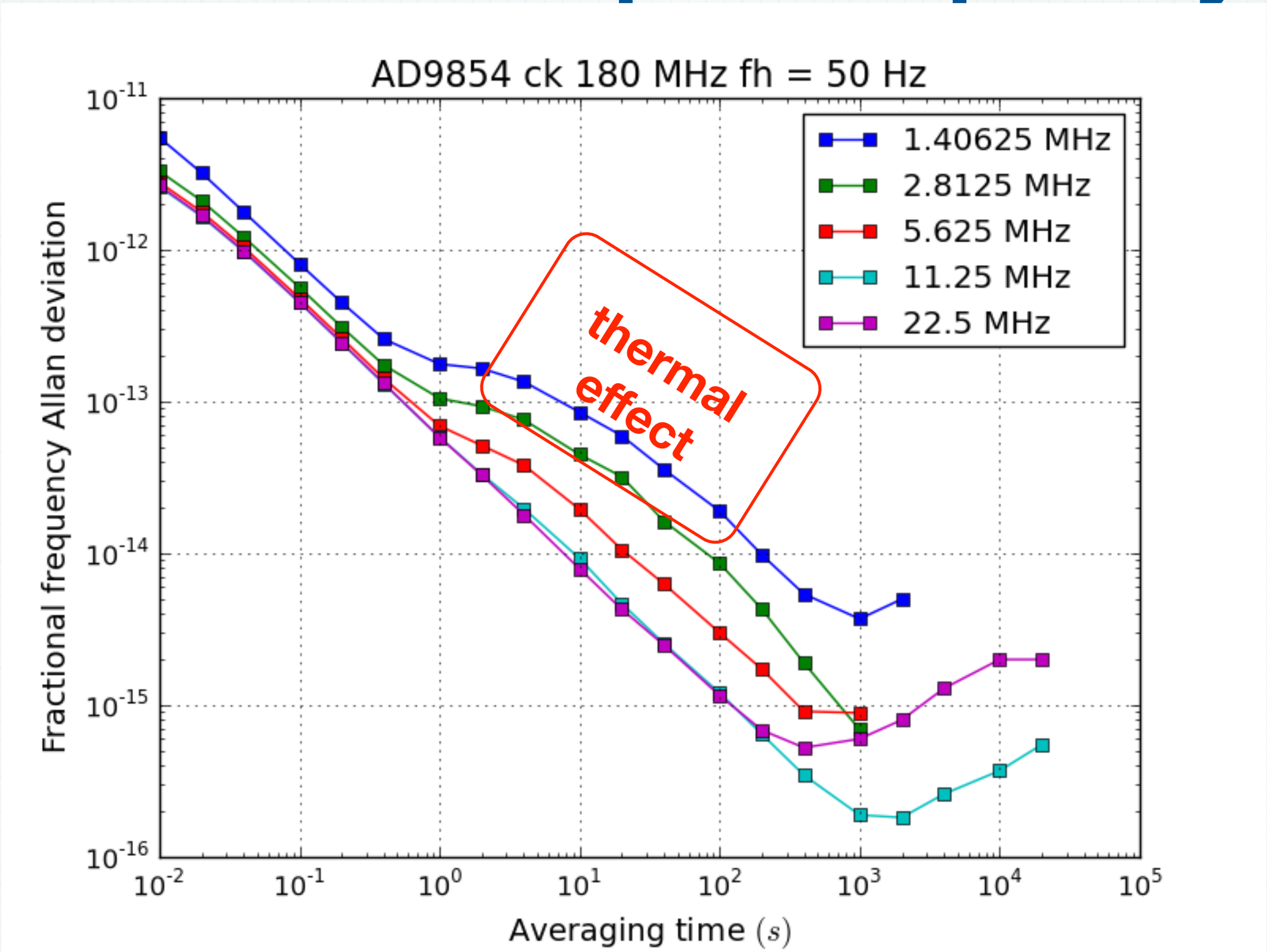
ADEV vs. clock frequency



ADEV vs. output frequency

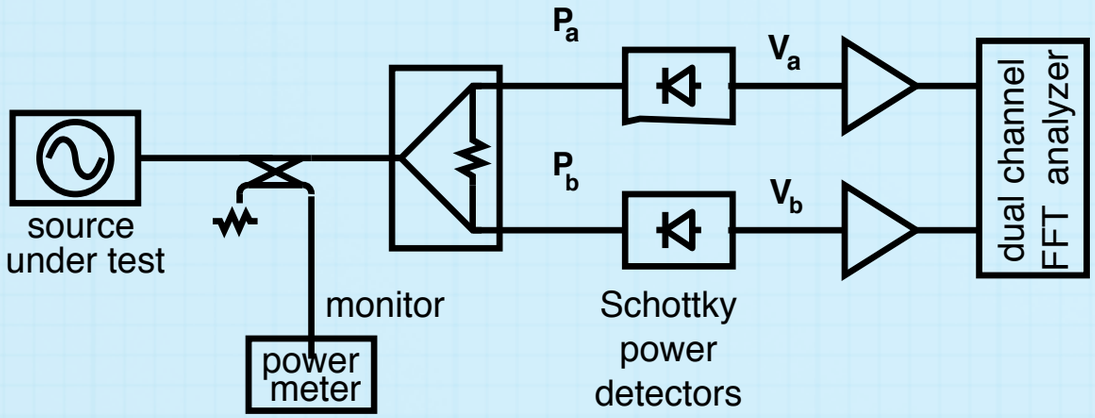


ADEV vs. output frequency



Experimental method (AM noise)

Cross-spectrum

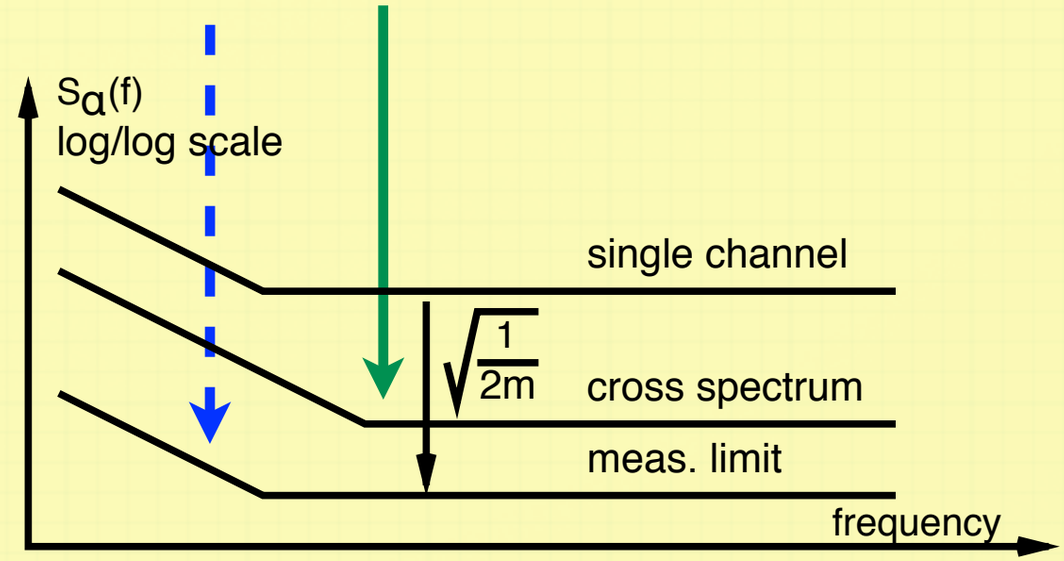


$$v_a(t) = 2k_a P_a \alpha(t) + \text{noise}$$
$$v_b(t) = 2k_a P_b \alpha(t) + \text{noise}$$

The cross spectrum $S_{ba}(f)$ rejects the single-channel noise because the two channels are independent.

$$S_{ba}(f) = \frac{1}{4k_a k_b P_a P_b} S_\alpha(f)$$

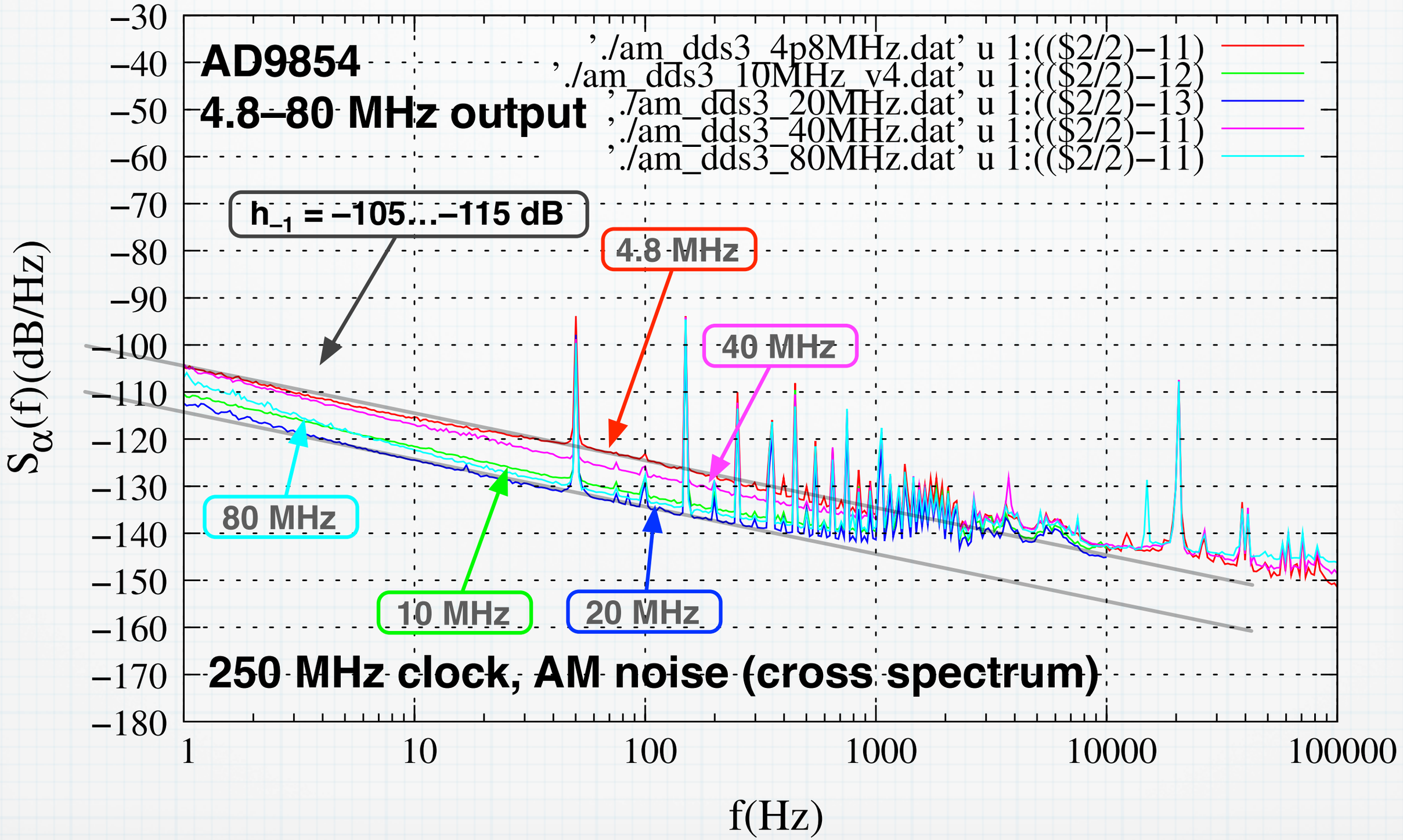
- **Averaging on m spectra, the single-channel noise is rejected by √1/2m**
- **A cross-spectrum higher than the averaging limit validates the measure**



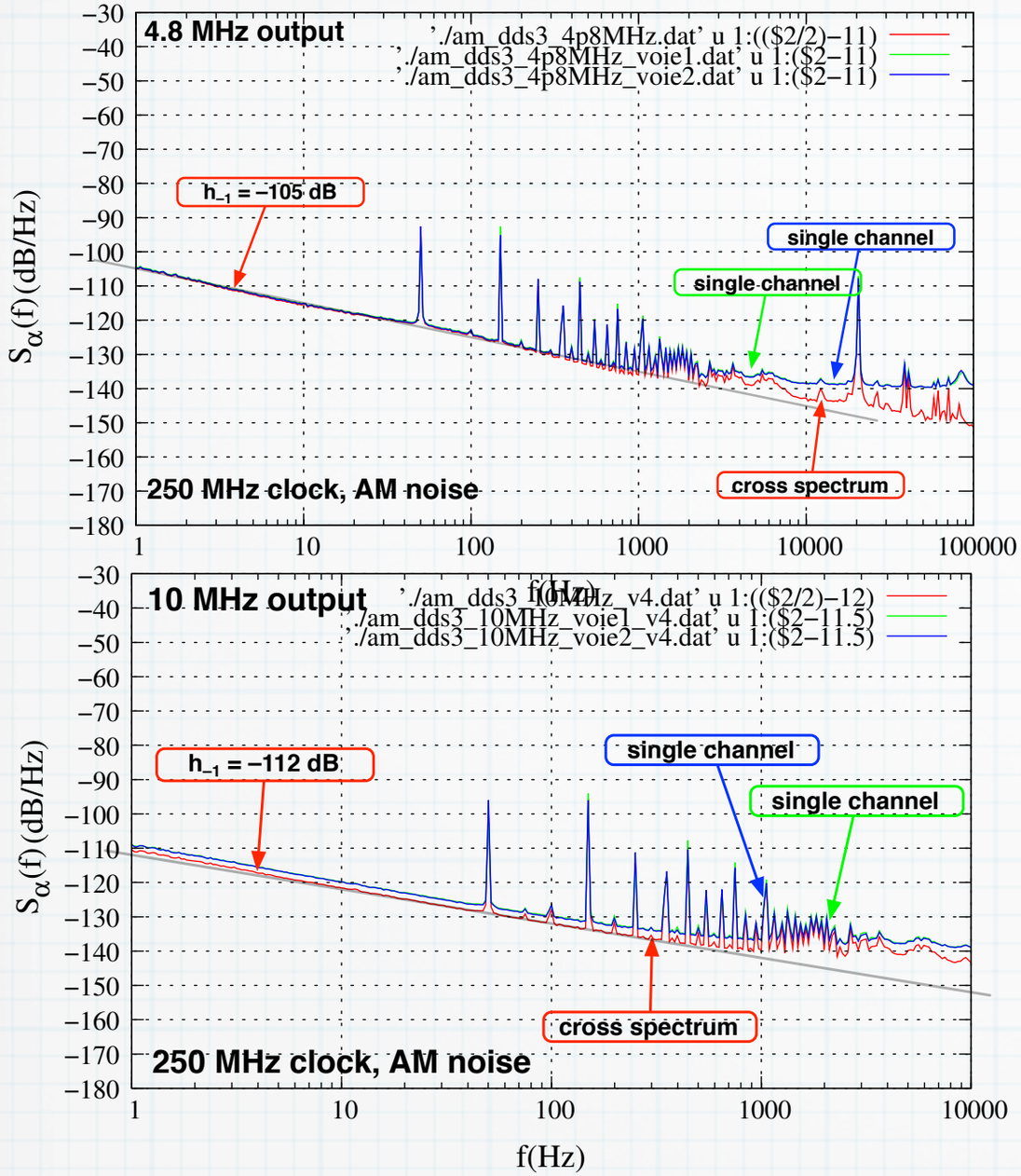
E. Rubiola, The measurement of AM noise of oscillators, arXiv:physics/0512082, Dec. 2005

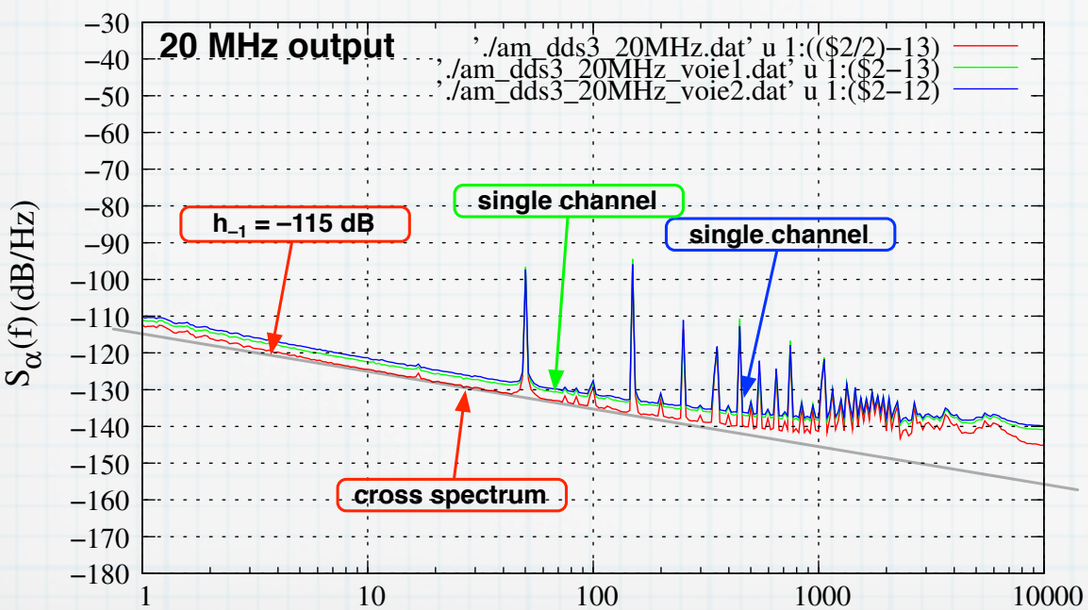
E. Rubiola, F. Vernotte, The cross-spectrum experimental method, arXiv:1003.0113v1 [physics.ins-det], Feb. 2010

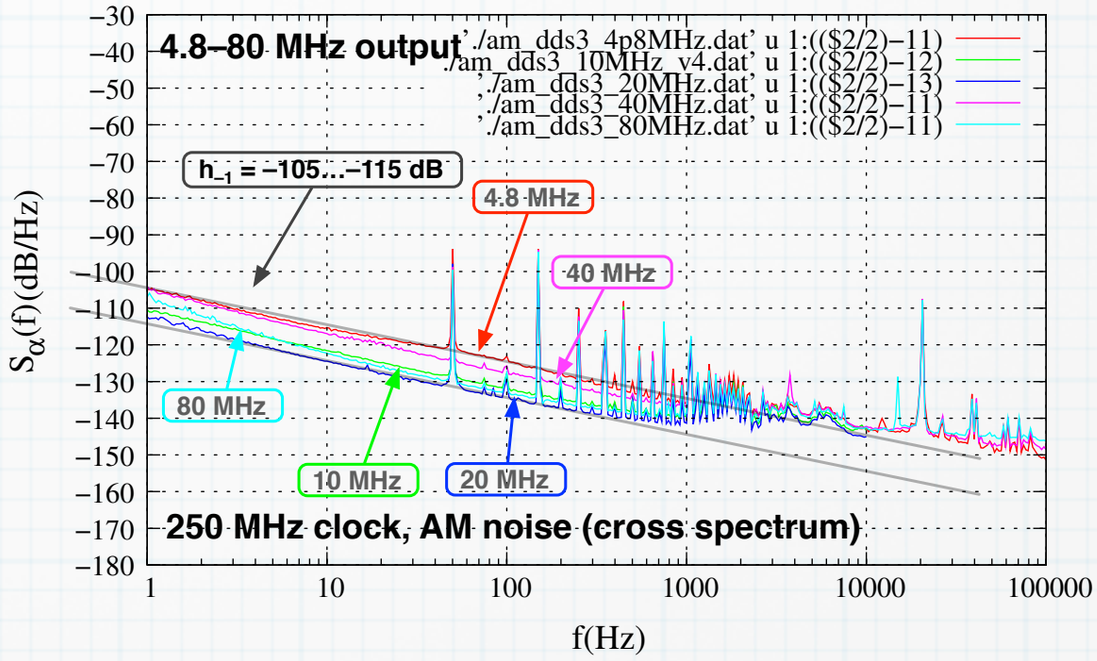
AM noise (1)


AD9854
4.8–80 MHz output
'./am_dds3_4p8MHz.dat' u 1:((($2/2)−11)
'./am_dds3_10MHz_v4.dat' u 1:((($2/2)−12)
'./am_dds3_20MHz.dat' u 1:((($2/2)−13)
'./am_dds3_40MHz.dat' u 1:((($2/2)−11)
'./am_dds3_80MHz.dat' u 1:((($2/2)−11)
h_-1 = –105…–115 dB
4.8 MHz
40 MHz
80 MHz
10 MHz
20 MHz
250 MHz clock, AM noise (cross spectrum)
S_α(f)(dB/Hz)
f(Hz)
−30
−40
−50
−60
−70
−80
−90
−100
−110
−120
−130
−140
−150
−160
−170
−180
1
10
100
1000
10000
100000

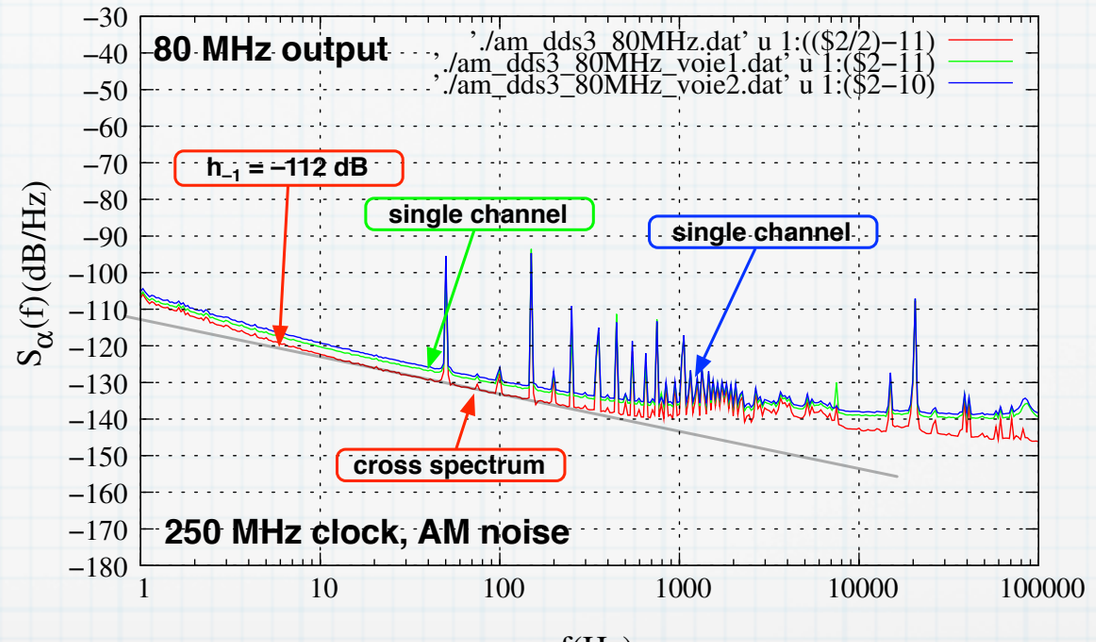
AM noise (2)


4.8 MHz output
'./am_dds3_4p8MHz.dat' u 1:(($2/2)−11)
'./am_dds3_4p8MHz_voie1.dat' u 1:($2−11)
'./am_dds3_4p8MHz_voie2.dat' u 1:($2−11)
h_-1 = −105 dB
single channel
single channel
cross spectrum
250 MHz clock, AM noise
S_α(f) (dB/Hz)
f(Hz)


10 MHz output
'./am_dds3_10MHz_v4.dat' u 1:(($2/2)−12)
'./am_dds3_10MHz_voie1_v4.dat' u 1:($2−11.5)
'./am_dds3_10MHz_voie2_v4.dat' u 1:($2−11.5)
h_-1 = −112 dB
single channel
single channel
cross spectrum
250 MHz clock, AM noise
S_α(f) (dB/Hz)
f(Hz)


4.8–80 MHz output
'./am_dds3_4p8MHz.dat' u 1:(($2/2)−11)
'./am_dds3_10MHz_v4.dat' u 1:(($2/2)−12)
'./am_dds3_20MHz.dat' u 1:(($2/2)−13)
'./am_dds3_40MHz.dat' u 1:(($2/2)−11)
'./am_dds3_80MHz.dat' u 1:(($2/2)−11)
h_-1 = −105…−115 dB
4.8 MHz
40 MHz
80 MHz
10 MHz
20 MHz
250 MHz clock, AM noise (cross spectrum)
S_α(f) (dB/Hz)
f(Hz)

20 MHz output
'./am_dds3_20MHz.dat' u 1:(($2/2)−13)
'./am_dds3_20MHz_voie1.dat' u 1:($2−13)
'./am_dds3_20MHz_voie2.dat' u 1:($2−12)
h_-1 = −115 dB
single channel
single channel
cross spectrum
250 MHz clock, AM noise
S_α(f) (dB/Hz)
f(Hz)


80 MHz output
'./am_dds3_80MHz.dat' u 1:(($2/2)−11)
'./am_dds3_80MHz_voie1.dat' u 1:($2−11)
'./am_dds3_80MHz_voie2.dat' u 1:($2−10)
h_-1 = −112 dB
single channel
single channel
cross spectrum
250 MHz clock, AM noise
S_α(f) (dB/Hz)
f(Hz)

Conclusions

- Noise theory and model for the DDS
- A lot of still-not-published experimental data
  - Phase noise
  - Allan deviation
  - Amplitude noise
- Experiments done at INRIM and at FEMTO-ST
- Model and experimental data are in fair agreement

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5 — Dividers

- Π and Λ Dividers
- Microwave Dividers

Π and Λ Dividers

Motivations

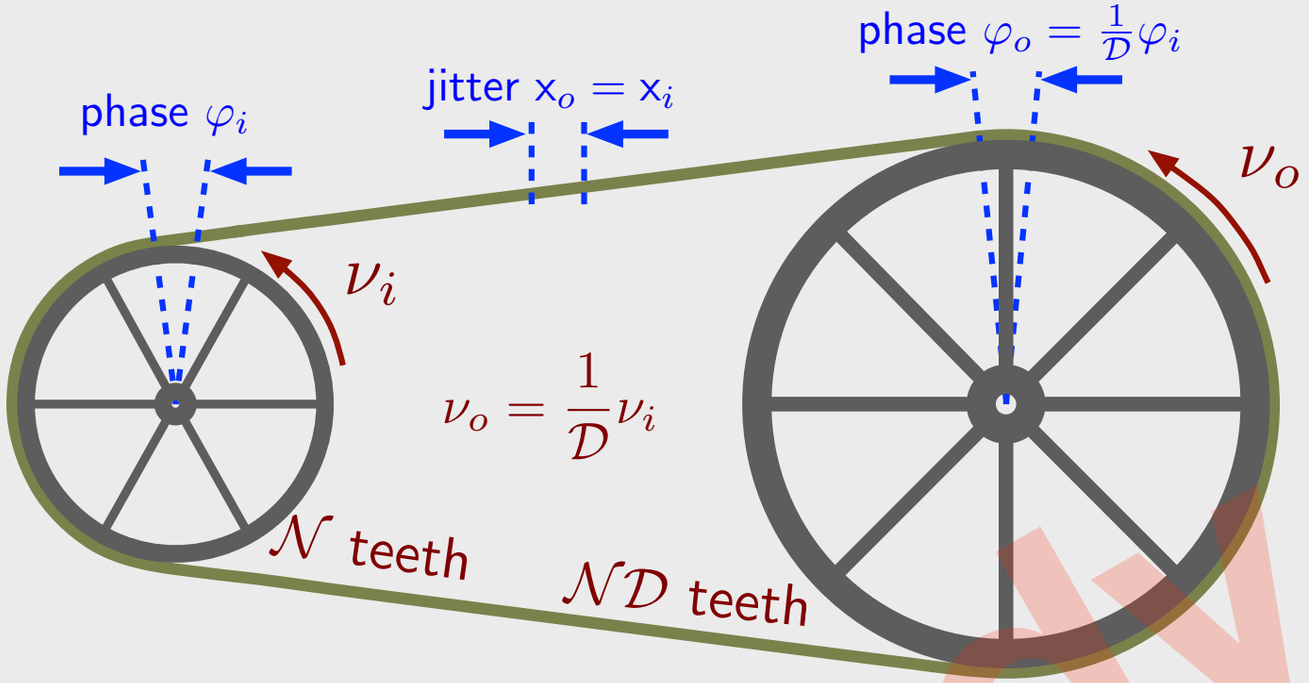
- Seminal article by W. F. Egan (1990)
  - Milestone in the domain, never forget it
  - However, TTL and ECL logic families are now obsolete

- Microwave (photonics) –> highest spectral purity
- Transfer the spectral purity to HF/VHF
  - Dividers are more comfortable than multipliers
    - NIST now uses analog dividers

- Nowadays digital electronics is fantastic
  - CPLD & FPGA –> Easy to duplicate
  - High number of gates for cheap
  - High toggling frequency (1.5 GHz)

W. F. Egan Egan WF, Modeling phase noise in frequency dividers, IEEE T UFFC 37(4), July 1990
E. Rubiola & al, Phase noise in the regenerative frequency dividers, IEEE T IM 41(3), June 1992
A. Hati & al, Ultra-low-noise regenerative frequency divider…, Proc IEEE IFCS, May 2012

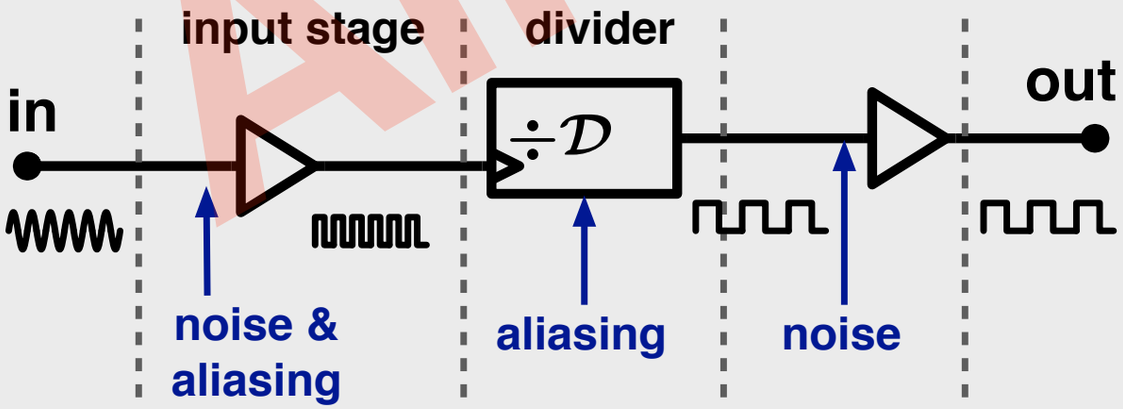
The Gear Work Model

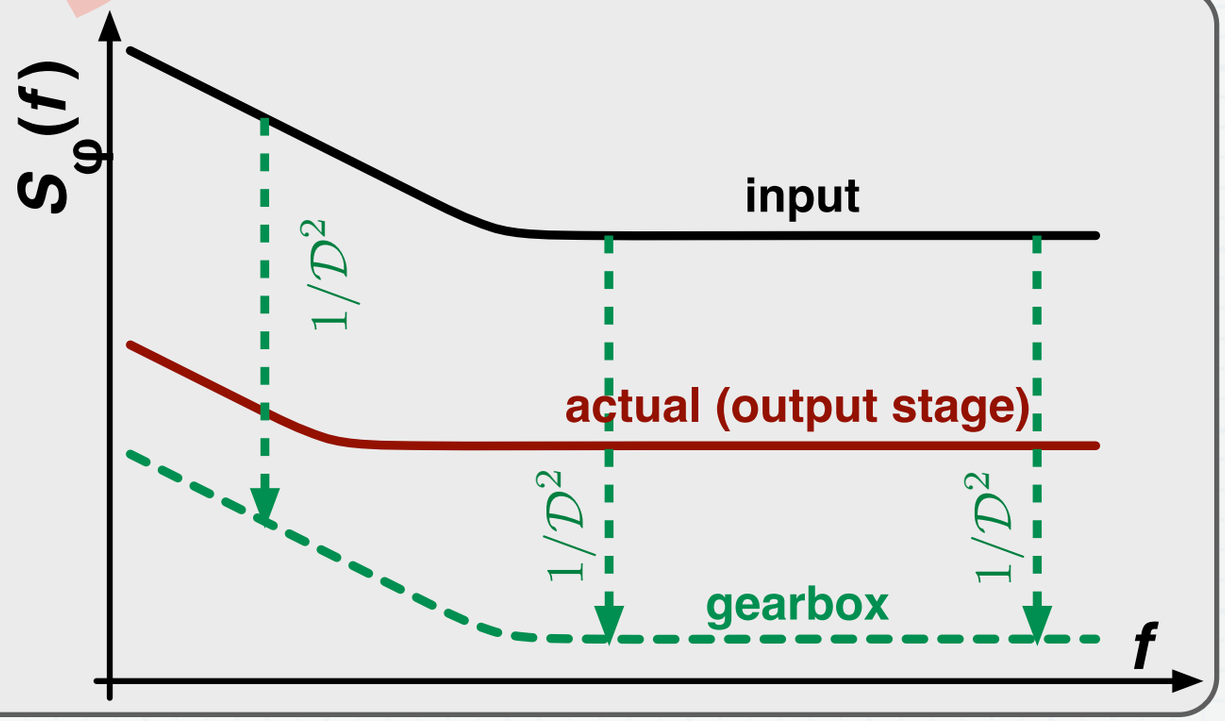


- **The noise-free divider**
  - **Keeps the input jitter x(*t*) (phase-time fluctuation)**
  - **Scales down**
    - **φ by 1/*D*** [rad]
    - **Sφ by 1/*D*²** [rad²/Hz]

In the real divider

- **Sφ of the output often dominates**
- **Aliasing is present**





W. F. Egan Egan WF, Modeling phase noise in frequency dividers, IEEE T UFFC 37(4), July 1990

Parseval Theorem

The energy calculated in the time domain is equal to the energy calculated in the frequency domain

time domain

$$\int_{-\infty}^{\infty} |x(t)|^2 \, dt = \int_{-\infty}^{\infty} |X(f)|^2 \, df$$

frequency domain

Average power, truncated signal

$$\sigma^2 = \frac{1}{T} \int_0^T |x(t)|^2 \, dt$$

One-sided PSD, truncated signal

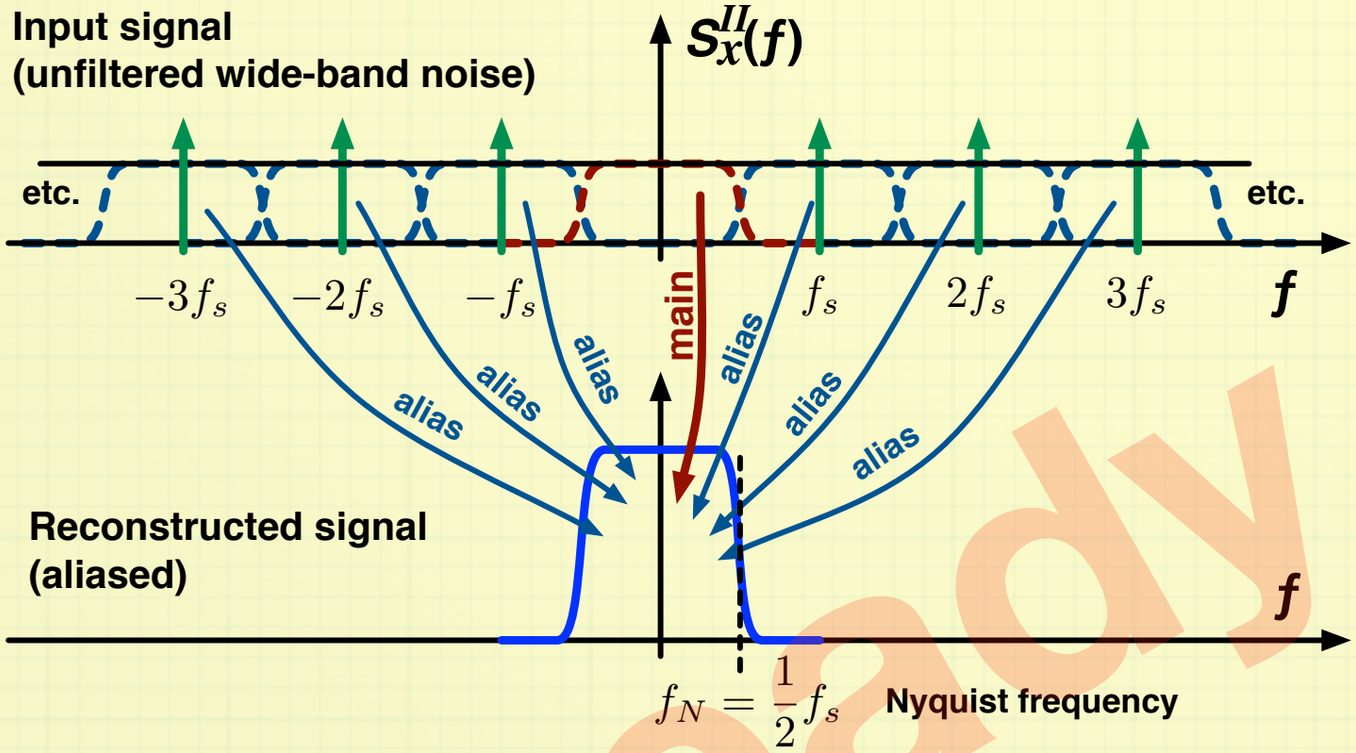
$$S_x(f) = \frac{2}{T} |X_T(f)|^2$$

$$\sigma^2 = \int_0^{\infty} S_x(f) \, df$$

For ergodic signals, the time average is equal to the ensemble average

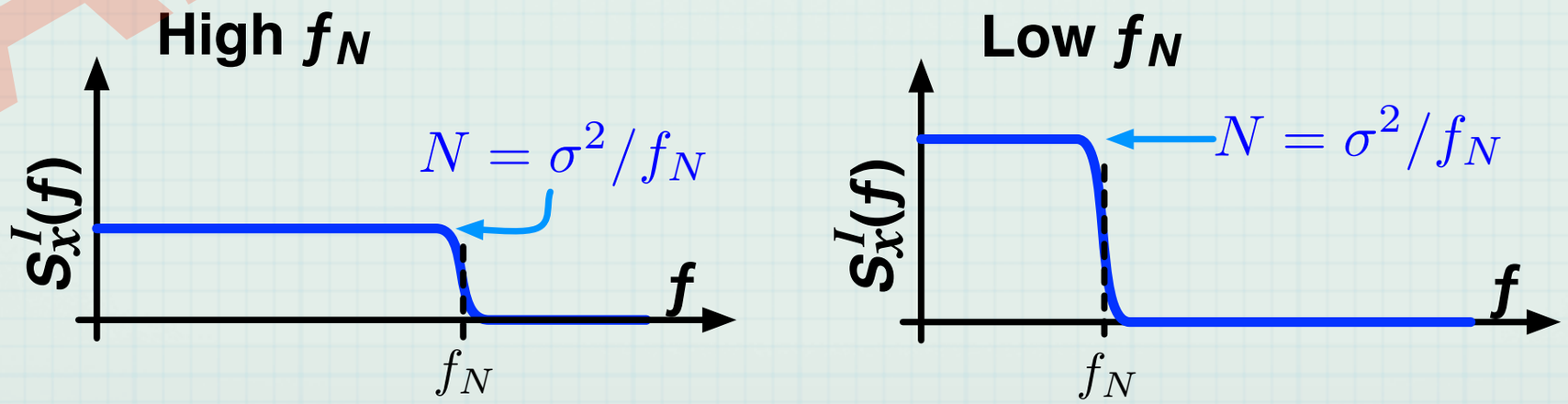
Sampling and Aliasing

— Energy conservation applies to the unfiltered signal —

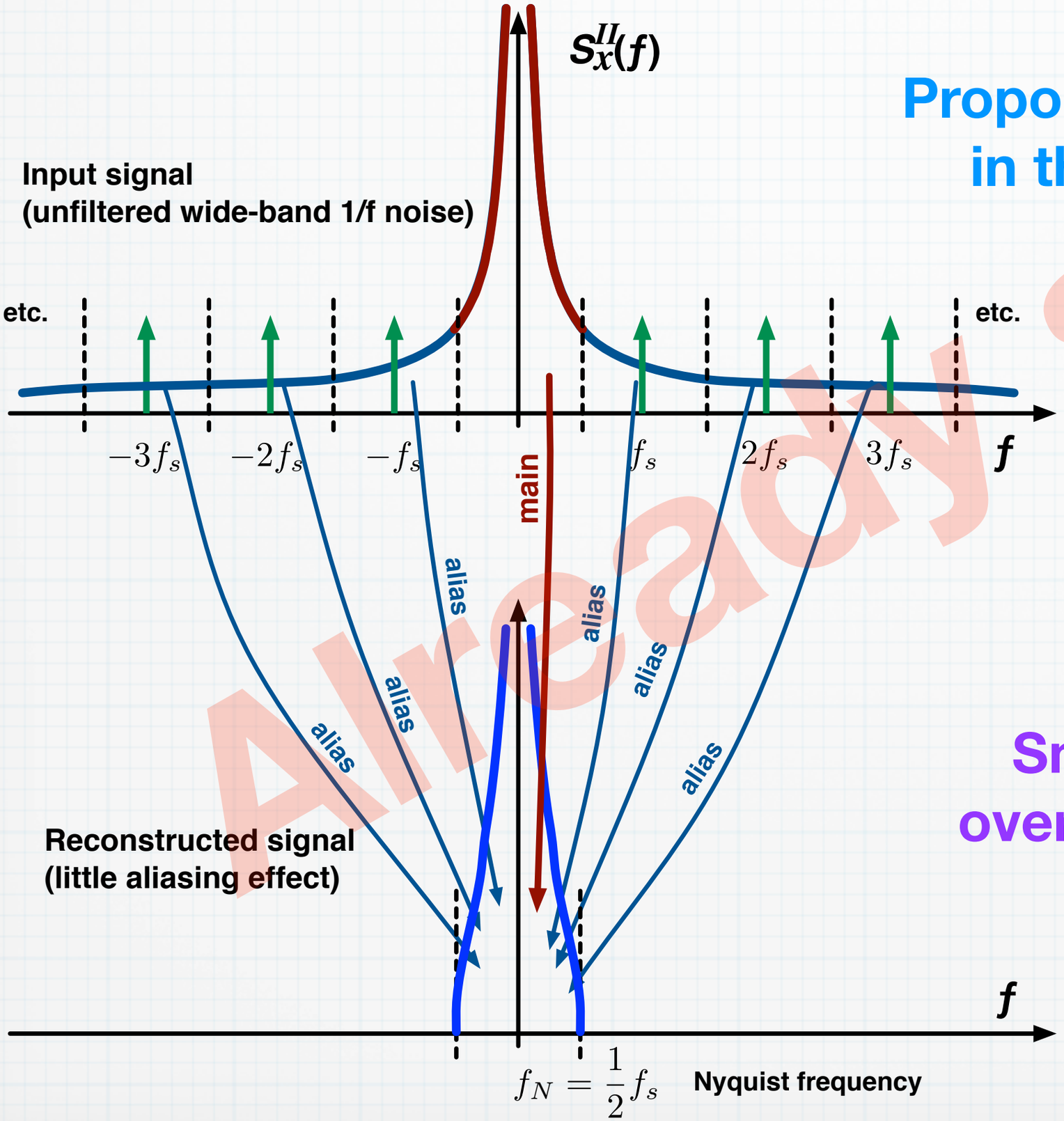


- Multiple aliases overlap to the main part of the spectrum
- With white noise, the PSD increases by B/f_N (Bandwidth / Nyquist f)

Downsampling increases the (PM) noise spectrum



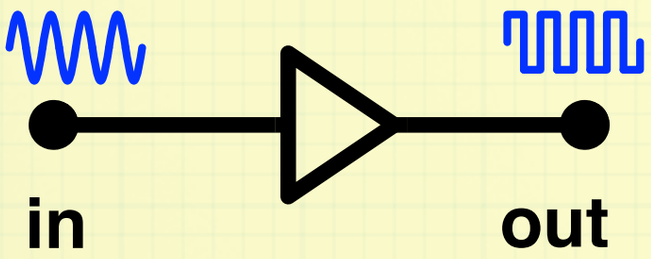
Aliasing and 1/*f* Noise



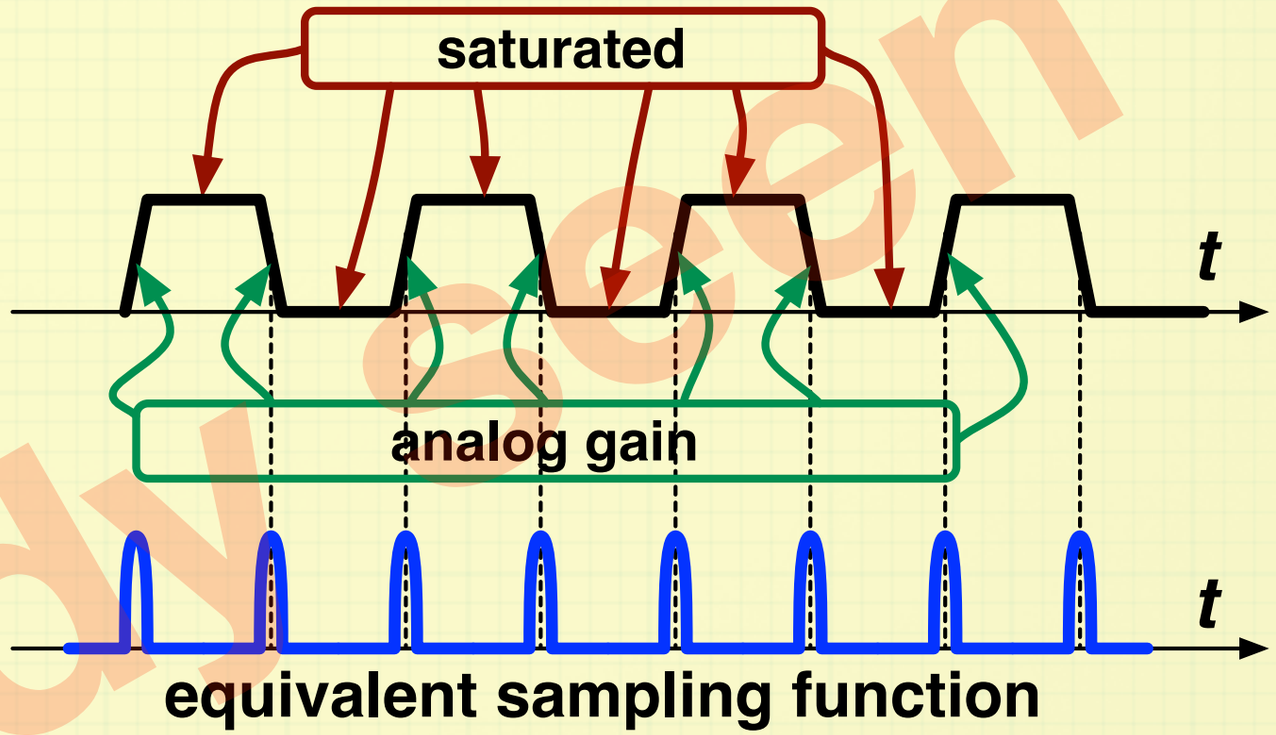
Proportionally lower power in the higher-*f* aliases

Small effect on the overall noise spectrum

PM-Noise Aliasing in the Input Stage



Convert the input sinusoid into a square wave, as appropriate



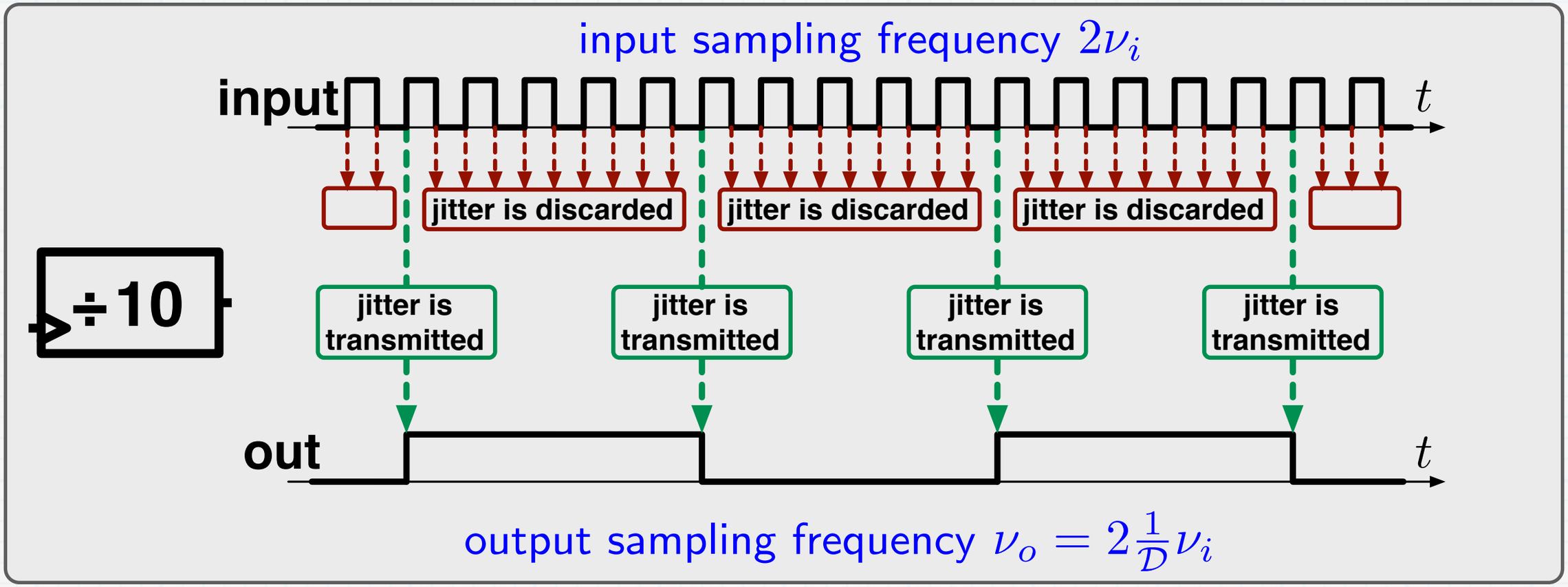
- Edge-sampling at $2\nu_i$ inherent in the sin-to-square conversion
- Full-bandwidth (B) noise is taken in
- The phase-noise Nyquist frequency is ν_i
- The sampling process increases the noise by B/ν_i

Eventually, clipping removes the AM noise [Pfaff 1974]

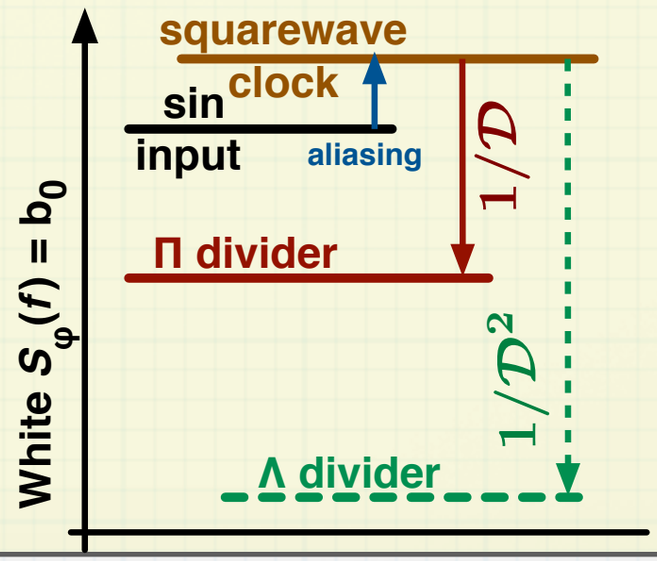
Aliasing in Π Divider

Regular synchronous divider

The Greek letter Π recalls the square wave Π Π Π Π



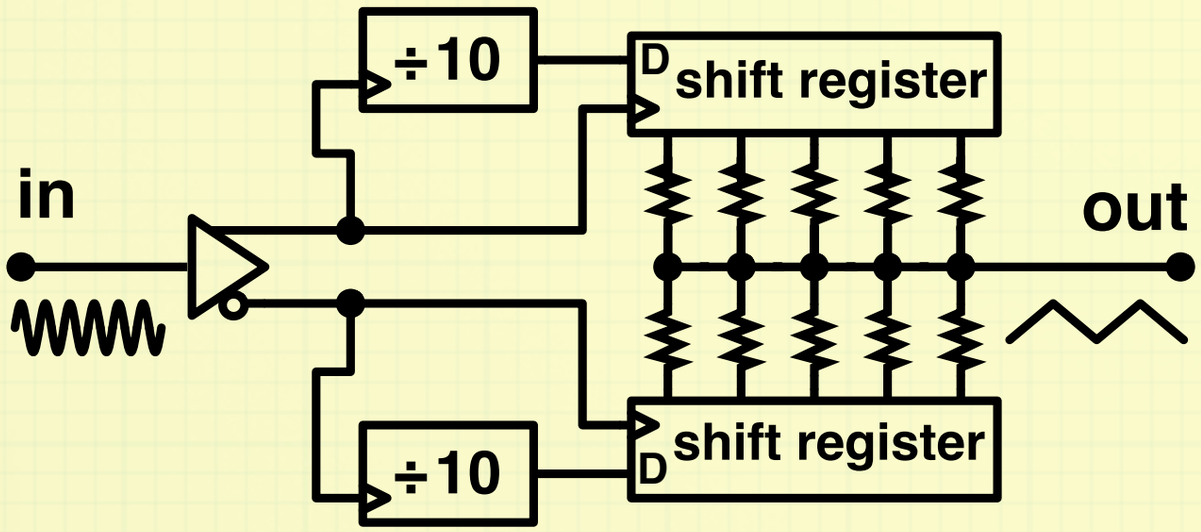
- The gearbox scales *S*φ down by 1/*D*²
- The divider takes 1 edge out of *D*
  - Raw decimation without low-pass filter
  - Aliasing increases *S*φ by *D*
- Overall, *S*φ scales down by 1/*D*



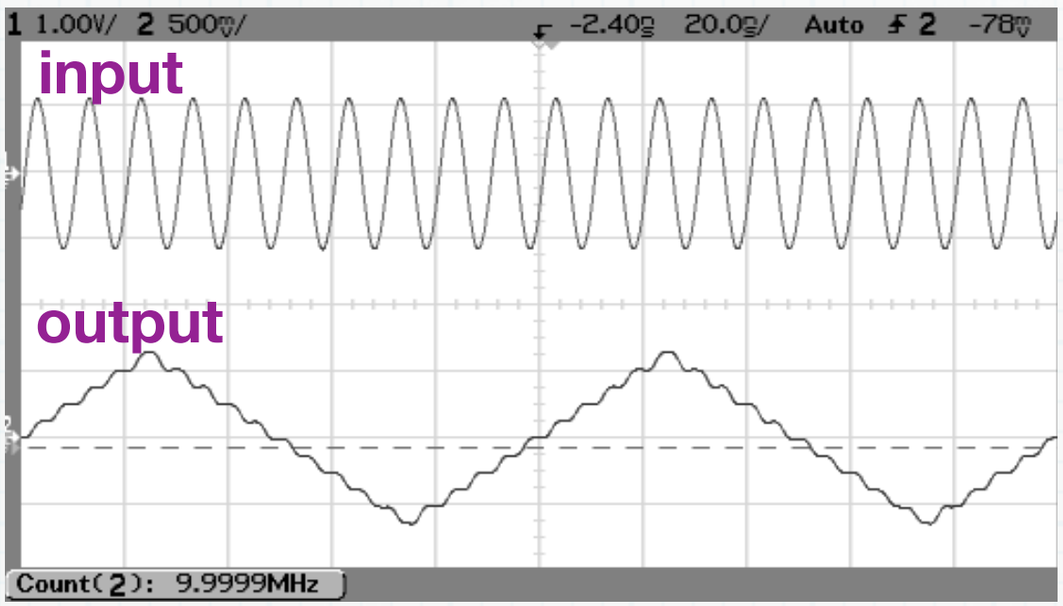
The Λ Divider – Little/no Aliasing

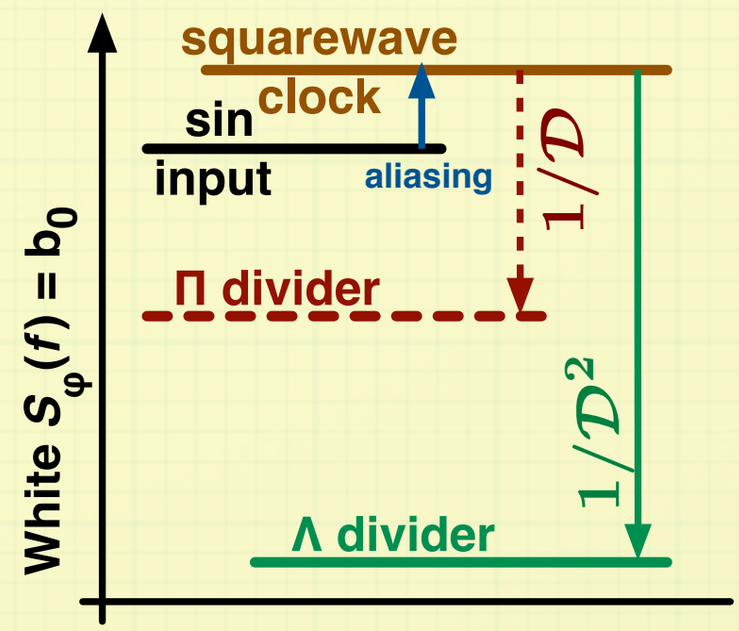
New divider architecture

Series of Greek letters ΛΛΛΛ recalls the triangular wave



- Gearbox and aliasing –> 1/*D* law
- Add *D* independent realizations shifted by 1/2 input clock,
- reduce the phase noise by 1/*D*,
- … and get back the $1/D^2$ law





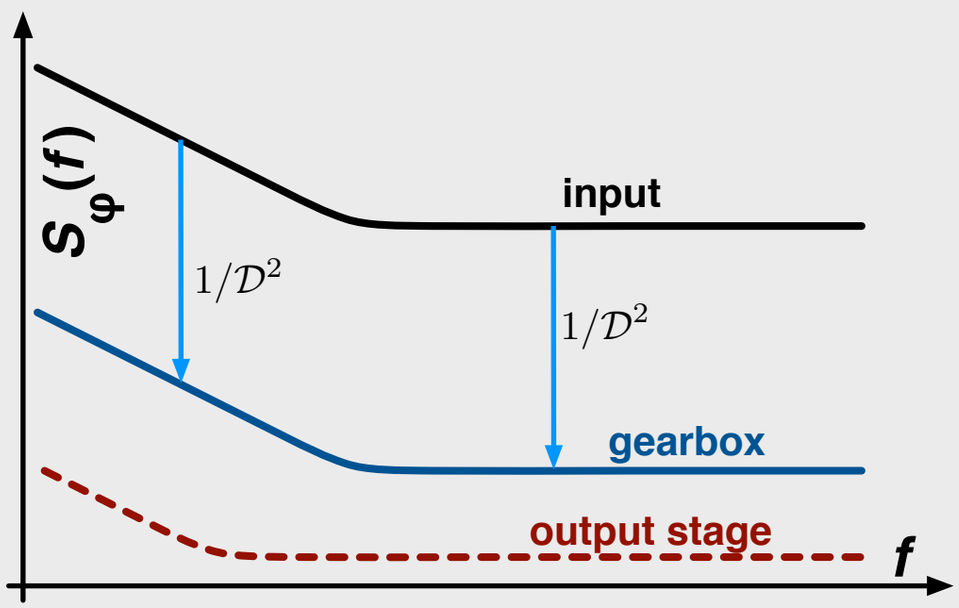
The names Π and Λ derive from the shape of the weight functions in our article on frequency counters

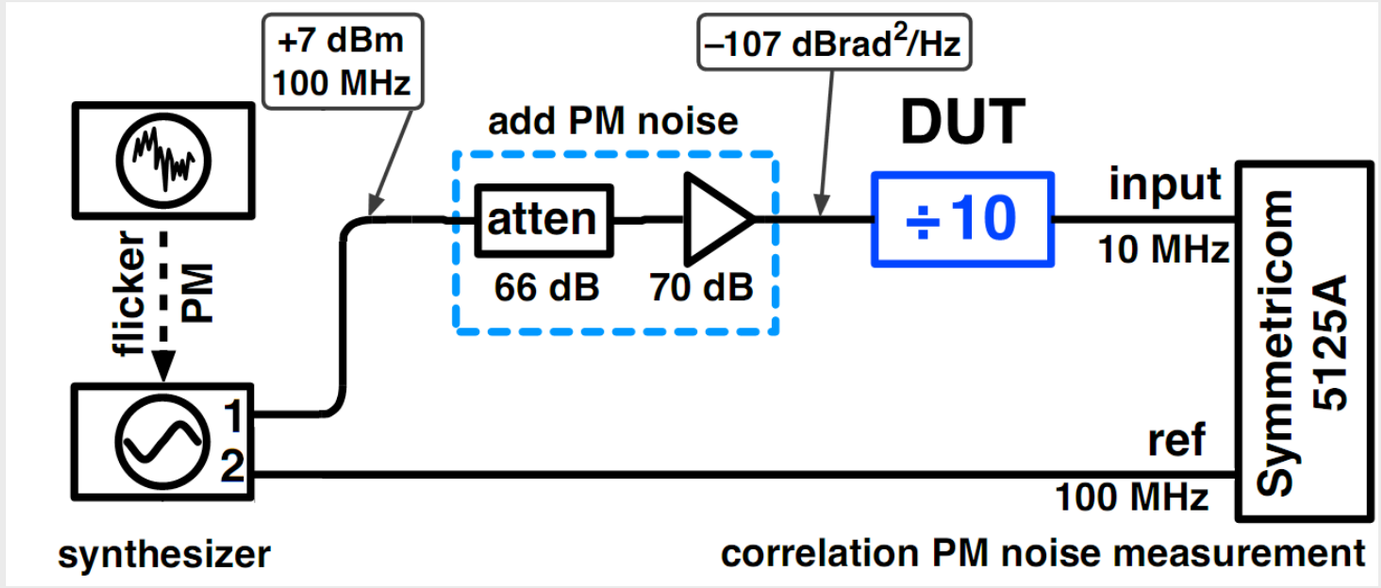
E. Rubiola, On the measurement of frequency … with high-resolution counters, RSI 76 054703, 2005

Experimental Method

Large input PM noise is used to emphasize the effect of aliasing

- **Intentionally high PM noise at the input**
- **The scaled-down input noise is higher than the output-stage noise**





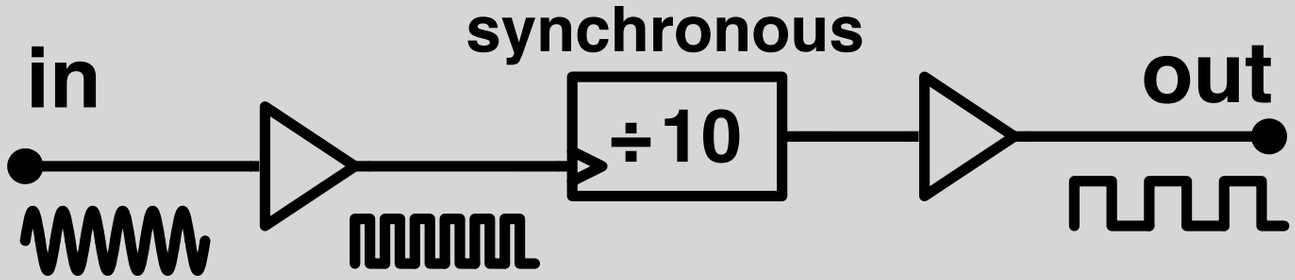
- **Large attenuation/ampli –> noise**
- **Digital instruments for phase-noise measurement can handle**

$$f_{\text{input}} \neq f_{\text{reference}}$$

- **Correlation reduces the background**

Dividers Under Test

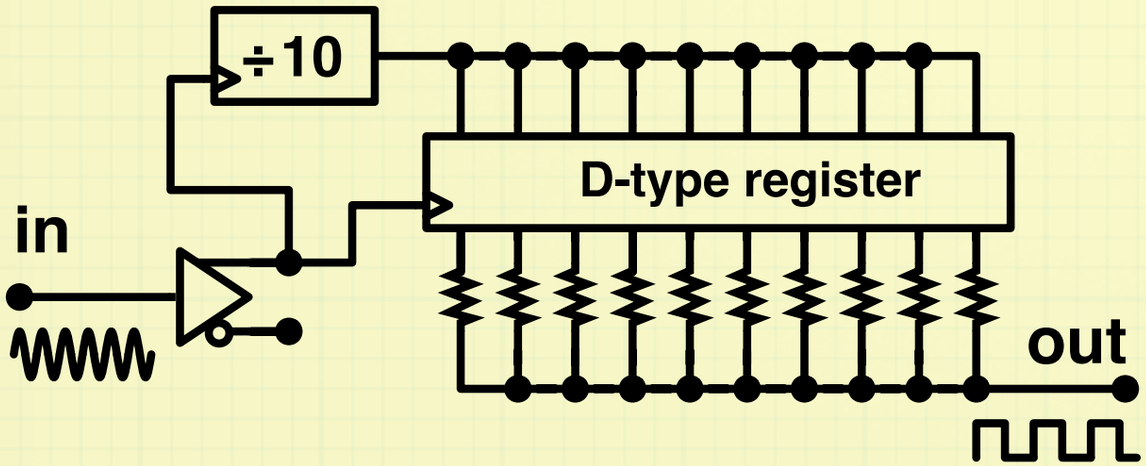
EPM3064A CPLD (Altera MAX 3000 Series, 64 macro-cells, speed grade 7 ns)



Π divider

– the one everybody knows –

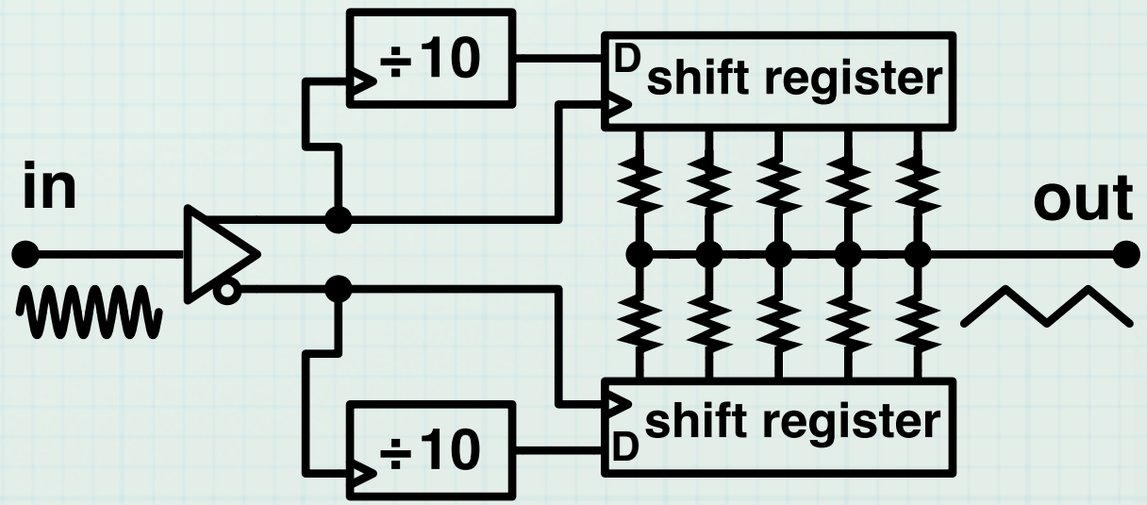
Multi-buffer Π divider



The outputs are arguably independent

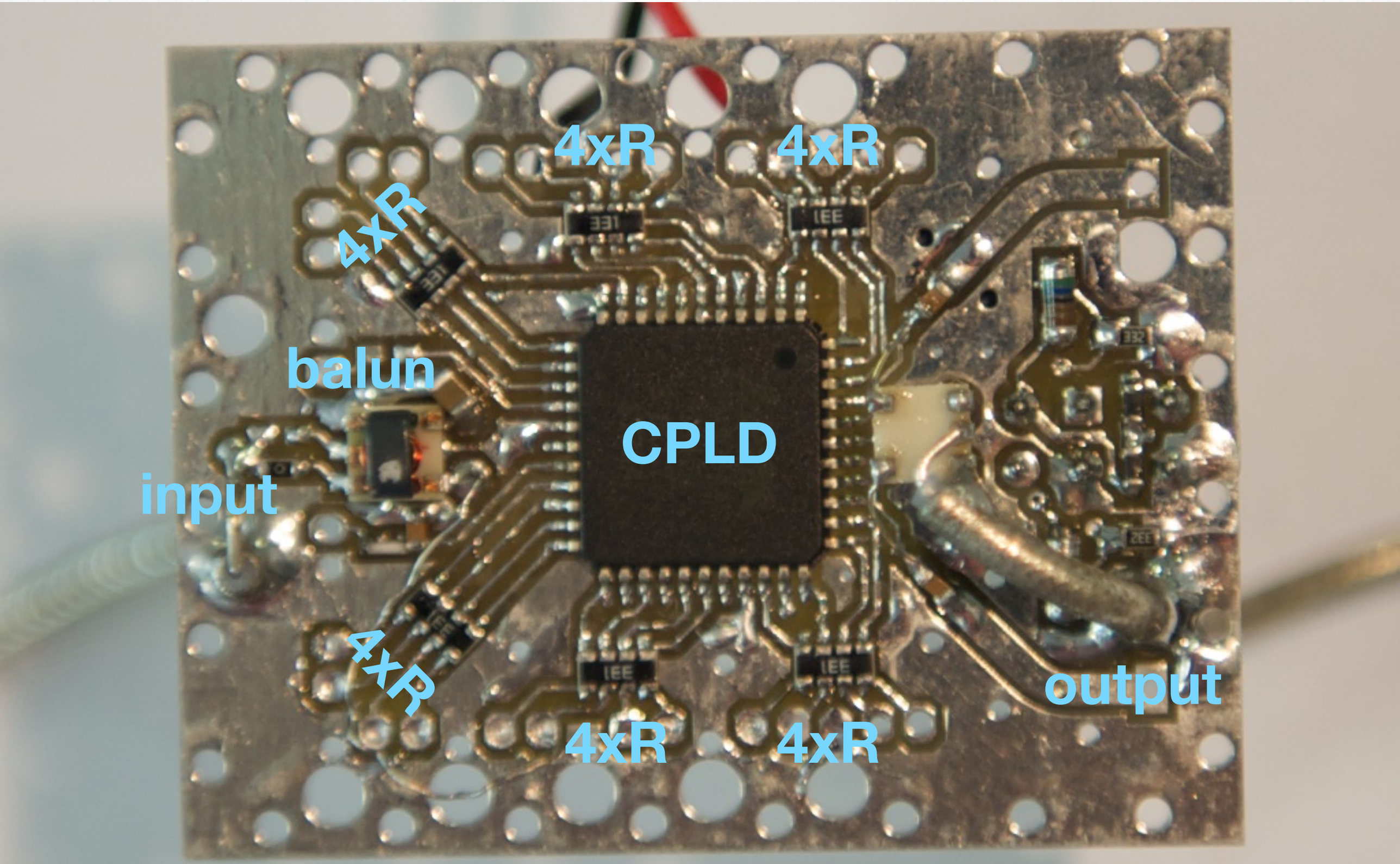
Try to reduce the output-stage noise

Λ divider

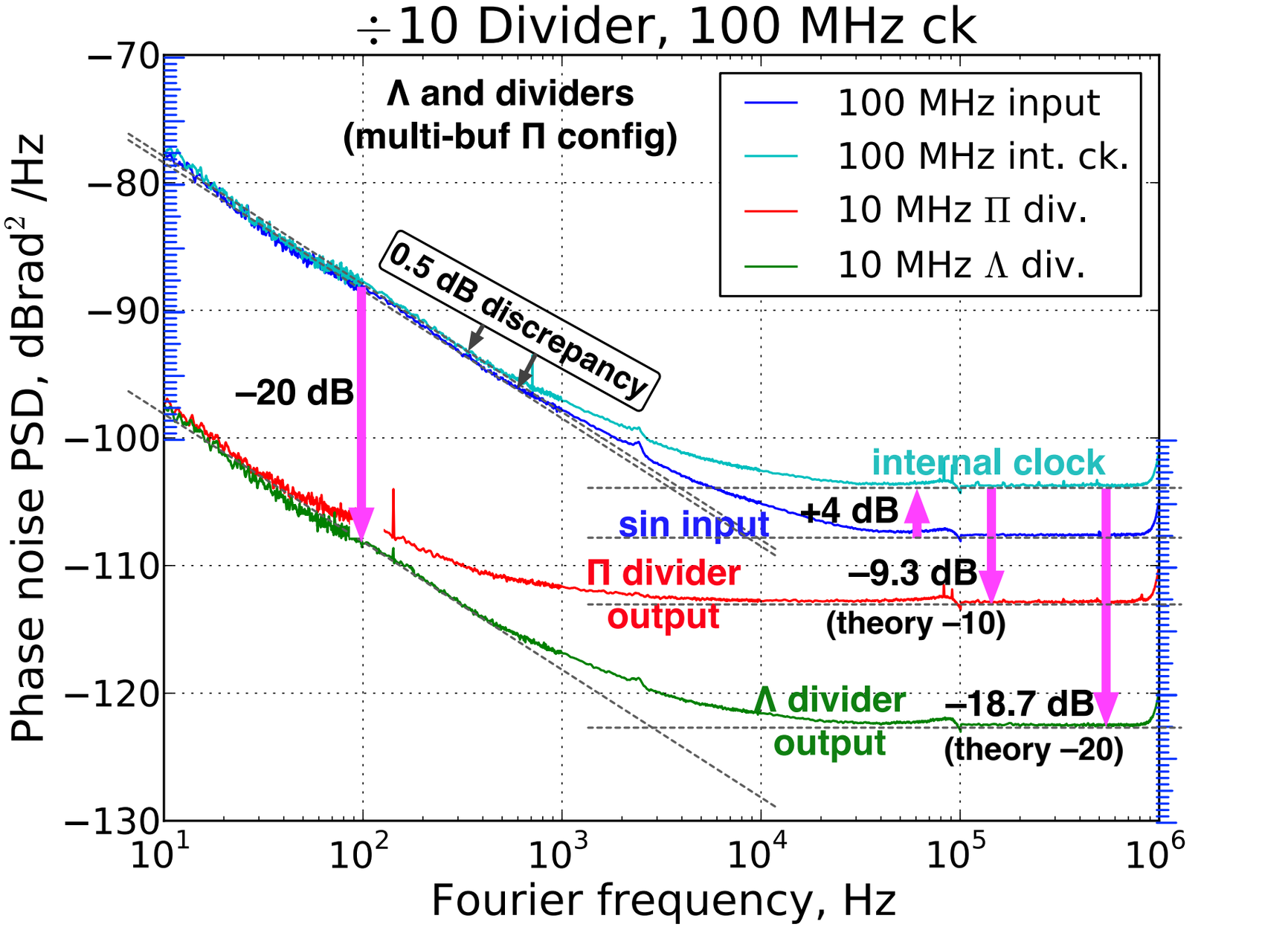


White noise:
The clock edges are independent
Correct for aliasing

As Simple as That…



Results – Test on Aliasing

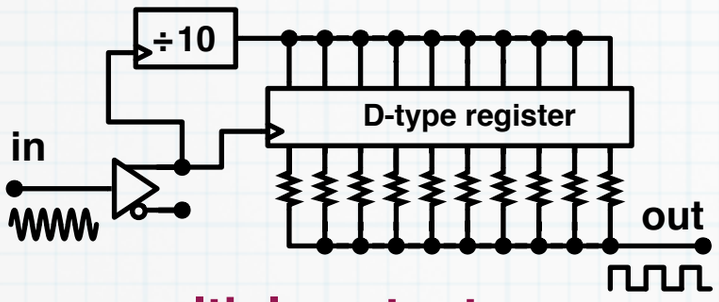


- **Flicker region**
  - **Negligible aliasing**
  - **1/D^2 law (–20 dB)**

- **White region**
- **Aliasing in the front-end –> +4 dB**
- **1/D law and 1/D^2 law**

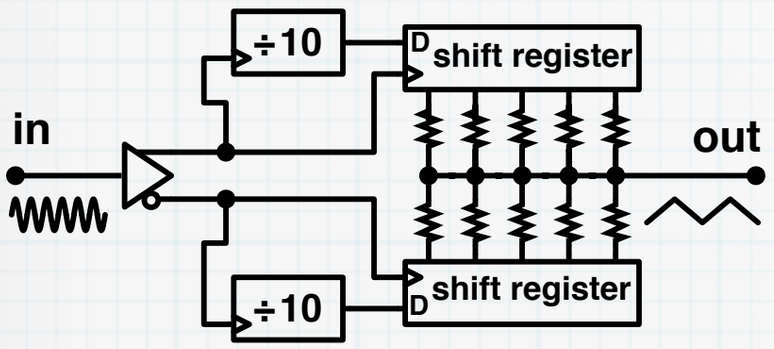
Phase Noise of Real Dividers

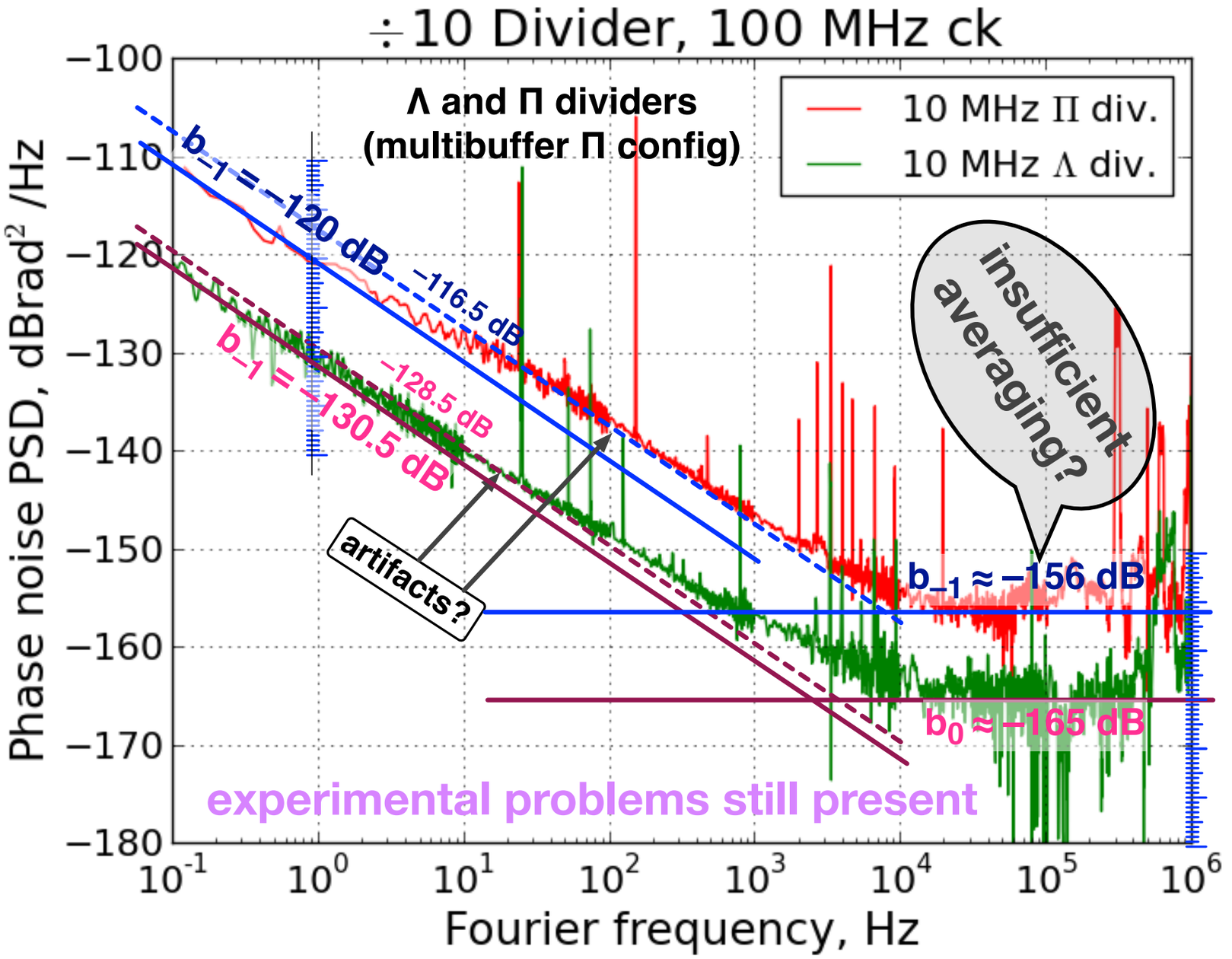
Multibuffer Π divider



multiple outputs are expected to reduce the output-stage noise – not happened, why? –

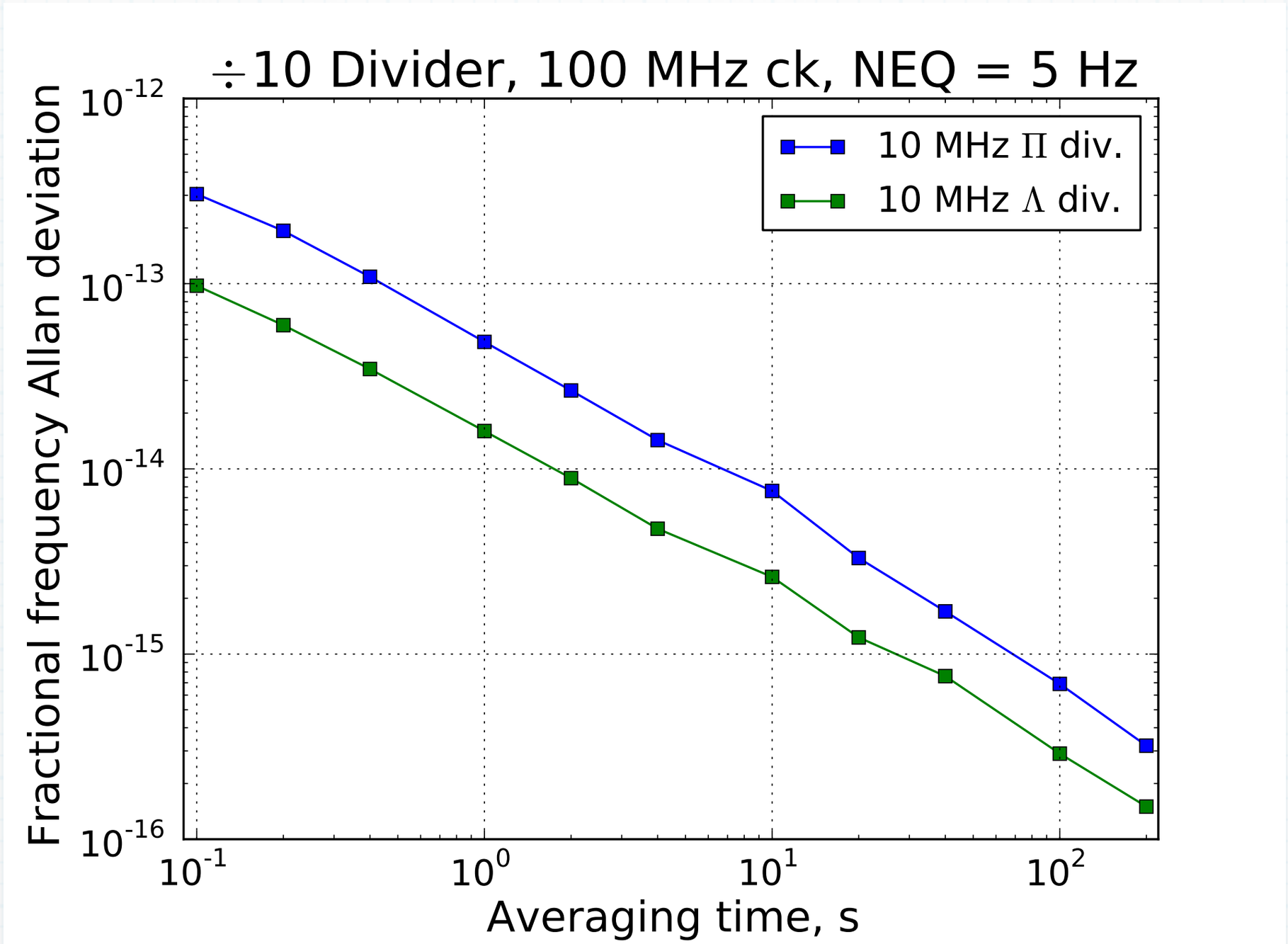
Λ divider





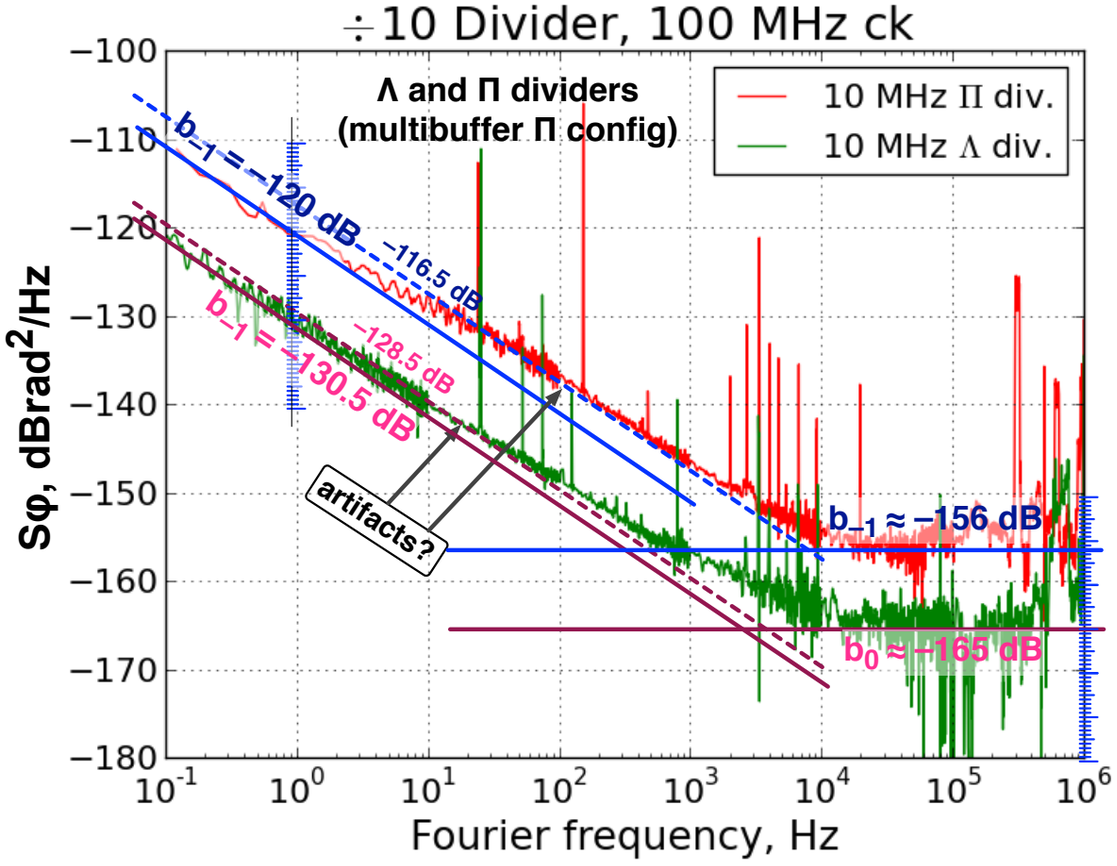
- Flicker region –> Negligible aliasing
- The multibuffer Π divider is still not well explained
- The Λ divider exhibits low 1/*f* and low white noise

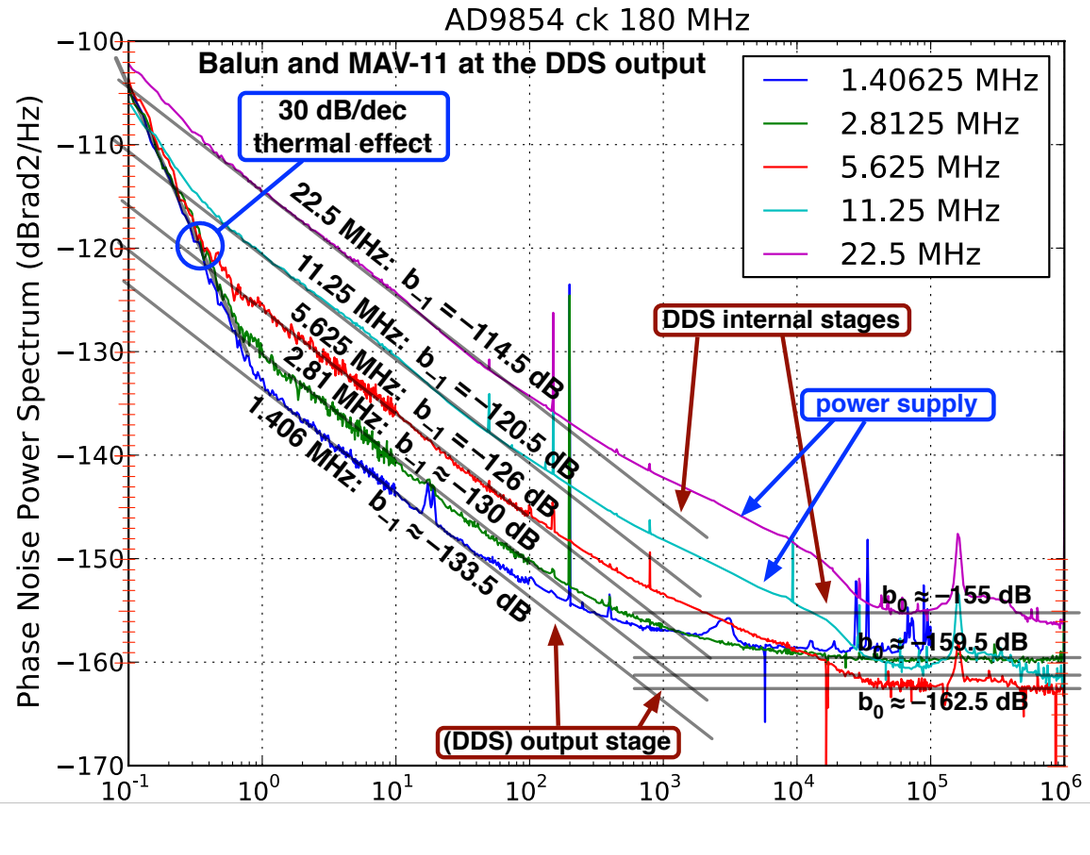
Allan Deviation in Real Dividers



- **Slope 1/τ, typical of white and flicker PM noise**
- **The Λ divider performs 2×10^{-14} at $\tau = 1$ s, 10 MHz output**

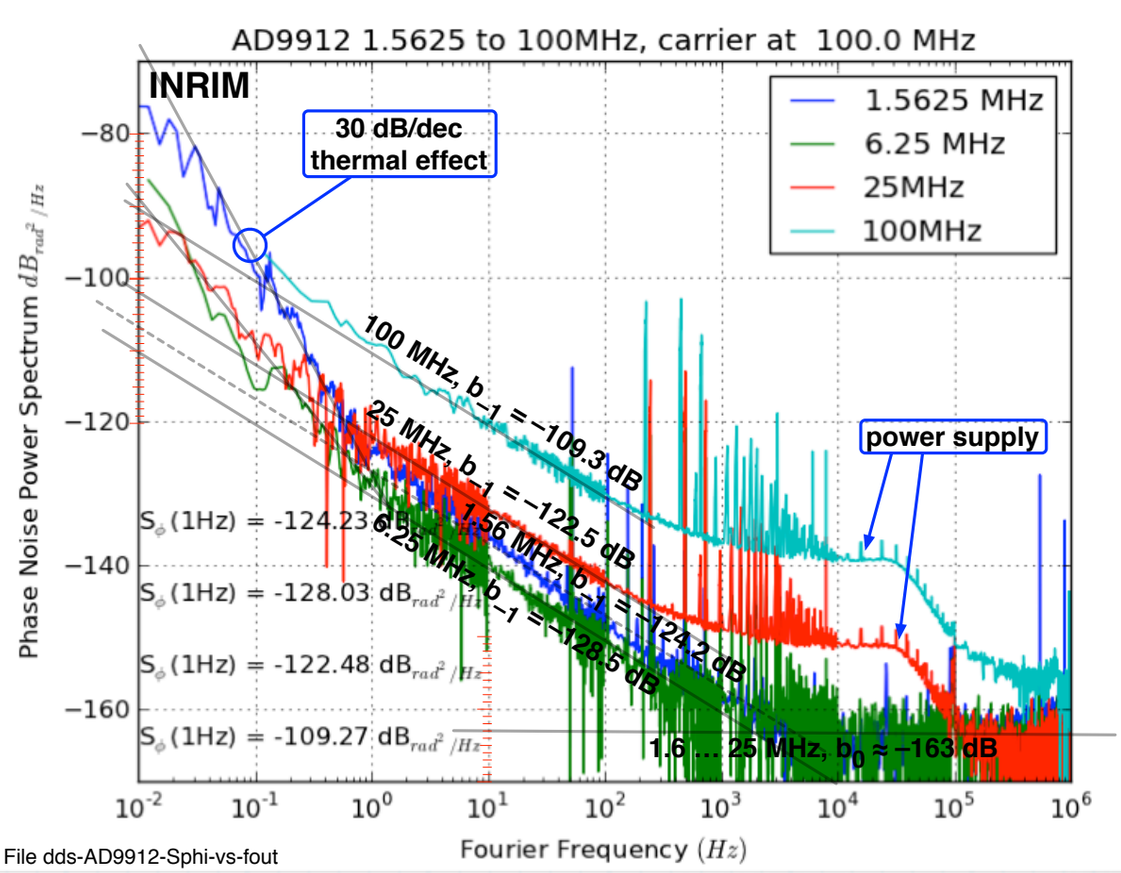
The Λ Divider Versus the DDS



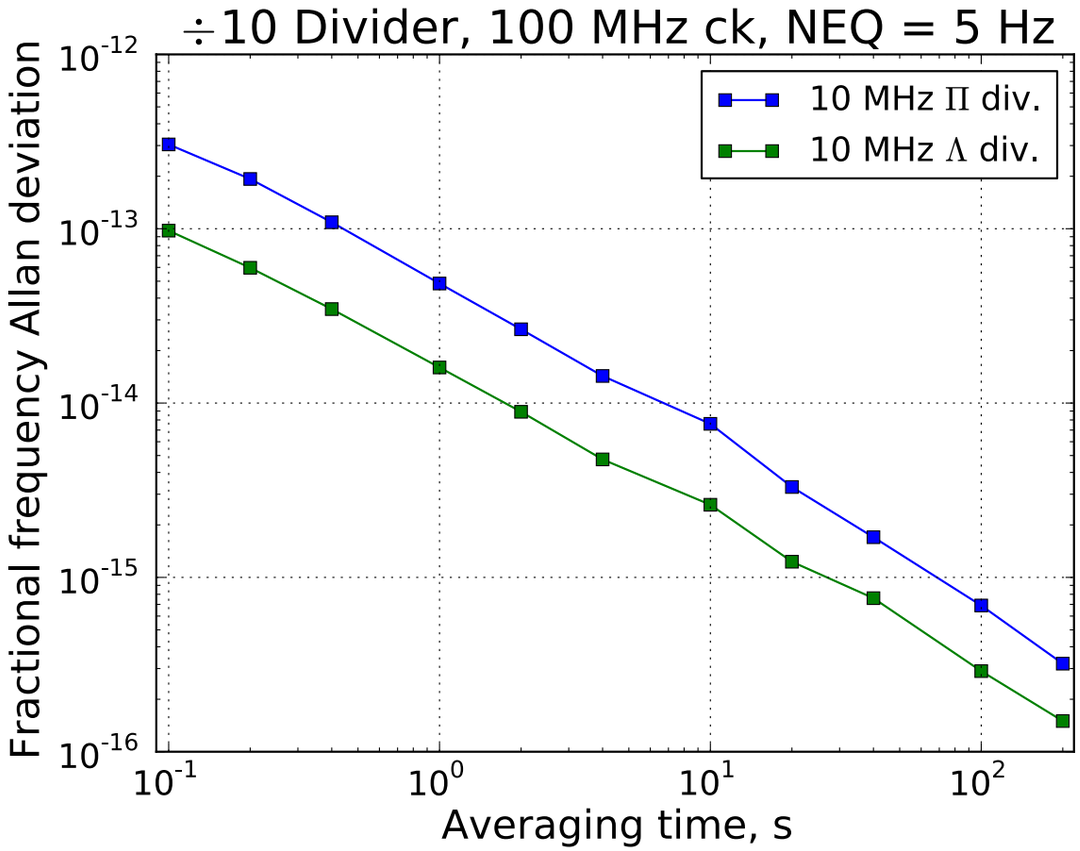


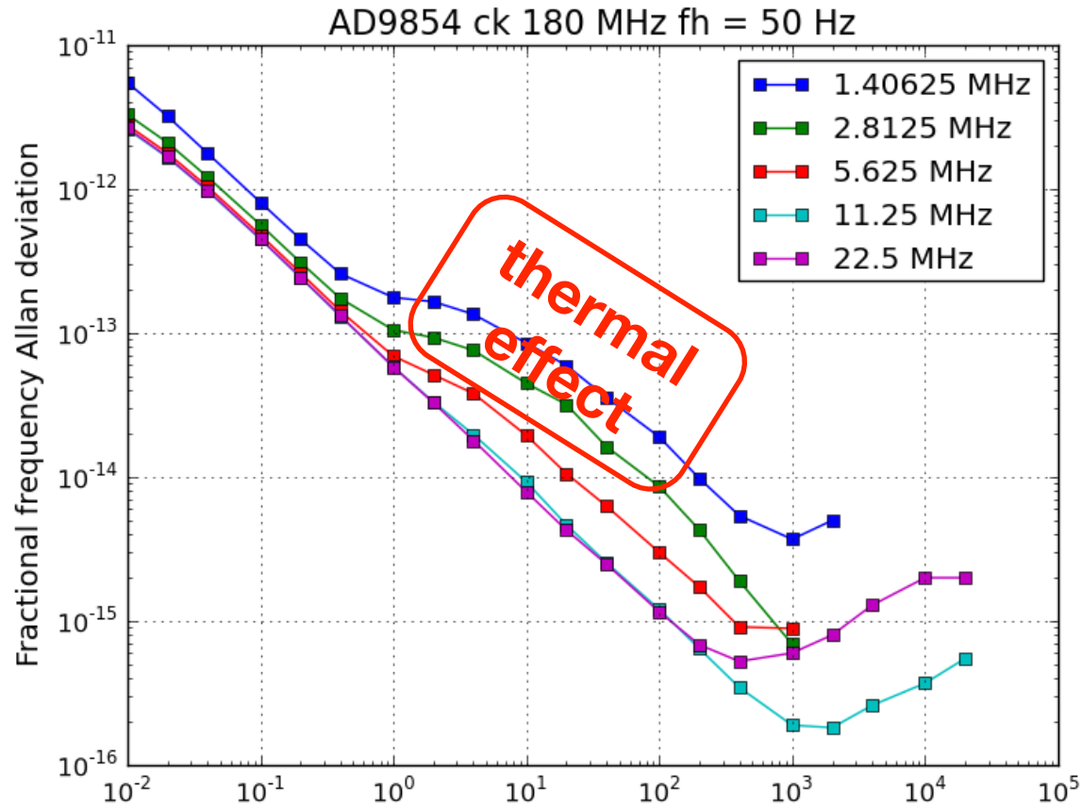
Noise of the Λ divider and two DDSs

noise	Λ div.	AD9854	AD9912
b_0	–165	–160	≈ –163
b_{-1}	–130.5	–121.5	–129 inferred
b_{-2}	—	—	–132 plot not shown
b_{-3}	—	–134	(seen at lower v_o)

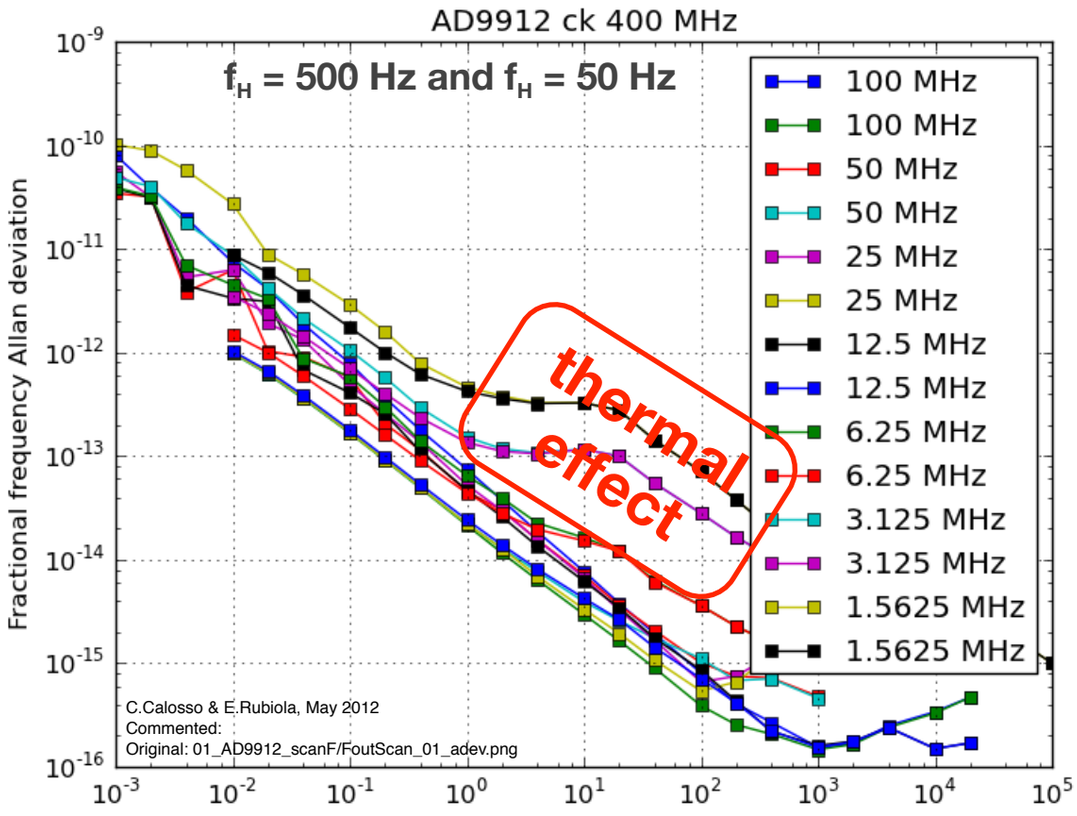


The Λ Divider Versus the DDS





- The Λ divider performs 2×10^{-14} at τ = 1 s, 10 MHz output
- Thermal effects make the DDS worse at τ > 1 s
- The Λ divider is free from thermal effects – at the scale shown



The Bottom Line

- Aliasing in traditional dividers
  - Increases white noise
  - Has little effect on flicker
- Flicker in multi-buffer Π divider not understood yet
- The new Λ divider
  - Is little/no affected by aliasing
  - Exhibits the lowest PM noise

    flicker: $b_{-1} \approx -130$ dB

    white: $b_0 \approx -165$ dB
  - Features 2×10^{-14} at $\tau = 1$ s, 10 MHz output
  - Is free from the thermal effects seen in DDSs at $\tau > 1$ s

home page http://rubiola.org

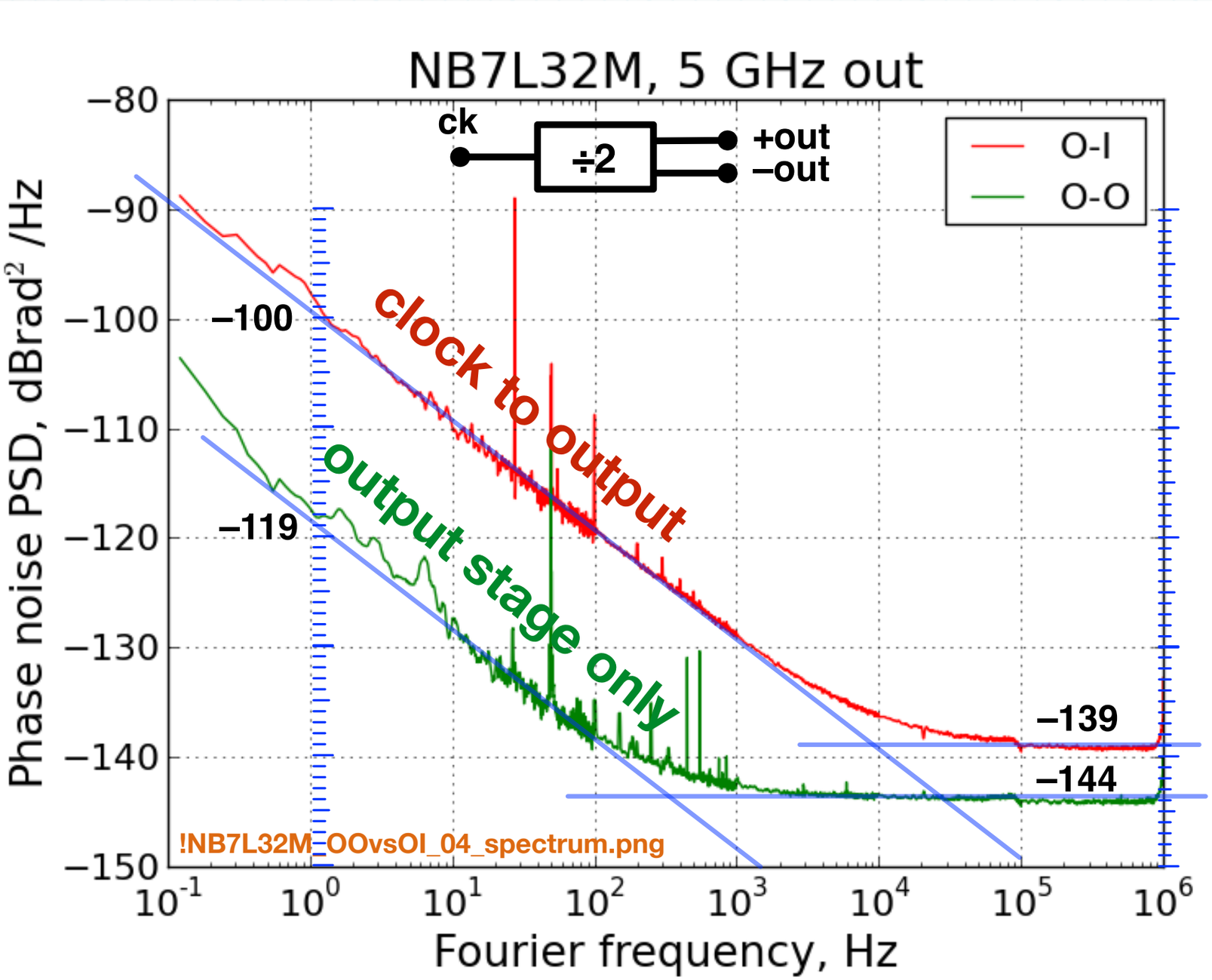
Thanks – J. Groslambert, V. Giordano, M. Siccardi, J.-M. Friedt

Grants from ANR (Oscillator IMP and First-TF network), and Region Franche Comte

Microwave Dividers

NB7L32M ÷2 µWave Divider

10 GHz ÷ 2 = 5 GHz

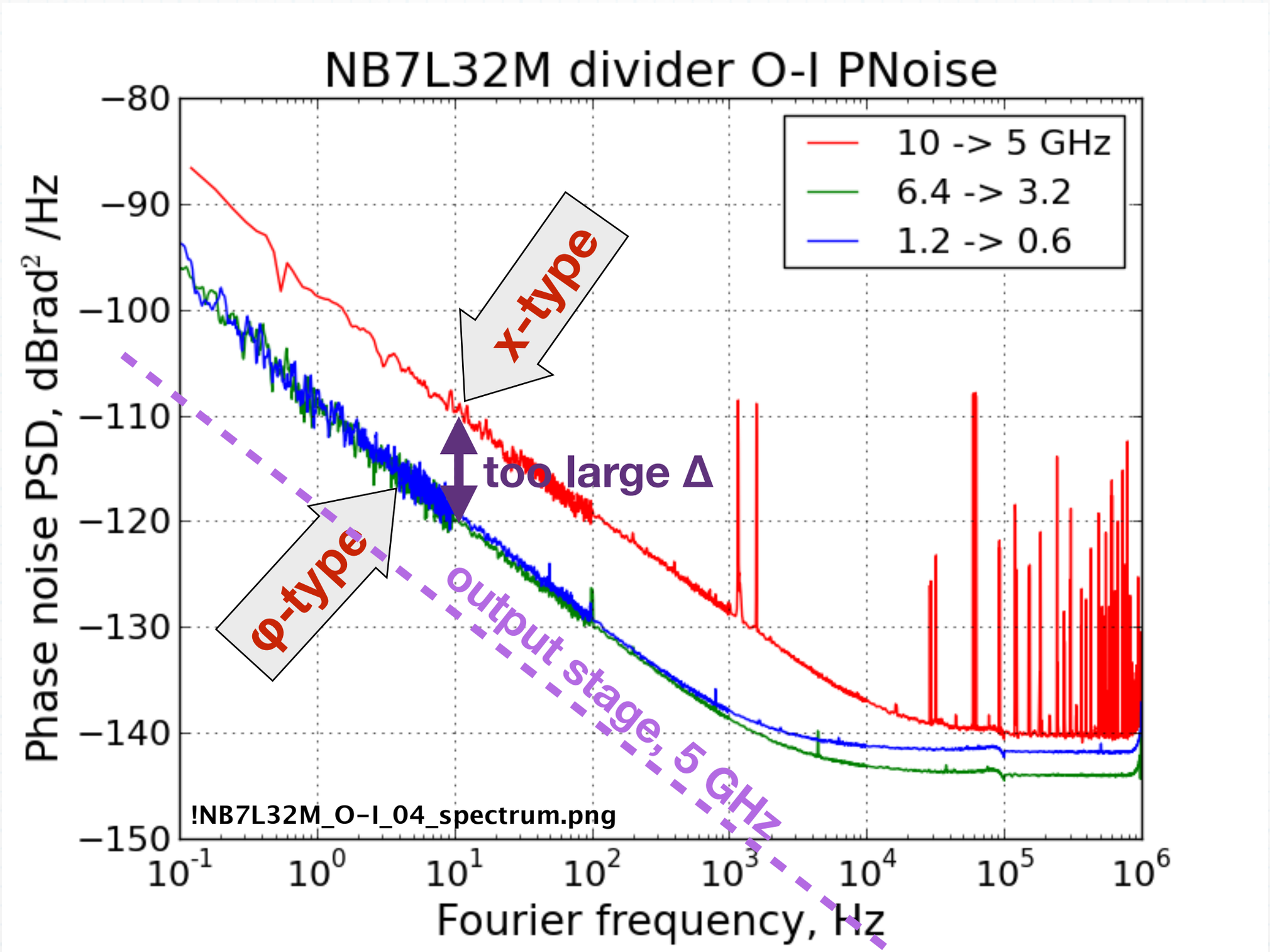


Method

- Compare two dividers
- Use 5.01 GHz as a common oscillator, and beat
- Digital PM noise measurement at 10 MHz
- O-I: Two equal dividers
- O-O: Two outputs of the same divider
- Shown: spectrum of one divider

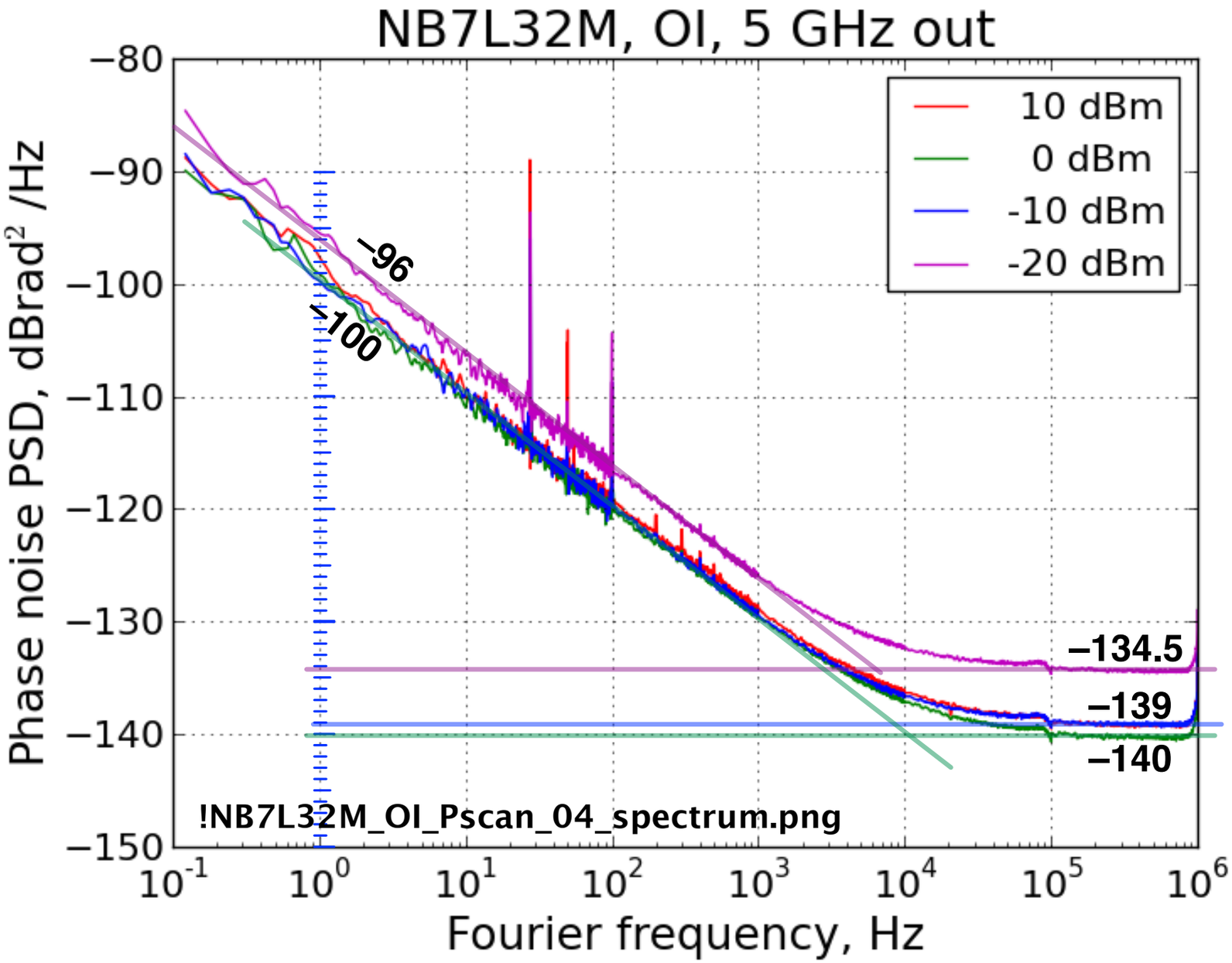
NB7L32M ÷2 µWave Divider

Phase noise vs input frequency



NB7L32M ÷2 µWave Divider

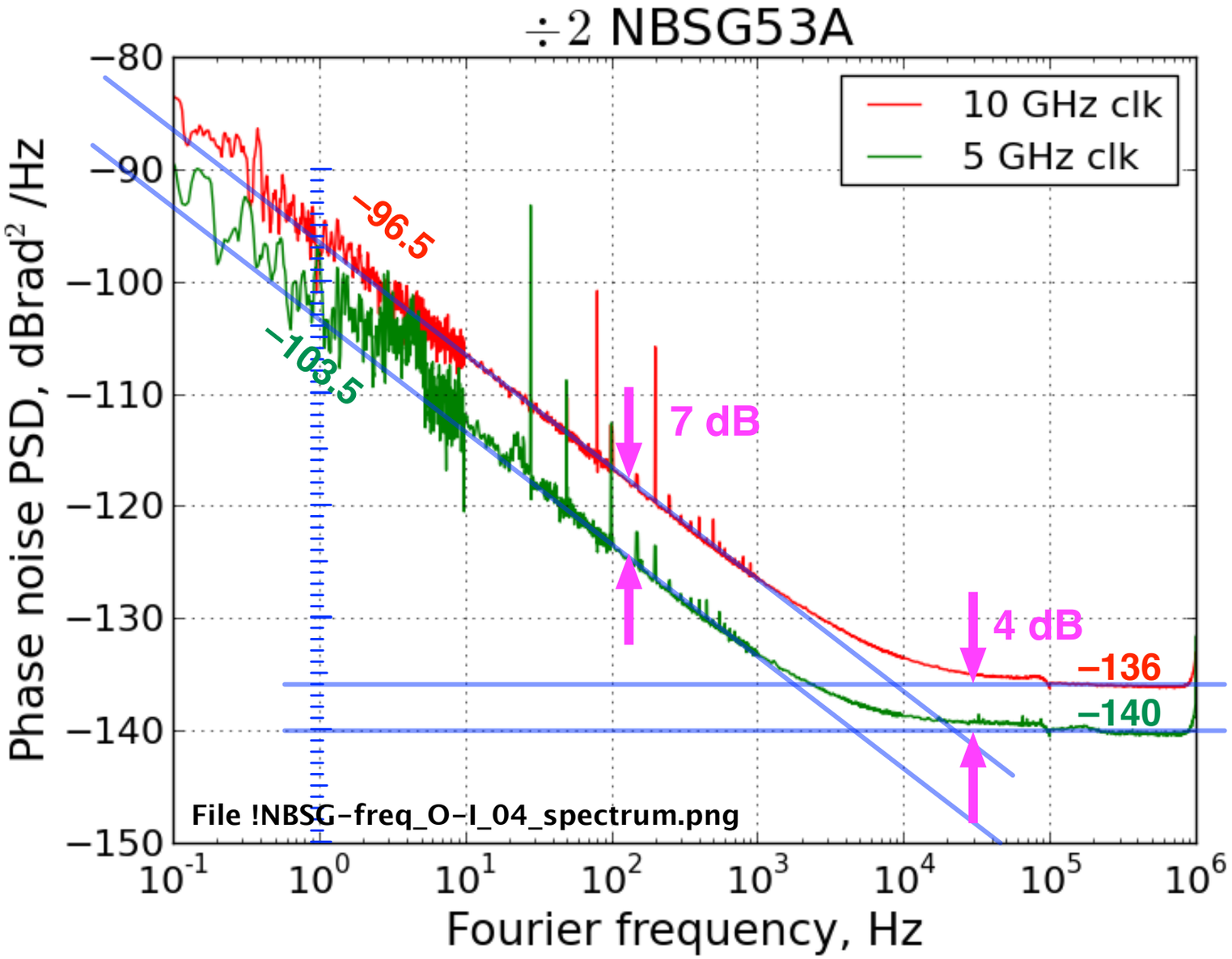
Works fairy well even at low input power (useful)



Notes

- At –16 dBm the white noise increases by 3 dB
- The critical power where $(b_0)_\varphi = (b_0)_x$ is –16 dBm
- Hence $(b_0)_{x\text{-type}} \approx -140$ dB

NBSG53A SiGe ÷2 µWave Divider



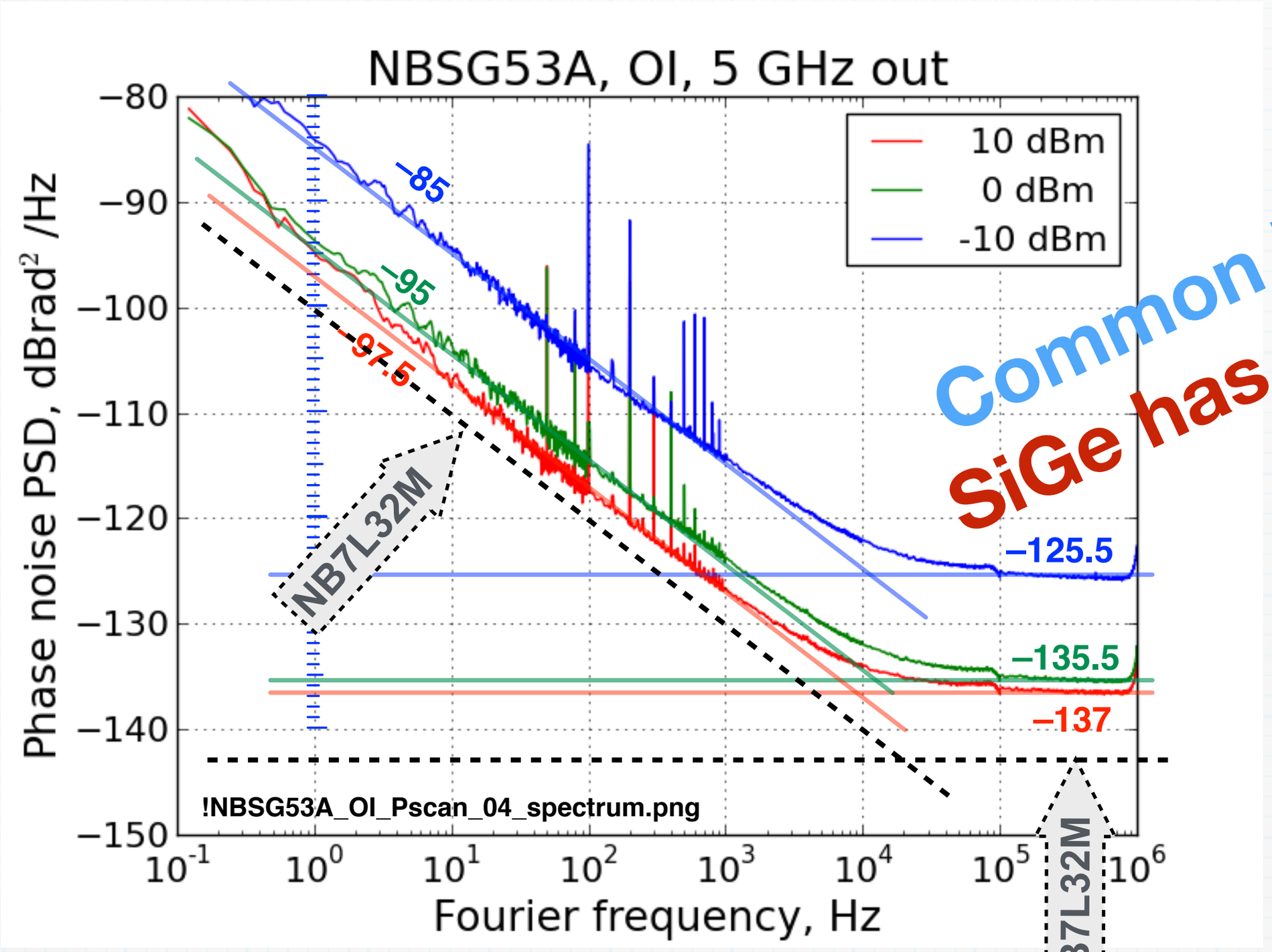
Method

- Use 5.01 (2.51) GHz as a pivot oscillator, and mixers
- Digital PM noise measurement at 10 MHz
- One divider shown

- 1/*f* –> pure gearbox model (as expected)
- White –> aliased gearbox model (as expected)
- Likely, 1 dB discrepancy in w and 1/f (mixer response)

Debugged:
–97.5 and –137

NBSG53A SiGe ÷2 µWave Divider

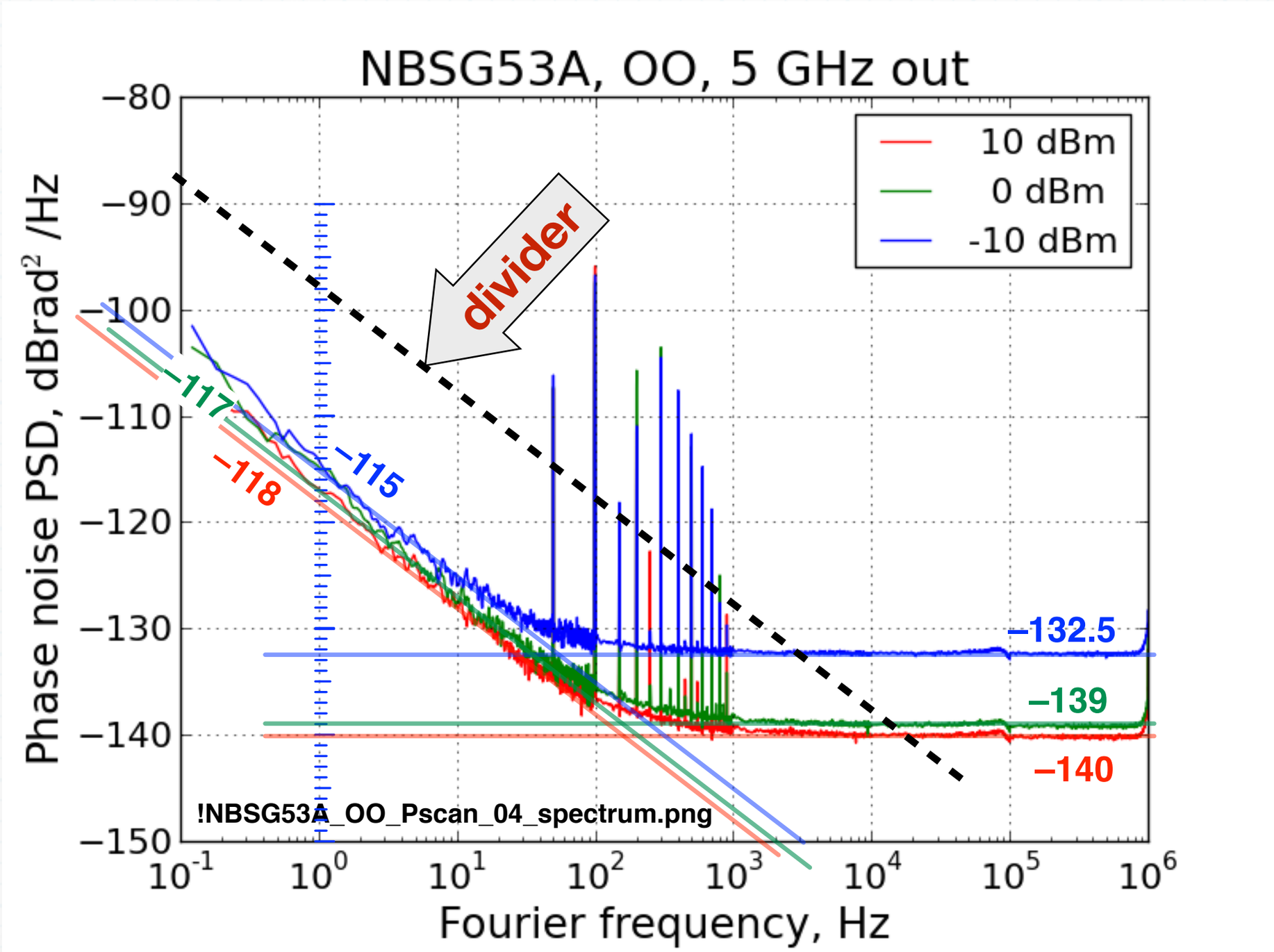


Common belief
SiGe has low 1/f

- Compares unfavorably to the NB7L32M
- More noise and less tolerance to low power

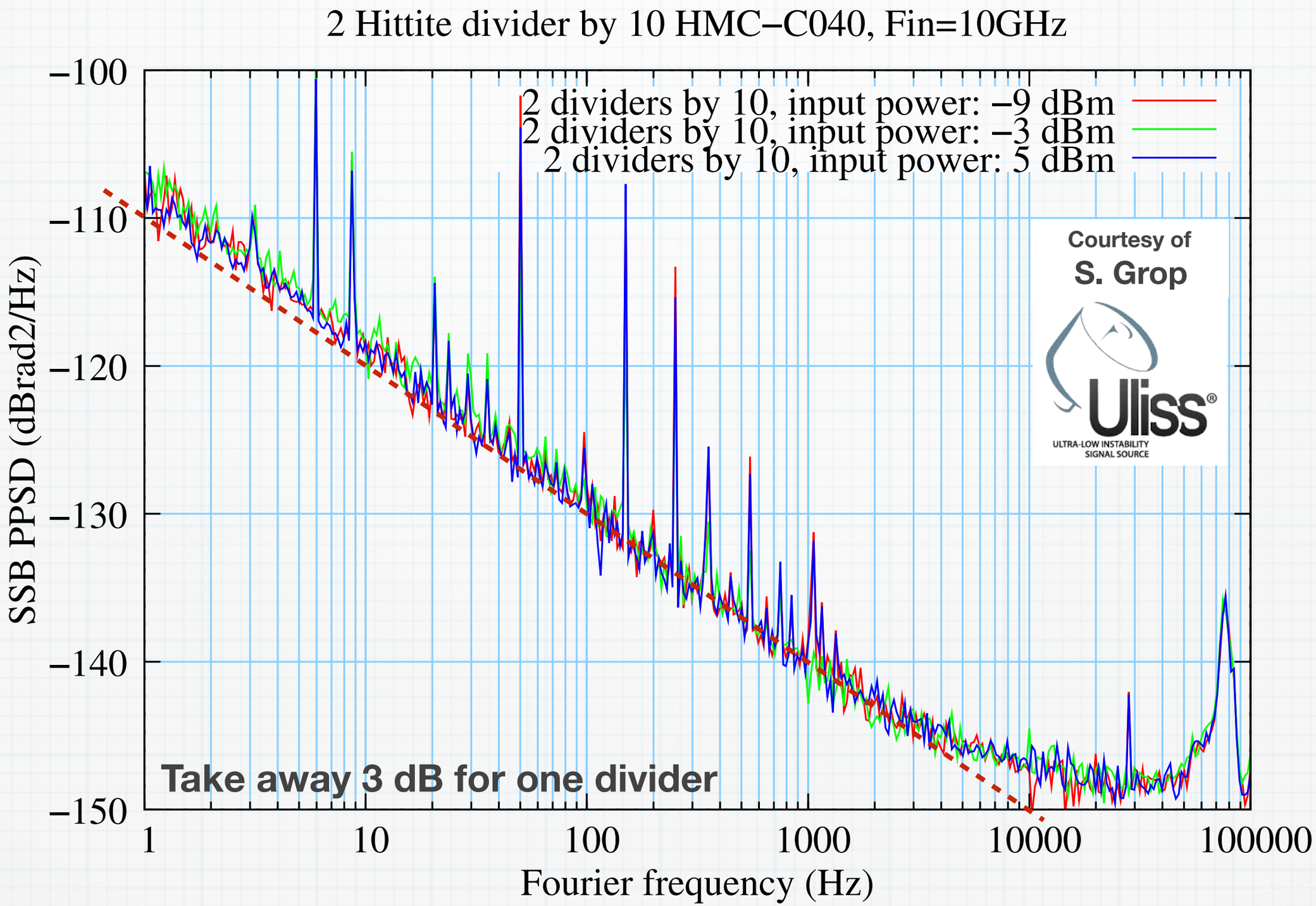
NBSG53A SiGe ÷2 µWave Divider

Output vs Output gives info about the output stage



The problem seems in the gear box, rather in the output stage

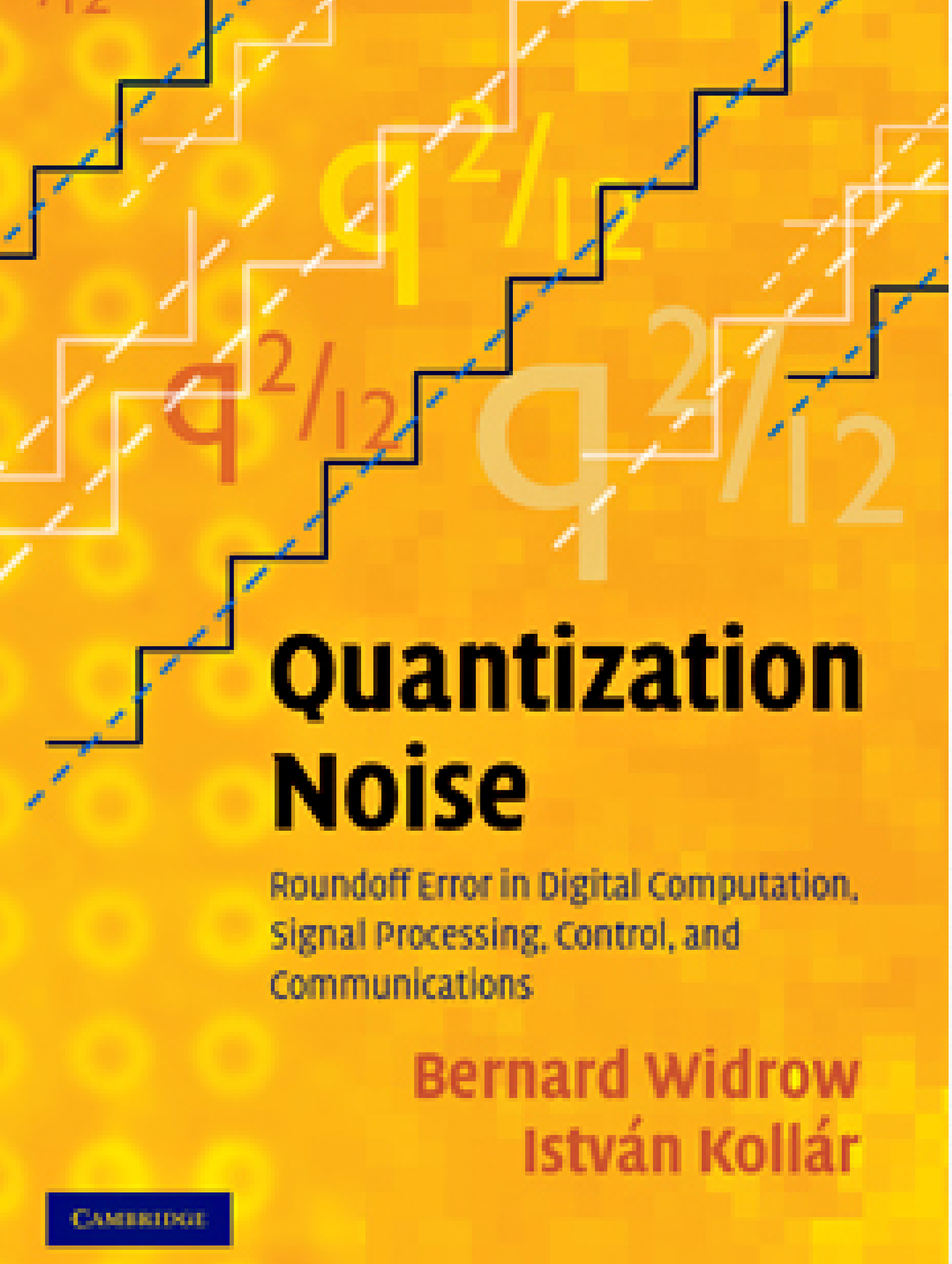
Hittite HMC-C040, ÷10 Divider



Microwave Dividers Compared

	10 GHz ÷2	5 GHz ÷2	2.5 GHz ÷2	lower	
NB7L32M	–100	–109	–109	–109	600 MHz 1.2 GHz ÷2
NBSG53A	97.5	–103.5		–104	800 MHz 1.6 GHz ÷2
HMC-C040				–113	1 GHz 10 GHz ÷10
HMC705LP4				–121	0.5 GHz 2.5 GHz ÷5

Suggested Readings



Suggested Reading

Bernard Widrow, Istvan Kollar

Quantization Noise

Cambridge 2008
ISBN 978-0-511-40990-5

- Chapter 15: **Roundoff noise** in **FIR** digital filters and in **FFT** calculations
- Appendix G: **Quantization of a sinusoidal input**

Suggested Reading

ANALOG-DIGITAL CONVERSION

Walt Kester

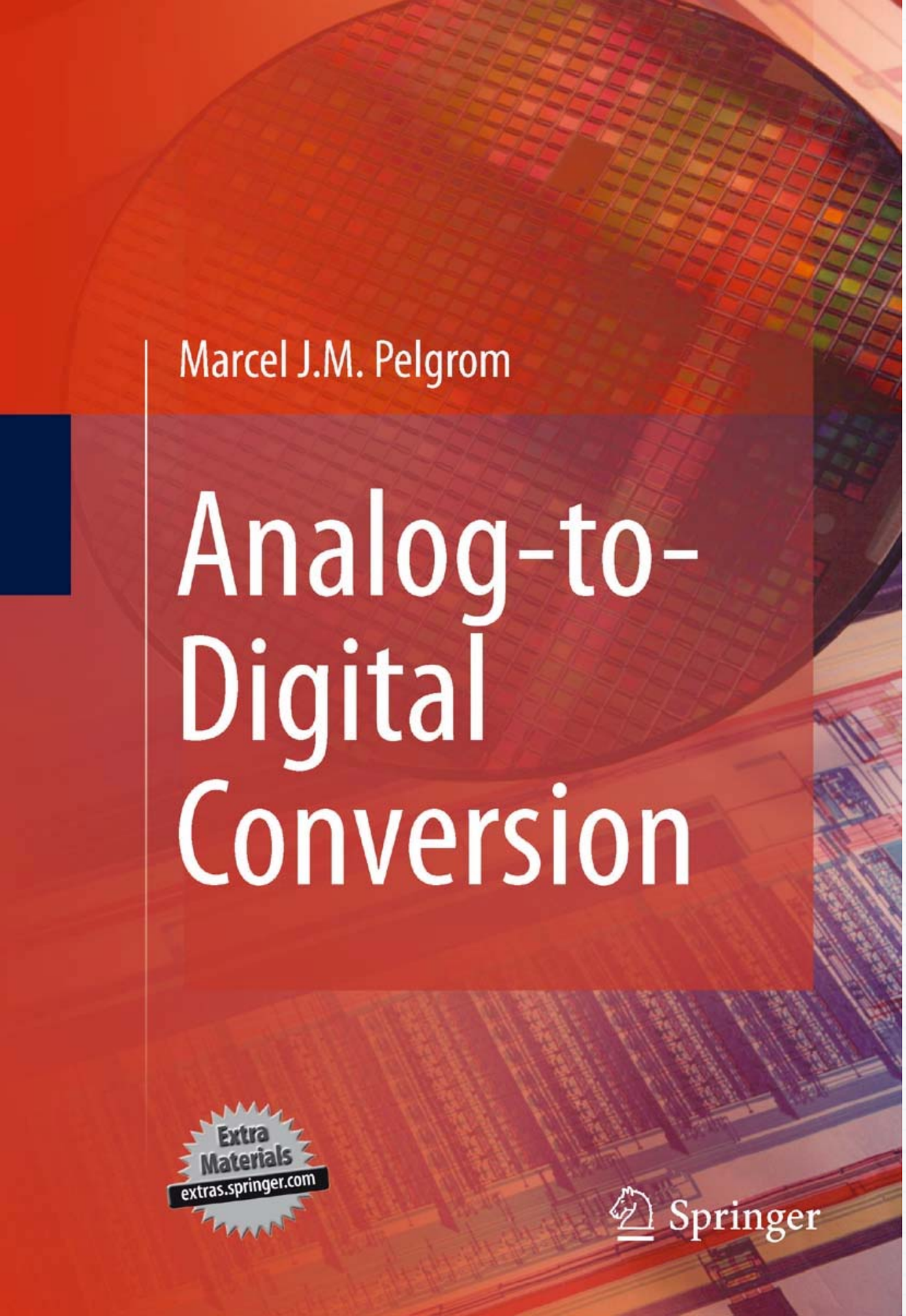
Editor

ANALOG DEVICES

Walt Kester (editor)

Analog-Digital Conversion

Analog Devices 2004
ISBN 0-916550-27-3



Suggested Reading

Marcel J. M. Pelgrom

Analog-to-Digital Conversion

Springer 2010

ISBN 978-90-481-8888-8