Digital Electronics Based on Red Pitaya Platform For Coherent Fiber Links

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***Abstract*— Recent improvements and continuous research on accurate clocks and frequency standards require the study of suitable tools and techniques for frequency transfer that minimize the added noise and allow fully exploiting these clocks in metrology applications. Different experiments performed during the last decade validated fiber links as the most performing tool for frequency transfer, reaching a statistical uncertainty of 10^{-20} for thousands kilometers links [1]. Recently, digital implementations have been used for metrological applications due to the flexibility, cost effective and compact solutions that can be achieved. In this paper, we propose a digital implementation for the detection and compensation of the phase noise induced by the fiber link. The beat note, representing the fiber length variations, is acquired directly with a fast Analog to Digital Converter (ADC) followed by a Tracking Numerical Controlled Oscillator (NCO). This reduces the component's latency and the communication delay between different blocks, increasing the tracking bandwidth. In addition, we report the characterization of the main components that allows foreseeing which are the limiting aspects and the expected performance of the complete implementation. The proposed system is being implemented on Red Pitaya, an open source platform driven by a Zynq, System on Chip (SoC) of Xilinx that contains a FPGA and an ARM processor embedded on the same chip.**

Keywords—Digital Electronics; Fiber Link; FPGA; IIR filter; NCO; PLL; Time and Frequency transfer.

I. INTRODUCTION

The progress achieved on optical clocks along the last years, allowed reaching frequency stability in the 10^{-18} range. In order to exploit such a performance in metrological applications, fiber links are being widely used for frequency transfer and dissemination. However, mechanical and temperature stresses generate fiber length variations and therefore phase fluctuations that have be compensated or cancelled if a degradation of the clock information is not desired. In this regard, different techniques exist: the classical, Doppler compensation [2] and the more recent, two-ways cancellation [3]. In the traditional analog configuration, the fiber noise is detected through, a tracking Voltage Controlled Oscillator (VCO) that cleans up the beat note of two lasers, and a frequency divider that increases the dynamic of the mixer. Afterward, a servo compensates the noise by acting on the frequency that drives the Acousto-Optic Modulator (AOM). This kind of configuration demonstrated to work well [4, 5]. However, it has low flexibility and it is not predisposed naturally for efficient reconfiguration, monitoring and remote operation.

The advantages of a digital implementation on coherent fiber links were demonstrated, for the first time, by C. E. Calosso *et al.*, in [6]. There, the approach is based on the Tracking Direct Digital Synthesizer (DDS) technique, which detects the fiber phase noise directly. The flexibility of this system allowed demonstrating, a 6 dB improvement of the unsuppressed noise limit, and the two-ways scheme, with simple software reconfigurations. The system was usable only up to 47 km, limited by the serial communication of the DDS. For extending its usability to thousand-kilometer link it is necessary to increase the tracking bandwidth from 20 kHz to the megahertz region; that means to redesign the board with parallel communication components.

In this paper we propose an entirely digital implementation, from phase detection to fiber noise compensation. This alternative approach is based on a commercial board that integrates fast ADCs, DACs and a SoC. In addition to the advantages provided by the tracking DDS (monitoring and flexibility), here we exploit the reduction of the communication delay between components that leads to a tracking bandwidth increment, a key point for long links implementation. The work is focused on the critical aspects: latency and resources usage of each functional block implemented in the FPGA and residual noise of the main components. Based on these results, a tracking bandwidth of 2 MHz and a residual frequency stability of 10^{-18} at 1s are expected.

II. TRACKING DDS - PREVIOUS DIGITAL CONFIGURATION

Fig. 1 depicts the Doppler compensation technique using the Tracking DDS approach. A first DDS tracks the phase of the beat note and retrieves the fiber link noise directly. Then, a servo compensates for it by correcting the phase of a second DDS that drives the AOM. This implementation can reach a tracking bandwidth up to 1MHz using parallel communication with the DDS.

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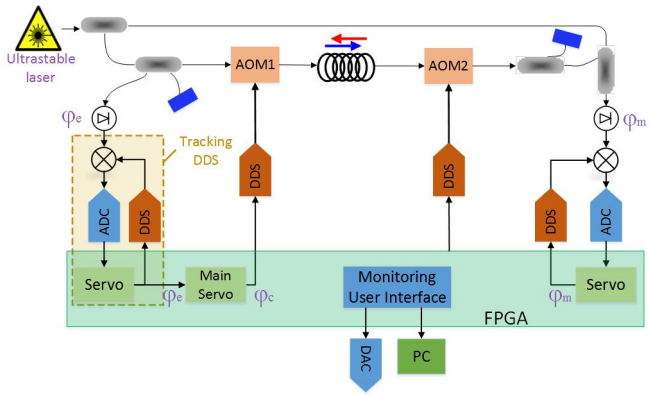

Fig. 1. Doppler compensation implemented by using tracking DDS.

III. Tracking NCO Description

In the proposed implementation (Fig. 2), mixers and DDSs are replaced by digital blocks implemented on the FPGA, simplifying the hardware interconnection. DDSs are replaced by Numerical Controlled Oscillators (NCOs) and analog mixing is performed through a numerical multiplication. The phase is detected using digital I/Q demodulation having access to the quadrature and in-phase components of the beat note, allowing not only detecting phase but also amplitude fluctuations. The high frequency component is removed by a low pass filter, designed for avoiding the loop dynamic reduction.

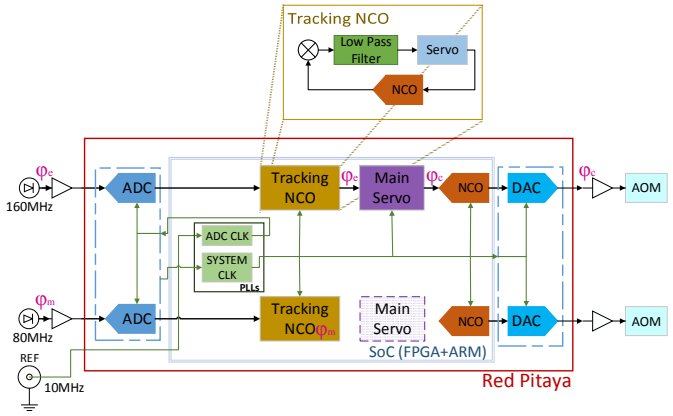

Fig. 2. Description of Tracking NCO block diagram. The phase detector and additional NCOs are implemented on the FPGA. The clock distribution is performed through one of the PLLs provided in the FPGA.

This scheme makes the tracking bandwidth independent of the ADC delay and the data more accessible for monitoring or for additional processing.

IV. Implementation and Characterization

The implementation and characterization of the blocks was performed on Red Pitaya [7], the same platform currently in use for the complete system integration. Such a platform has two fast ADCs of 14 bits and 125MSPs, and two fast Digital to Analog Converters (DACs) of 14 bits and 125MSPs. The SoC, Zynq 7010, integrates in a single device a dual core ARM Cortex-A9 and an Artix-7 FPGA. Red Pitaya runs Linux, which provides, among other features, different protocols for remote connection.

The aim of this preliminary implementation is to characterize the main blocks: ADC, DAC, internal PLL, NCO and low pass filter, in order to test their suitability and contribution level to the performance of the complete system. Furthermore, it allows obtaining the necessary information to foresee the usage of the FPGA resources and to evaluate data latency that impacts directly on the maximum tracking bandwidth. Thereby, the complete system implementation feasibility is verified according to the application requirements.

The ADC characterization is reported in [8]. The parameter of main interest is the additive noise, which for a sinusoid at maximum amplitude results in a pure φ-type phase noise of -103 dBrad^2/Hz at 1Hz (flicker) and of -152 dBrad^2/Hz at 1 MHz (white).

The tracking bandwidth is determined by the delay introduced by the blocks that belong to the tracking loop (Fig. 3), the low pass filter, the servo and the NCO. In order to keep the stability of the loop, the maximum bandwidth is given by (1).

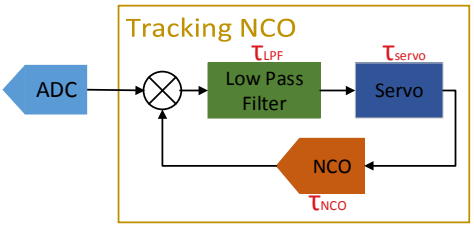

Fig. 3. Description of tracking NCO phase detector. The ADC delay is out of the loop and does not limit the tracking bandwidth.

$$B_{max} = \frac{1}{8\tau_{Tot}}, \quad \tau_{Tot} = \tau_{LPF} + \tau_{servo} + \tau_{NCO} \tag{1}$$

The filter introduces not only delay due to the implementation, but also phase shift related to the filter typology. Both components will be taking into account as filter total delay (τ_{LPF}).

A. Clock Distribution - PLL

In the general scheme for frequency transfer and comparison, an Acousto-Optic Modulator (AOM) is used in the remote laboratory in order to separate reflections from the useful signal. A second AOM, placed in the local laboratory, corrects the fiber noise. In the proposed implementation, the AOMs are driven by the DACs, which in turn, are referred to the board time-base. The same time-base drives the ADCs that detect the phase of the beat notes. As a consequence, the phase noise of the internal time-base adds noise to the link. In this regard, the time-base is obtained from an external reference, taking advantage of the internal PLL of the FPGA.

B. Numerical Controlled Oscillator

The NCO implemented here is based on the DDS IP core provided by Xilinx. The block generates the sine and cosine signals, used for the detection of the quadrature (Q) and in-phase (I) components of the beat note, respectively. The configuration chosen minimizes latency and FPGA resources usage. The NCO has been sized taking into account that the

ADC has 11 effective bits (ENOB=11bits). In order not to degrade the information from the ADC, an output resolution of 16 bits was chosen. In addition, the NCO features 48 bits for phase and frequency, a latency $\tau_{NCO} = 2\ T_{clk} = 16$ ns, and a maximum clock frequency of 460 MHz. It utilizes 72 configurable logic blocks (1.63%) and 54 kb RAM (1.66%).

C. Low Pass Filter

The filter plays an important role for what concerns the maximum tracking bandwidth achievable. Therefore, it was designed to minimize the phase shift and the delay on the signal and, at the same time, without excessive use of the FPGA resources. The typology chosen was an Infinite Impulse Response (IIR) elliptic of third order. The filter implemented has a total delay $\tau_{LPF} = 4.82\ T_{clk} = 38.6$ ns and the transfer function depicted in Fig. 4. The filter specifications, guarantee the rejection of the high frequency component resulting from the multiplication. In this case, due to the sampling frequency this component will be at 70 MHz for φ_e and 90 MHz for φ_m. With respect to the Finite Impulse Response (FIR) implementation, it exhibits much smaller latency and -57% of resources usage. Particular attention has been paid on data resolution to ensure stability to the filter.

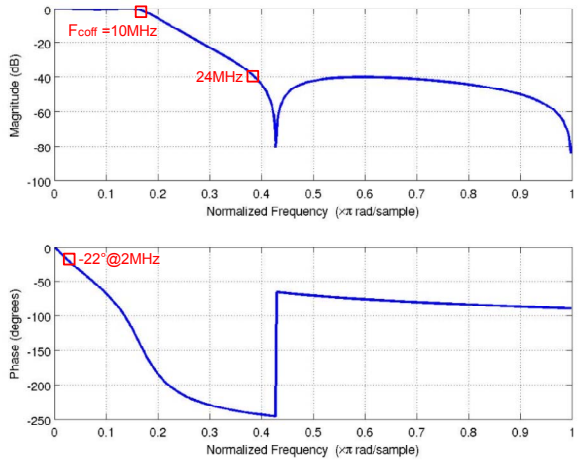

Fig. 4. Low pass filter design specifications. Cut off frequency: 10MHz, stop band attenuation: 40dB. Phase shift added at the desired frequency: 22°.

The features of the filter implemented are: Filter Order: 3, latency: 8 ns, phase shift at the desired tracking bandwidth (2MHz): 22°, output precision: 31 bits fixed point. FPGA Utilization: 0.53% Logic Cells, 12.5% DSPs (Multipliers).

D. Servo

The servo performs a Proportional and Integrative (PI) control in order to correct the phase of the NCO according to the beat note phase. The implementation is based on the architecture performed for the Tracking DDS. The latency added by this block is $\tau_{servo} = 1\ T_{clk} = 8$ ns.

V. Results

The residual phase noise of the two DACs was measured here. The DACs were driven by the NCO outputs at 40 MHz, the value that will be used for driving the AOMs. The result is shown in Fig. 5. It is dominated by flicker noise (b_{-1} = -97 dBrad^2/Hz) that leads to a residual stability of $6.5\text{x}10^{-13}$ at 1s ($f_h = 50$Hz)

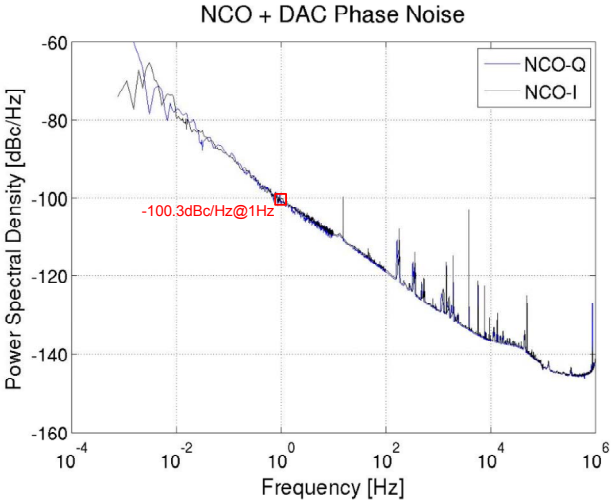

Fig. 5. The main phase noise contribution is added by the DAC.

The residual phase noise of the PLL embedded in the FPGA is shown in Fig. 6.

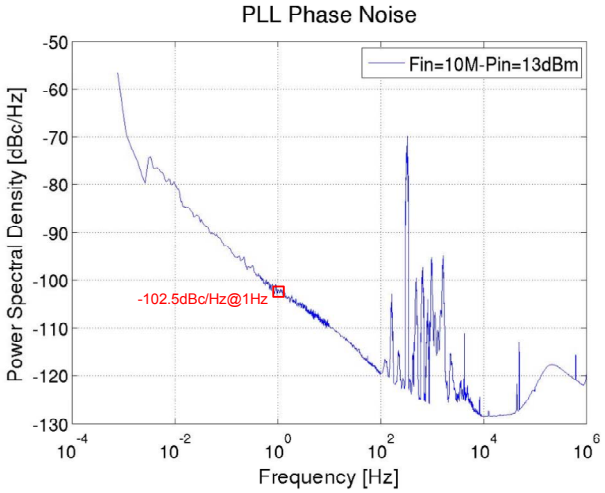

Fig. 6. PLL residual phase noise. Input frequency of 10MHz.

The flicker noise obtained is -99.5 dBrad^2/Hz at 1Hz referred to the reference (10 MHz). The residual stability is $8.8\text{x}10^{-13}$ at 1 s (f_h = 50 Hz). It is the component with the highest noise and limits the overall performance. Nevertheless, we decided to privilege the compactness of the system and to avoid using external frequency multiplier. Thanks to the leverage between RF and optical frequencies, the system is expected to affect the fiber link performance at the level of 10^{-18} at 1s, allowing reaching the 10^{-21} region at 200 s.

Fig. 7 depicts the Allan deviation of the PLL phase noise. The frequency stability expected for the complete system is about 10^{-18} at 1s, close to the frequency stability obtained with the Tracking DDS approach.

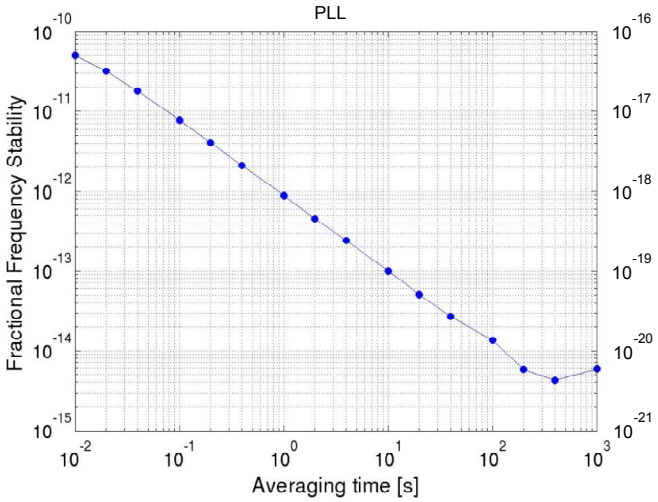

Fig. 7. Allan deviation of the PLL phase noise. Expected frequency stability of the completed system implementation.

The total bandwidth is expected to be 2 MHz according with the results obtained of each block implementation and characterization, compatible with thousand kilometers links.

Thanks to the NCO implementation, the system will have access to the in-phase component which allows performing automatic power compensation on the fiber.

The tracking NCO features a "dead frequencies range" due to the sampling frequency (125 MHz) used for this implementation. For input frequencies close to the sampling clock, the tracking bandwidth is faster than the information and therefore it can not be detected. This can be solved changing the sampling frequency. However, for the first approximation of the system the scheme will remain as it was shown here.

The implementation of the entire system is being performed currently. The electronics will be used on the Italian Link for Frequency and Time from Turin to Florence that is 642-km long [9].

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