Phase Noise and Jitter in Digital Electronics

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Outline

• Basics
• FPGAs — Mechanisms / Examples / Facts
• ADCs — Basics / Examples
• DDSs — Basics / Advanced / Examples
• Dividers — Π and Λ / Microwave

home page http://rubiola.org
Acknowledgments

This tutorials gathers a wealth of (mostly unpublished) material developed by

The Go Digital Team@ FEMTO-ST, Besancon, F

chiefly

Pierre-Yves “PYB” Bourgeois
Gwenhael “Gwen” Goavec-Merou
Jean-Michel Friedt
Yannick Gruson

Claudio Calosso, INRIM, Torino, Italy

...and myself

Caveat

Only a fraction of this can be taught at a 1–2 H session
1 – Basics
Jitter

ITU defines jitter as the variations in the significant instants of a clock or data signal, vs a “perfect” clock

- Jitter —> Usually fast phase changes $f >$ a few tens of Hz
- Wander —> Usually slower phase changes (due to temperature, voltage, etc)

Designers first care about consistency of logic functions,

- First, maximum timing error
- Sometimes RMS value and probability distribution

Time and Frequency community focuses on

- PM noise spectra
- Delay spectra
- Two-sample variances (ADEV, TDEV, etc.)

\[
v(t) = V_0 [1 + \alpha(t)] \cos [2\pi v_0 t + \varphi(t)] \quad x(t) = \frac{\varphi(t)}{2\pi v_0}
\]
Phase Time \( x(t) \) — or Jitter

- Let’s allow \( \varphi(t) \) to exceed \( \pm \pi \), and count the no of turns.
- This is easily seen by scaling \( \omega \) down (up) to \( \omega = 1 \text{ rad/s} \) using a noise-free gear work.
- The phase-time fluctuation associated to \( \varphi(t) \) is
  \[
  x(t) = \frac{\varphi(t)}{\omega_0}
  \]
- \( x(t) \) is a normalized quantity, independent of \( \omega_0 \).
Physical Concept of PSD $S(f)$

Power Spectral Density

- The PSD is the distribution of power vs. frequency (power in 1-Hz bandwidth).
- The PS is the distribution of energy vs. frequency (energy in 1-Hz bandwidth).
- Frequency can be continuous or discrete (histogram),
- In mathematics,
  - the power is a square quantity
  - the energy is power integrated in time
- Power (energy) in physics is a square (integrated) quantity
  - PSD $\rightarrow$ W/Hz (or V²/Hz, A²/Hz, etc.)
  - PS $\rightarrow$ J/Hz

See Nelson's talk
The Polynomial Law

\[ v(t) = V_0 [1 + \alpha(t)] \cos [2\pi \nu_0 t + \varphi(t)] \]

Phase Noise

\[ S_{\varphi}(f) = \sum_{i \leq -4} b_i f^i \]

Jitter (phase-time) PSD

\[ x(t) = \frac{\varphi(t)}{2\pi \nu_0} \]

\[ S_x(f) = \sum_{i \leq -4} k_i f^i \]

Fractional Frequency PSD

\[ y(t) = \dot{x}(t) = \frac{\dot{\varphi}(t)}{2\pi \nu_0} \]

\[ S_y(f) = \sum_{i \leq -2} h_i f^i \]

See Nelson's talk.
Converting PM noise to TDEV

You may be more familiar to $\sigma_y^2(\tau) = h_0/2\tau + 2\ln(2)h_{-1}$

$\sigma_x(\tau) = \frac{2 \ln(2) b_{-1}}{(2\pi \nu_0)^2}$

$\sigma_x^2 = \frac{b_0}{2(2\pi \nu_0)^2 \tau}$

$\varphi(t)$

phase-time (fluctuation)

$\chi(t) = \frac{\varphi(t)}{2\pi \nu_0}$

random phase

TDEV $\sigma_x(\tau)$

same as ADEV, but we use $x(t)$ instead of $y(t)$
Phase Noise Sampling

- Sampling occurs at the edges
  - (in some cases, only at rising or falling edges)
- Square wave signals need analog bandwidth at least
  \[ 3 \nu_{\text{max}} \ldots 4 \nu_{\text{max}} \]
- Aliasing is expected

Saturated analog gain

Equivalent sampling function

Variance \[ \sigma_x^2 = \mathbb{E}\{x^2\} \]

Input sampling frequency \[ 2\nu_0 \longrightarrow \text{noise bandwidth} \ B = \nu_0 \]
• The Parseval Theorem states that the total energy (or power) calculated in the time domain and in the frequency domain is the same.

• Ergodicity allows to interchange time domain and statistical ensemble.

\[ \sigma^2 = N B \]

\[ N'B' = N''B'' \]

...and PM noise scales up with the reciprocal of the carrier frequency.
Aliasing and $1/f$ Noise

Low power in the high-$f$ aliases

Little or no effect on the noise spectrum

And virtually no effect with $1/f^2$, $1/f^3$, $1/f^4$ ...
2 – FPGAs

- Noise Mechanisms
- Examples
- Additional Facts
Noise Mechanisms
FPGA Interconnection Structure

- Delay & jitter
  - General routing through switch points
  - Delay & jitter rather uniform in a block
  - Large spread over the interconnect matrix
  - Dedicated clock lines managed separately
  - Low and predictable delay & jitter

Device dependent blocks
- Input/Output
- RAM
- PLL
- NCO
- …etc.
Output Jitter Limitations

• Output can be synchronized to the clock

• Jitter cannot be smaller than
  • External clock signal
  • Clock input stage
  • Clock distribution
  • Output stage
Phase Noise in the Input Stage

Threshold fluctuation

\[ v_{in} \]

\[ v_{out} \]

threshold noise \( n(t) \)

phase noise \( \varphi(t) \)

\[ \text{slope} \]

\[ \text{SR} = \frac{dv}{dt} \]

actual threshold

nominal threshold

error \( x(t) \) = \( n(t) / \text{SR} \)

\[ t \]

\[ t \]

mechanism

\[ x(t) = \frac{n(t)}{(SR)(t)} \]

\[ \varphi(t) = \frac{2\pi \nu_0 n(t)}{(SR)(t)} \]
Phase Noise in the Input Stage

Sinusoidal signal

\[ v(t) = V_0 [1 + \alpha(t)] \cos [2\pi \nu_0 t + \varphi(t)] \quad \Rightarrow \quad SR = 2\pi \nu_0 V_0 \]

\[ x(t) = \frac{n(t)}{SR} \quad \Rightarrow \quad x(t) = \frac{1}{2\pi \nu_0} \frac{n(t)}{V_0} \]

\[ \varphi(t) = \frac{2\pi \nu_0 n(t)}{SR} \quad \Rightarrow \quad \varphi(t) = \frac{n(t)}{V_0} \]

\[ S_{\varphi}(f) = \frac{S_n(f)}{V_0^2} \]

\( \varphi \)-type noise (constant vs \( \nu_0 \))
\( \varphi\)-type PM Noise

Remember that white noise is subject to aliasing, flicker is not

\[
S_\varphi(f) = \frac{S_n(f)}{V_0^2}
\]

pure \( \varphi\)-type

\[
S_\varphi(f) = \sum h_i f^i
\]  
[do not mistake with \( S_y(f) \)]

aliased \( \varphi\)-type

\[
S_\varphi(f) = \frac{B}{\nu_0 V_0^2} S_n(f)
\]

corner \( f_c = \frac{\nu_0}{B} \frac{h_{-1}}{h_0} \)
**φ-type Jitter**

\[ S_x(f) = \frac{S_n(f)}{(2\pi \nu_0 V_0)^2} \]

- **Pure φ-type**
  \[ S_x(f) = \frac{S_n(f)}{(2\pi \nu_0 V_0)^2} \]
  - Line: \[ h_{-1}/f \]
  - Spectral density: \[ k_{-1}/f \]

- **Aliased φ-type**
  \[ S_x(f) = \frac{B}{\nu_0} \frac{S_n(f)}{(2\pi \nu_0 V_0)^2} \]
  - Line: \[ h_0 \]
  - Spectral density: \[ k_0 \]
  - Spectral density: \[ \sim 1/\nu_0^3 \]
  - Spectral density: \[ \sim 1/\nu_0^2 \]

**Power Law**

\[ S_x(f) = \sum k_i f^i \]
\[ S_n(f) = \sum h_i f^i \]
Internal Delay Fluctuation

x-type noise

• The internal delay fluctuates by an amount $x(t)$

• This has nothing to do with threshold and frequency
x-type Jitter

Remember that white noise is subject to aliasing, flicker is not.

\[ S_x(f) = \begin{cases} 
  \frac{k_{-1}}{f} & \text{pure x-type} \\
  \frac{1}{\nu_0} \langle x^2 \rangle & \text{aliased x-type} 
\end{cases} \]

\[ f_c = \frac{\nu_0 k_{-1}}{\langle x^2_w \rangle} \]

Power law \( S_x(f) = \sum k_i f^i \)
Remember that white noise is subject to aliasing, flicker is not.
The $\varphi$-type noise noise may show up or not, depending on input noise and SR.

At the comparator out, the edges attain full SR and bandwidth of the technology.

Complex distribution $\rightarrow$ independent fluctuations add up:

$$x(t) = \sum_i x_i(t) \quad \text{and} \quad \langle x^2(t) \rangle = \sum_i \langle x_i^2(t) \rangle$$
Full Noise Mechanism

### Flicker (not aliased)

\[
S_\varphi(f) = \frac{b_{-1}}{f}
\]

\[
S_x(f) = \frac{k_{-1}}{f}
\]

### White (aliased)

\[
S_\varphi(f) = b_0
\]

\[
S_x(f) = k_0
\]
## Summary of the Noise Types

<table>
<thead>
<tr>
<th>Noise class</th>
<th>Dependence on $\nu_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$S_\varphi(f)$</td>
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<tr>
<td>Pure $\varphi$-type</td>
<td>$C$ vs. $\nu_0$</td>
</tr>
<tr>
<td>Aliased $\varphi$-type</td>
<td>$1/\nu_0$</td>
</tr>
<tr>
<td>Pure $x$-type</td>
<td>$\nu_0^2$</td>
</tr>
<tr>
<td>Aliased $x$-type</td>
<td>$\nu_0$</td>
</tr>
</tbody>
</table>

- **Pure $x$-type.** High speed circuits, inside the device. Must be $1/f$, otherwise aliasing shows up.
- **Aliased $x$-type.** High speed circuits, inside the device, at low switching frequency. The clock must be either high frequency sin(), or sharp square wave, so that the threshold has no effect.
Noise Types and AVAR

High frequency

- $\sigma_y^2(\tau)$ indep. of $\nu_0$
- $h_1$ indep. of $\nu_0$
- $b_{-1} \sim \nu_0^2$
- pure x type

Low frequency

- $\sigma_y^2(\tau) \sim 1/\nu_0^2$
- $h_1 \sim 1/\nu_0^2$
- $b_{-1} = C$ vs. $\nu_0$
- pure $\varphi$ type

Graph showing CYCIll, ck. buff., out vs in. with different frequencies:

- 3.125 MHz
- 400 MHz

Low frequency data points:
- 400MHz
- 200MHz
- 100MHz
- 50MHz
- 25MHz
- 12.5MHz
- 6.25MHz
- 3.125MHz
Examples

Measurements are performed with the Symmetricom (Microsemi) DS 5125 and DS 5120 dual-channel phase meter.
Cyclone III Clock Buffer

**Flicker**
- High $v_0$ $\rightarrow$ scales as $v_0$ (x-type)
- Low $v_0$, $\rightarrow$ to $\varphi$-type (bumps 0.1–10 Hz)

**White**
- Aliasing shows up at low $v_0$
Cyclone III Output Buffer

Double buffer, Out vs Out

Phase noise PSD, dB/Hz

-160 -140 -120 -100 -80

10^0 10^1 10^2 10^3 10^4

Fourier frequency, Hz

3.125 MHz
6.25 MHz
12.5 MHz
25 MHz
50 MHz
100 MHz
200 MHz
400 MHz

x-type

φ-type at lower ν?
- Flicker region → Negligible aliasing
- The Π divider is still not well explained
- The Λ divider exhibits low 1/f and low white noise
• Slope $1/\tau$, typical of white and flicker PM noise

• The $\Lambda$ divider performs $2 \times 10^{-14}$ at $\tau = 1$ s, 10 MHz output
Max V CPLD [180 nm]

We do not trust this spectrum (bump -> supply voltage?)

- Two lambda dividers
- output-to-output and common clock,
- low $f$, emphasizes the 1/f noise
- Same, only output-to-output and common clock

![Graph showing phase noise PSD]
Max V CPLD [180 nm]

We do not trust this spectrum (bump → supply voltage?)

- Two lambda dividers
- output-to-output and common clock,
- low $f$, emphasizes the $1/f$ noise
- Clock, difference between the two outputs
Cyclone II Λ Divider [90 nm]
Cyclone II Clock Buffer [90 nm]
Zynq (28 nm), Λ Divider

Zynq (28 nm) ÷10 Λ divider, 100 MHz Æ 10 MHz

Phase noise PSD, dBrad² /Hz

Sφ(1Hz) = -101.12 dBrad² /Hz

Fourier frequency, Hz
74S140 – Old TTL 50 Ω Driver

SN744S140N. 10 dBm

Phase noise PSD, dB(πrad)^2/Hz

-160 -150 -140 -130 -120 -110 -100 -90

10^{-1} 10^0 10^1 10^2 10^3 10^4 10^5 10^6

Fourier frequency, Hz

30MHz 15MHz 7.5MHz 3.75MHz

aliased-φ

φ-type

X-type
Some Facts
Related to Phase and Noise

- Volume Law
- Input Chatter
- Internal PLL
- Thermal Effects
- ......
• Flicker coeff $b_{-1}$ is $\approx$ independent of power
• The flicker of a branch is not increased by splitting the input power
• The carrier adds up coherently, the phase noise adds up statistically
• Hence, the $1/f$ phase noise is reduced by a factor $m$

Gedankenexperiment
- Flicker is of microscopic origin (Gaussian $\rightarrow$ central limit theorem)
- Join the $m$ branches of a parallel device forming a compound
- $1/f$ PM is proportional to the inverse size of the active region
The Volume Law!

- Zynq 28 nm
- Cyclone II 90 nm
- Cyclone III 65 nm
- Max V 180 nm
- Max 3000 300 nm

Exact 1/V law -30 dB/dec (Residuals 3.2 dB rms)

-26.2 dB/dec (Residuals 3 dB rms)

Bad experim. conditions, discarded

Phase noise at 1 Hz, dB/rad^2/Hz

Flicker coefficient b^-1

Technology, nm

Log scale
Input Chatter (1/3)

Chatter occurs when the RMS Slew Rate of noise exceeds the slew rate of the pure signal.

**Pure signal**

\[ v(t) = V_0 \cos(2\pi\nu_0 t) \]

\[ \text{SR} = 2\pi\nu_0 V_0 \]

**Wide band noise**

\[ \langle \text{SR}^2 \rangle = 4\pi^2 \int_0^B f^2 S_V(f) \, df \]

\[ = \frac{4\pi^2}{3} \sigma_V^2 B^2 \quad \text{(rms)} \]

**Chatter threshold**

\[ \nu_0^2 = \frac{1}{3} \frac{S_V B^3}{V_0^2} \]

**Example**

- \( V_0 = 100 \text{ mV peak} \)
- 10 nV/√Hz noise
- 650 MHz max -> 2 GHz noise BW
- Chatter threshold\( \nu = 5.2 \text{ MHz} \)

**With high-speed devices, chatter can occur at unexpectedly high frequencies**
Simulation of Chatter (2/3)

**Conditions**

\(v_0 = 1\) Hz, \(V_0 = 1\) V\_peak \(\sqrt{\langle v_0^2 \rangle} = 10\) mV rms noise

Noise BW increases in powers of 2

De-normalize for your needs
Input Chatter – Example (3/3)

Good agreement with theory

Experiment
- Cyclone III FPGA
- Estimated noise 10 nV/√Hz
- Estimated BW 2 GHz

\[ V_0 = 50 \text{ mV} \ (100 \text{ mV}_{\text{pp}}) \]
\[ v_0 = 4.7 \text{ MHz} \]

\[ V_0 = 100 \text{ mV} \ (200 \text{ mV}_{\text{pp}}) \]
\[ v_0 = 4.7 \text{ MHz} \]

Asymmetry shows up
Explanation takes a detailed electrical model, which we have not
A Λ divider (inside the FPGA) enables the measurement

- The divider noise is low enough
- A trick to work at low frequency
Cyclone III Internal PLL (2/4)

- Low-Q LC oscillator ($Q \approx 10$), 0.6–1.3 GHz
- Optional $\div 2$ always present
- We set $D = 1$ (for lowest noise)
- QUARTUS decides $C$ and $N$
Cyclone III Internal PLL (3/4)

PLL used as a buffer

Crossover between phi-type and x-type at 20 MHz

- φ-type
  16 μrad/√Hz @ 1 Hz
- x-type
  220 fs/√Hz @ 1 Hz

x-type -> analog noise in the phase detector
Cyclone III Internal PLL (4/4)

PLL used as a frequency multiplier

- **1/f** phase noise is dominant
- Scales as $N^2$ -> analog noise in the phase detector

**Graph:**
- **Phase noise PSD, dBrad^2/Hz**
- **Fourier frequency, Hz**
- **Stability**
  - $1.5 \times 10^{-12}$ @ 1 s
  - $(f_H = 500 \text{ Hz})$
  - $-115 \text{ dB} + 20 \log_{10}( \nu_0 )$ in MHz

**Diagrams:**
- **CYCIII PLL, 10 MHz ext. ck.**
- **File:** CYCIII-PLL-Multiplier
  - E.Rubiola, C.Calosso, Sept 2014
- **File:** CYCIII-PLL-Scheme
  - VCO
  - phase detect
  - $\div N$
  - $\div C$
  - 2
  - optional mux
  - $\nu_{\text{VCO}}$
  - lock
  - mix
  - $\nu_i$
  - $\pm D$
  - phase detect
  - $\nu_o$
Thermal Effects (1/3)

Principle
• FPGA dissipation change $\Delta P$ by acting on frequency
• Energy $E = CV^2$ dissipated by the gate capacitor in a cycle

Conditions
• Cyclone III used as a clock buffer
• Environment temperature fluctuations are filtered out with a small blanket (necessary)
• Two separate measurements (phase meter and counter) → trusted result

Outcome
(1) Thermal transient, due to the change of the FPGA dissipation
(2) Slow thermal drift, due to the environment
(3) Overall effect of $\Delta P$
Warning: In real applications, other parts of the same FPGA impact on the temperature, thus on phase – drift is possible
Thermal Effects (3/3)

Cyclone III clock buffer

File: Cyclone-III-adev-VS-Idle-time-H
C.Calosso, E.Rubiola, Aug 2014

A: contiguous runs

B: 1H idle time between runs

Bump due to the residual temperature of the previous run

No significant bump if the measurement is delayed by 1 H after switching $v_0$. 
Cyclone III, Voltage Supply

- All but one low-noise voltage supplies
- The noise is critical only in the core supply
Threshold-Noise Measurement

- Keep the logic at the threshold, where it shows analog gain
- Measure the voltage (current) fluctuation needed to stabilise at the threshold
- Works only on simple (old) circuits
- Threshold-mismatched cascade \(\rightarrow\) gain not accessible
- FPGAs complexity make the analog gain inaccessible
3 − ADCs
Basics
is very important to remember that the actual transfer characteristic is not a line, but a number of discrete points.

Figure 2.15: Transfer Functions for Ideal 3-Bit DAC and ADC

The input to an ADC is analog and is not quantized, but its output is quantized. The transfer characteristic therefore consists of eight horizontal steps. When considering the offset, gain and linearity of an ADC we consider the line joining the midpoints of these steps—often referred to as the code centers.

For both DACs and ADCs, digital full-scale (all “1”s) corresponds to 1 LSB below the analog full-scale (FS). The (ideal) ADC transitions take place at ½ LSB above zero, and thereafter every LSB, until 1½ LSB below analog full-scale. Since the analog input to an ADC can take any value, but the digital output is quantized, there may be a difference of up to ½ LSB between the actual analog input and the exact value of the digital output. This is known as the quantization error or quantization uncertainty as shown in Figure 2.15. In ac (sampling) applications this quantization error gives rise to quantization noise which will be discussed in Section 2.3 of this chapter.

As previously discussed, there are many possible digital coding schemes for data converters: straight binary, offset binary, 1’s complement, 2’s complement, sign magnitude, gray code, BCD and others. This section, being devoted mainly to the analog issues surrounding data converters, will use simple binary and offset binary in its examples and will not consider the merits and disadvantages of these, or any other forms of digital code.

The examples in Figure 2.15 use unipolar converters, whose analog port has only a single polarity. These are the simplest type, but bipolar converters are generally more useful in real-world applications. There are two types of bipolar converters: the simpler is merely a unipolar converter with an accurate 1 MSB of negative offset (and many converters are arranged so that this offset may be switched in and out so that they can be used as either unipolar or bipolar converters at will), but the other, known as a sign-magnitude converter is more complex, and has N bits of magnitude information and an additional bit which corresponds to the sign of the analog signal. Sign-magnitude DACs are quite rare.

Spectrum of the Quantization Noise

The analog-to-digital converter introduces a quantization error $x$, $-V_q/2 \leq x \leq +V_q/2$

Ergodicity suggests that the quantization noise can be calculated statistically

$$\sigma^2 = \frac{V_q^2}{12}$$

The Parseval theorem states that energy and power can be evaluated by integrating the spectrum

$$N B = \frac{V_q^2}{12}$$

Changing $B$ in geometric progression (decades) yields naturally $1/B$ (flicker) noise

$$N = \frac{V_q^2}{12B}$$

$1/12$ is $-10.8$ dB
Quantization & Sinusoidal Signals

SNR = \((3/2) \, 2^{2m}\)

6.02 m + 1.76 dB

---

**Signal power**

\[ P_0 = \frac{V_{PP}^2}{8} = \frac{A^2 V_{FSR}^2}{8} \]

**Noise power**

\[ \sigma^2 = \frac{V_{lsb}^2}{12} \]

**Parseval theorem**

\[ S_V = \frac{\sigma^2}{B \cdot \frac{1}{2} f_s} \Rightarrow S_V = \frac{V_{lsb}^2}{6 f_s} \]

**Phase noise** \( S_{\phi} = b_0 \) (white)

\[ b_0 = \frac{S_V}{P_0} \Rightarrow b_0 = \frac{V_{lsb}^2}{V_{FSR}^2} \cdot \frac{4}{3 A^2 f_s} \]

\[ b_0 = \frac{1}{(2^m)^2} \cdot \frac{4}{3 A^2 f_s} \]

Approximation (fairly large \( V_p \))

\[ A^2 = 2/3 (-1.8 \text{dB}) \Rightarrow b_0 \approx \frac{1}{(2^m)^2} \cdot \frac{2}{f_s} \]

---

Warning: We assume that the noise power is equally distributed in 0 dB. This is not true in our case because samples and carrier are highly coherent. See Widlar, Koller, Appendix G for details. Anyway, we temporarily accept the uniform distribution, hoping that the reality is not too far.
Phase Noise

\[ b_0 = \frac{1}{(2^M)^2} \frac{4}{3A^2 f_s} \]

\[ b_0 \propto \frac{1}{(2^M)^2} \frac{2}{f_s} \]

Cost of 6 dB improvement:
- 1 bit
- factor-of-4 \( f_s \)

Obvious conclusion: practical ADCs feature lower \( b_0 \) at low \( f_s \) because of the higher no. of bits.
Selection of dual-channel converters

In phase measurements, a dual-channel converter is preferred because the two track-and-hold get the same clock, so the with minimum differential jitter.
• Analog noise is higher than quantization noise
• Given a voltage $V$ -> random distribution of output $N$
• This correct -> $V^2 = V_{\text{analog}}^2 + V_{\text{quant}}^2$
   (don’t spoil the resolution with insufficient no of bits)

**Information (bits)**

$$I = \sum_i -p_i \log_2(p_i)$$

**Equivalent No of Bits**

$$\text{ENoB} = \log_2 \left[ 1 + \frac{V_{\text{FSR}}}{\sqrt{12f_N \sigma_V}} \right]$$
Digital Filter and Decimation

Noise, Sampling, and the Parseval theorem

- Convolutions with low-pass h(t)
- 127 coeff. Blackman-Harris kernel provides 70 dB stop-band attenuation
- Future: we will use >>127 coefficients
Digital Down Conversion

Input data stream

$R \cos(2\pi \nu_0 t + \theta)$

I-Q detector

$\sin(2\pi \nu_0 t)$

$\cos(2\pi \nu_0 t)$

Output data stream

$R = \sqrt{I^2 + Q^2}$

$\phi = \text{atan2}(Q/I)$

$\rho = \sqrt{\rho^2}$

DDS

$n_k = (n_{k-1} + N) \mod D$

$D = 2^m$

$\nu_0 = \frac{N}{D} \nu_s$
Examples
## Hardware

<table>
<thead>
<tr>
<th>ADC type</th>
<th>AD9467 / Single Alazartech</th>
<th>LTC2145 / Dual Red Pitaya</th>
<th>LTC2158 / Dual Eval board</th>
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</thead>
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<tr>
<td>Platform</td>
<td>Computer</td>
<td>Zynq (onboard)</td>
<td>Zynq (separated)</td>
</tr>
<tr>
<td>Sampling $f$</td>
<td>250 MHz</td>
<td>125 MHz</td>
<td>310 MHz</td>
</tr>
<tr>
<td>Input BW</td>
<td>900 MHz</td>
<td>750 MHz</td>
<td>1250 MHz</td>
</tr>
<tr>
<td>Bits / ENoB</td>
<td>16 / 12</td>
<td>14 / 12</td>
<td>14 / 12</td>
</tr>
<tr>
<td>Exp.noise (2V&lt;sub&gt;fsr&lt;/sub&gt;)</td>
<td>–158 dBV&lt;sup&gt;2&lt;/sup&gt;/Hz</td>
<td>–155 dBV&lt;sup&gt;2&lt;/sup&gt;/Hz</td>
<td>–159 dBV&lt;sup&gt;2&lt;/sup&gt;/Hz</td>
</tr>
<tr>
<td>Delay / Jitter</td>
<td>1.2 ns / 60 fs</td>
<td>0? / 100 fs diff</td>
<td>1 ns / 150 fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0? / 80 fs single</td>
<td></td>
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<tr>
<td>Power supply</td>
<td>1.8 V &amp; 3.3 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
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<tr>
<td></td>
<td>1.33 W</td>
<td>190 mW</td>
<td>725 mW</td>
</tr>
</tbody>
</table>

Dissipation is relevant to thermal stability

For reference, 100 fs jitter is equivalent to

<table>
<thead>
<tr>
<th>carrier $f$</th>
<th>$\phi$ rms</th>
<th>$S_\phi(f) = b_0$</th>
<th>$10 \log_{10}[L(f)]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 MHz</td>
<td>6.3 µrad</td>
<td>$4 \times 10^{-18}$ rad$^2$/Hz</td>
<td>–177 dBc/Hz</td>
</tr>
<tr>
<td>100 MHz</td>
<td>63 µrad</td>
<td>$4 \times 10^{-17}$ rad$^2$/Hz</td>
<td>–167 dBc/Hz</td>
</tr>
</tbody>
</table>
The observed floor fits the theory
We always use the highest sampling frequency
Transition Noise Measurement

The differential clock jitter introduces additional noise due to the asymmetry between AM and PM.

At 10 MHz input, ≈100 fs the effect of jitter does not show up.
LT 2158 Noise

$S_v(f)$, dBV$^2$/Hz

LT 2158

-104 dBV$^2$/Hz @ 1 Hz

-158 dBV$^2$/Hz

$\approx$ 1 dB added

10 MHz, $V_{pp} \approx 0.95 \ V_{FSR}$
LT2145 (Red Pitaya) Noise

$S_v(f)$, dBV$^2$/Hz

LT 2145

-110 dBV$^2$/Hz @ 1 Hz

-153 dBV$^2$/Hz

$\approx$ 2 dB added

10 MHz, $V_{pp} \approx 0.95 \, V_{FSR}$
AD9467 (Alazartech) Noise

-110 dBV\(^2\)/Hz @ 1 Hz

\[ f(x) \approx -157 \text{ dBV}^2/\text{Hz} \approx 1 \text{ dB added} \]

10 MHz, \( V_{pp} \approx 0.95 V_{FSR} \)
Application to 10 GHz Cryogenic Oscillators

- Rejects the common-path jitter
- Takes in the differential jitter
• Background noise 5–6 dB higher than that of the TSC5125
• We use 2 channel cross spectrum
• TSC5125 uses 4 channel cross spectrum
The Four-Channel Scheme

ADC card 1

ADC

τa

ADC

τb

ADC

τc

DDC

φA–C

R

DDC

φB–C

R

Σ

FFT

(φA–B)1

(ΦA–ΦB)1

cross spectrum

Sφ(f)

AVG

ADC card 2

ADC

τa

ADC

τb

ADC

τc

DDC

φA–C

R

DDC

φB–C

R

Σ

FFT

(φA–B)2

(ΦA–ΦB)2
**Background Noise**

**L(\(f\)), dBc/Hz**

**Four-channel scheme**

-185 dBc baseline

Channel difference

-185 dBc baseline

1E3 AVG

1E6 AVG

"dif_cross_avg1000.txt"
"dif_cross_avg1000.dat"
"dif_ab_avg1000.dat_2chlimitpybAB"
"dif_cha_chb_avg1000.dat"
Compared to a Commercial Instrument

-- this is done only to make sure that there is no calibration mistake --

Four-channel scheme

Measure a Rohde Schwarz synthesizer

L(\(f\)), dBc/Hz

"sma-agilent-meas.dat"
"sma-alazar.dat" u 1:($2-10*\log10(2))
"sma.datasheet.dat"
Conclusions

- White noise
  - Depends on Fs and ENoB
  - Fits well the expectation
- Flicker $-110 \text{ dBV}^2/\text{Hz}$ best found
- First phase noise measurements, (direct & beat)
- Background $-185 \text{ dBc}$ with 4-channel scheme
- Modeling common-mode and differential jitter in progress
- Unwanted correlated effects still unknown
4 – DDSs

- Basics
- Advanced
- Experiments
Basics
Basic DDS scheme

integer: \( n_k = (n_{k-1} + N) \mod D \)

complex: \( z_k = z_{k-1} \exp(j\eta) \)

phase: \( \theta_k = (\theta_{k-1} + \eta) \mod 2\pi \)

<table>
<thead>
<tr>
<th>quantity</th>
<th>digital</th>
<th>analog</th>
</tr>
</thead>
<tbody>
<tr>
<td>state variable</td>
<td>( n )</td>
<td>( \theta = 2\pi \frac{n}{D} )</td>
</tr>
<tr>
<td>assoc. complex</td>
<td>( z = e^{j\theta} )</td>
<td></td>
</tr>
<tr>
<td>modulo</td>
<td>( D = 2^m )</td>
<td>( 2\pi )</td>
</tr>
<tr>
<td>increment</td>
<td>( N )</td>
<td>( \eta = 2\pi \frac{N}{D} )</td>
</tr>
<tr>
<td>time</td>
<td>( k, 0, 1, 2, \ldots )</td>
<td>( t = k/\nu_s )</td>
</tr>
</tbody>
</table>

clock freq. \( \nu_s \)  output freq. \( \nu_0 = \frac{N}{D} \nu_s \)

The contents \( n \) of the \( m \)-bit register is interpreted as a complex number
AD9912, a popular fast DDS

48 bit accumulator, 14 bit DAC, 1 GHz clock

AD9912 data sheet, Fig. 40

AD9912 data sheet, Fig. 45
AD9854, a popular DDS

48 bit accumulator, 300 MHz clock,
12 bit DAC, I-Q output, AM/PM/FM capability

clock in ≤ 300 MHz

clock multiplier

D = 2^48

D-type register

look-up table

amplitude control

in-phase DAC

modulation FM / PM / AM

AD9854 data sheet, Fig. 1
The noise-free synthesizer propagates the jitter $x$ (phase time).

- So, it scales the phase $\varphi$ as $N/D$,
- and the phase spectrum $S_\varphi$ as $(N/D)^2$.
- Notice the absence of sampling.
For N/D <<1, the scaled-down noise hits the output-stage limit

W.F. Egan, Modeling phase noise in frequency dividers, TUFFC 37(4), July 1990
Quantization noise

Analog-to-digital conversion introduces a quantization error $x \ [ -V_{\text{LSB}}/2 \leq x \leq +V_{\text{LSB}}/2 ]$

$n$-bit conversion: $V_{\text{LSB}} = \frac{V_{\text{FSR}}}{2^n}$

Wiener–Khintchine theorem: in ergodic systems, interchange time / ensemble

The noise can be calculated with statistics:

$$\sigma^2 = \frac{V_{\text{LSB}}^2}{12}$$

$$\sigma^2 = \frac{V_{\text{FSR}}^2}{12 \times 2^{2n}}$$

$1/12 \rightarrow -10.8 \text{ dB}$

$2^{2n} \rightarrow 6 \text{ dB/bit}$

Parseval theorem: Energy (power) calculated in time and in frequency is the same

$$N = \frac{V_{\text{FSR}}^2}{6 \times 2^{2n} \nu_s}$$

$$N = \frac{V^2}{\nu_s}$$
Quantization and PM noise

The white PM noise is

\[
P_0 = \frac{1}{8} V_{\text{FSR}}^2 V^2
\]

Example:
14 bit, 1 GHz \rightarrow -173 dB
14 bit, 400 MHz \rightarrow -169 dB
12 bit, 300 MHz \rightarrow -156 dB
Background noise

\[ V_{FSR} \]

\[ V_{pp} = A V_{FSR} \]

\[ A < 1 \]

**Sampling frequency** \( f_s \)

**Signal power**

\[ P_0 = \frac{V_{pp}^2}{8} = \frac{A^2 V_{FSR}^2}{8} \]

**Noise power**

\[ \sigma^2 = \frac{V_{lsb}^2}{12} \]

**Parseval theorem**

\[ S_v = \frac{\sigma^2}{B} \quad \Rightarrow \quad S_v = \frac{V_{lsb}^2}{6 f_s} \]

**Phase noise**

\[ S_{\phi} = b_0 \] (white)

\[ b_0 = \frac{S_v}{P_0} \]

\[ b_0 = \frac{1}{2^{M/2}} \cdot \frac{4}{3 A^2 f_s} \]

**Approximation** (fairly large \( V_p \))

\[ A^2 = 2/3 \] (-1.8 dB)

\[ b_0 \propto \frac{1}{2^{M/2}} \cdot \frac{\frac{2}{f_s}}{3 A^2 f_s} \]
Background noise

\[ b_0 = \frac{1}{(2M)^2} \times \frac{4}{3A^2} \frac{2}{\frac{f_s}{fs}} \]

Cost of 6 dB improvement
- 1 bit
- factor-of-4 \( f_s \)

Obvious conclusion: practical ADCs feature lower \( b_0 \) at low \( f_s \) because of the higher no. of bits
Advanced
State-variable truncation

\[ n_k = (n_{k-1} + N) \mod D, \quad D = 2^m \]

- Only quantization shows up with full m-bit conversion
- Technology \( \rightarrow \) q max
- Why \( p > q \)
- Slow pseudorandom beat, 3d 6h 11m 15s @ 1 GHz, 48 bit
- Spurs \( \rightarrow \) next
The power of spurs comes at expenses of white noise – yet not as one-to-one
Nonlinearity generates spurs

Non-linearity \rightarrow \text{harmonic distortion} \rightarrow \text{aliasing} \rightarrow \text{spurs}

The 3rd Nyquist zone is from \(F_s\) to \(1.5F_s\), and so on. Frequencies in the odd Nyquist zones map directly onto the 1st Nyquist zone, while frequencies in the even Nyquist zones map in mirrored fashion onto the 1st Nyquist zone. This is shown pictorially in Figure 4.10.

The procedure, then, for determining the aliased frequency of the \(N\)th harmonic is as follows:

1. Let \(R\) be the remainder of the quotient \((Nf_o)/F_s\), where \(N\) is an integer.
2. Let \(\text{SPUR}_N\) be the aliased frequency of the \(N\)th harmonic spur.
3. Then \(\text{SPUR}_N = R\) if \((R \leq 0.5F_s)\), otherwise \(\text{SPUR}_N = F_s - R\).

The above algorithm provides a means of predicting the location of harmonic spurs that result from nonlinearities associated with a practical DAC. As mentioned earlier, the magnitude of the spurs is not predictable because it is directly related to the amount of non-linearity exhibited by a particular DAC (i.e., non-linearity is DAC dependent).

Another source of spurs are switching transients that arise within the internal physical architecture of the DAC. Non-symmetrical rising and falling switching characteristics such as unequal rise and fall time will also contribute to harmonic distortion. The amount of distortion is determined by the effective ac or dynamic transfer function. Transients can cause ringing on the rising and/or falling edges of the DAC output waveform. Ringing tends to occur at the natural resonant frequency of the circuit involved and may show up as spurs in the output spectrum.

Clock feedthrough is another source of DDS spurs. Many mixed signal designs include one or more high frequency clock circuits on chip. It is not uncommon for these clock signals to appear at the DAC output by means of capacitive or inductive coupling. Obviously, any coupling of a clock signal into the DAC output will result in a spectral line at the frequency of the interfering clock signal. Another possibility is that the clock signal is coupled to the DAC’s sample clock. This causes the DAC output signal to be modulated by the clock signal. The result is spurs that are symmetric about the frequency of the output signal.

Proper layout and fabrication techniques are the only insurance against these forms of spurious contamination. The spectral location of clock feedthrough spurs is predictable since a device’s internal clock frequencies are usually known. Therefore, clock feedthrough spurs are likely to be non-linearity harmonic distortion.
PLL clock multiplier

- On-Silicon LC oscillator
  - (also used in other AD devices)
- Literature suggests $Q \approx 5...10$
  - Leeson $f_L = 50–100$ MHz
- Tight PLL is needed
- Divider noise
- No data from the manufacturer

The AD 9854 is likely similar, yet the VCO frequency is 300 MHz

This is just a wild guess!

![Diagram of SYSCLK PLL Multiplier](image)

- Phase noise response to PLL
- Loop filter “peaking” at cutoff
- Leeson frequency?
- $1/\sqrt{2}$
- free-running VCO?
3.3 V: lower PM noise than 1.8 V

Probably related to the cell size and to the dynamic range

Figure 16. Absolute Phase Noise Using CMOS Driver at 3.3 V, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed) DDS Run at 200 MSPS for 10 MHz

E. Rubiola, Mar 2007 (adapted from the Analog Devices data sheets)

Plots originally used to extract the noise parameters
High-Frequency DDSs

AD9914 12 bit, 3.5 GHz
64 bit accumulator (190 pHz res)

Residual Phase Noise
Data sheet Fig. 17

AD9915 12 bit, 2.5 GHz
64 bit accumulator (135 pHz res)

Residual noise is close to that of the gear-box model
Plots are from the manufacturer data sheet
Whether spurs are removed or not, is not said
Experiments

- AD9912 demo board
- AD9854 (9914) demo board
- Claudio’s AD9854 board
  - V1 – Current feedback OPA output stage
    - 25Ω input impedance, 8 nV/√Hz noise, kHz coupled
  - V2 – Balun and MAV-11 RF output amplifier
    - F = 3.6 dB, AC coupled (≥1–2) MHz
      - Specified above 50 MHz, yet works well below
Experimental method (PM noise)

- Pseudorandom noise, slow beat (days)
- The probability that two accumulators are in phase is $\approx 0$
- Two separate DDS driven by the same clock have a random and constant delay
- The delay de-correlates the two realizations, which makes the phase measurement possible

Single channel

Dual channel

kind of virtual mixer, after (sub)sampling & direct ADC
Claudio’s prototypes

- AD9954
- AD9854
- Cyclon
- AD9912
- balun
- MAV11
- AD9854
- AD9954
- Cyclon
PM noise vs. output frequency

AD9854 ck 180 MHz

Balun and MAV-11 at the DDS output

- 22.5 MHz: \( b_{-1} = -114.5 \text{ dB} \)
- 11.25 MHz: \( b_{-1} = -120.5 \text{ dB} \)
- 5.625 MHz: \( b_{-1} = -126 \text{ dB} \)
- 2.81 MHz: \( b_{-1} \approx -130 \text{ dB} \)
- 1.406 MHz: \( b_{-1} \approx -133.5 \text{ dB} \)

DDS internal stages

- 30 dB/dec
- Thermal effect?

(DDS) output stage

- 1.40625 MHz
- 2.8125 MHz
- 5.625 MHz
- 11.25 MHz
- 22.5 MHz

Power supply
AD9912 noise vs. out frequency
– low Fourier frequencies –

AD9912 1.5625 to 100MHz, carrier at 100.0 MHz

Phase Noise Power Spectrum $dB_{rad^2}/Hz$

$S_\phi (1Hz) = -124.23 \, dB$

$S_\phi (1Hz) = -128.03 \, dB_{rad^2}/Hz$

$S_\phi (1Hz) = -122.48 \, dB_{rad^2}/Hz$

$S_\phi (1Hz) = -109.27 \, dB_{rad^2}/Hz$
• The –140 dB floor is due to AD8002 at the DDS output
• The flicker is unchanged (comes from the DDS)
**AD9854 noise**

**AD9852, AD9854**

**Specs, regular output**

- Two outputs: cos+aux / I-Q
- 48 bit accu, 12 bit dac
- $f_c = 300$ MHz, 3.3V cmos

Flicker is in fair agreement

White is made low by spurs

**Basic formula for white noise**

$$b_0 = \frac{4}{3} \frac{1}{2^2n \nu_s} \text{ rad}^2/\text{Hz}$$

<table>
<thead>
<tr>
<th>who</th>
<th>meas, dB</th>
<th>math, dB</th>
<th>clock, MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>specs</td>
<td>-159</td>
<td>-155.8</td>
<td>300</td>
</tr>
<tr>
<td>YG</td>
<td>-158</td>
<td>-155.0</td>
<td>250</td>
</tr>
<tr>
<td>CC</td>
<td>-162.5</td>
<td>-153.6</td>
<td>180</td>
</tr>
</tbody>
</table>
Flicker is in quite a good agreement between YG and CC

I–Q spectra cannot be compared to specs

250 MHz clock, I–Q noise

\[ b_{-1} = -118 \text{ dB}, \quad \text{scales as } 1/\nu^2 \]

\[ -140 \text{ dB@ } 180 \text{ MHz: (opa AD8002 white)} \]

INRIM

\[ \text{hits } b_{-1} = -132 \text{ dB} \]

\[ \text{hits } -158 \text{ dB} \]
PM noise vs. output amplitude

- PM noise scales 6 dB per factor-of-two output amplitude
- Signature of digital multiplication: lower amplitude is obtained by reducing the integer number at the DAC input
High-frequency DDSs

AD9915 12 bit, 2.5 GHz
64 bit accumulator (135 pHz res)
PM noise vs. clock amplitude

-163 dB @ –8 dBm

flicker

another flicker-like process?

1/f\textsuperscript{4} from thermal fluctuation?

-122 dB from supply voltage

1/f\textsuperscript{4} from thermal fluctuation?

flicker

b\textsubscript{−1} \approx −122 dB

-163 dB @ −8 dBm

-167 dB @ +7 dBm

-167 dB @ +7 dBm
The effect of the clock frequency

AD9912 ck 400 MHz, out 12.5 MHz

Phase Noise Power Spectrum $dB_{rad}^2/Hz$

INRIM

Clock frequency ($\geq 200$ MHz spec)

- 400 MHz
- 50 MHz
- 100 MHz
- 200 MHz
- 50 MHz

Fourier Frequency (Hz)
Thermal effects

- Low-frequency temperature fluctuations induce phase noise
- A large thermal mass helps
AD9912 Voltage sensitivity

- Agilent E8257D
- Power Splitter (PSC-2-1, Minicircuits)
- Phasemeter Symmetricom TSC5125A
- Demo board
- AD9912

Graphs and diagrams showing sensitivity to 1.8V power supply.
AD9912 temperature sensitivity

- Temperature control (chamber)
- Measured: –2 ps/K
- Includes cables, baluns etc
AD9912 sensitivity to temperature (alternate)
AD9912 temperature sensitivity

- High frequency: $-2 \text{ ps/K}$, constant
- Low frequency: $1/v^3$ law
PM noise of the AD 9912

- At 50 MHz and 10/12.5 MHz we get ≈15 dB lower flicker than the data-sheet spectrum
- Experimental conditions unclear in the data sheets
Spurs reduce the white noise

Phase Noise PSD

AD9854, ck 300 MHz

INRIM

floor reduction
spurious

INRIM
Spurs can be amazing
More about a PM-noise bump

- Low PSRR (power-supply rejection ratio) of PM noise

- For instance, The AD9912 at 25 MHz out has 15 ps/% supply-voltage sensitivity

- No bump at $10^3$–$10^5$ Hz is seen in the data-sheet spectra

- DC regulator may show a similar bump, alone or with the output capacitor

X7R SMD capacitor shows low ESR ($\leq 5$ mΩ)
PLL clock multiplier

10 → 640 → 10 MHz
PLL clock multiplier

10 -> 640 -> 10 MHz
PLL clock multiplier

AD9912: 10--->640--->10, carrier at 10.0 MHz

Phase Noise Power Spectrum $dB_{rad^2/Hz}$

$S_\phi (1Hz) = -115.32 \, dB_{rad^2/Hz}$

$S_\phi (1Hz) = -116.83 \, dB_{rad^2/Hz}$
Effect of other parts on the PCB

A blinking LED somewhere on the PCB spoils the output spectrum.
ADEV vs. clock frequency

$H_r = 500 \text{ Hz and } H_f = 50 \text{ Hz}$

specs: $ck \geq 200 \text{ MHz}$

C. Calosso & E. Rubiola, May 2012
Commented:
Original: 02_AD9912_scanFck/FckScan_01_adev.png
ADEV vs. output frequency

\[ f_H = 500 \text{ Hz and } f_H = 50 \text{ Hz} \]

C.Calosso & E.Rubiola, May 2012

Commented:

Original: 01_AD9912_scanF/FoutScan_01_aDEV.png

thermal effect
ADEV vs. output frequency

AD9854 ck 180 MHz fh = 50 Hz

Fractional frequency Allan deviation

Averaging time (s)
The cross spectrum $S_{ba}(f)$ rejects the single-channel noise because the two channels are independent.

\[ S_{ba}(f) = \frac{1}{4k_a k_b P_a P_b} S_\alpha(f) \]

Averaging on $m$ spectra, the single-channel noise is rejected by $\sqrt{1/2m}$.

A cross-spectrum higher than the averaging limit validates the measure.

---

AM noise (1)

AD9854
4.8–80 MHz output

250 MHz clock, AM noise (cross spectrum)

\[ S_\alpha(f)(\text{dB/Hz}) = \frac{\alpha}{2} - 11 \]

\[ h_{-1} = -105\ldots-115 \text{ dB} \]

4.8 MHz
10 MHz
20 MHz
40 MHz
80 MHz

\[ .//am_dds3\_4p8MHz.dat \ u 1:(($2/2)–11) \]
\[ .//am_dds3\_10MHz\_v4.dat \ u 1:(($2/2)–12) \]
\[ .//am_dds3\_20MHz.dat \ u 1:(($2/2)–13) \]
\[ .//am_dds3\_40MHz.dat \ u 1:(($2/2)–11) \]
\[ .//am_dds3\_80MHz.dat \ u 1:(($2/2)–11) \]
AM noise (2)

250 MHz clock, AM noise

4.8 MHz output

10 MHz output

20 MHz output

4.8–80 MHz output

250 MHz clock, AM noise (cross spectrum)
Conclusions

- Noise theory and model for the DDS
- A lot of still-not-published experimental data
  - Phase noise
  - Allan deviation
  - Amplitude noise
- Experiments done at INRIM and at FEMTO-ST
- Model and experimental data are in fair agreement

http://rubiola.org
5 — Dividers

- Π and Λ Dividers
- Microwave Dividers
Π and Λ Dividers
Motivations

- **Seminal article by W. F. Egan (1990)**
  - Milestone in the domain, never forget it
  - However, TTL and ECL logic families are now obsolete

- **Microwave (photonics) → highest spectral purity**

- **Transfer the spectral purity to HF/VHF**
  - Dividers are more comfortable than multipliers
    - NIST now uses analog dividers

- **Nowadays digital electronics is fantastic**
  - CPLD & FPGA → Easy to duplicate
  - High number of gates for cheap
  - High toggling frequency (1.5 GHz)

E. Rubiola & al, Phase noise in the regenerative frequency dividers, IEEE T IM 41(3), June 1992
The Gear Work Model

- The noise-free divider
  - Keeps the input jitter $x(t)$ (phase-time fluctuation)
  - Scales down
    - $\varphi$ by $1/D$ [rad]
    - $S\varphi$ by $1/D^2$ [rad$^2$/Hz]

In the real divider
- $S\varphi$ of the output often dominates
- Aliasing is present

Parseval's Theorem

The energy calculated in the time domain is equal to the energy calculated in the frequency domain.

\[
\int_{-\infty}^{\infty} \left| x(t) \right|^2 dt = \int_{-\infty}^{\infty} \left| X(f) \right|^2 df
\]

**Time domain:**
- Average power, truncated signal
  \[
  \sigma^2 = \frac{1}{T} \int_{0}^{T} \left| x(t) \right|^2 dt
  \]

**Frequency domain:**
- One-sided PSD, truncated signal
  \[
  S_x(f) = \frac{2}{T} \left| X_T(f) \right|^2
  \]

For ergodic signals, the time average is equal to the ensemble average.
Sampling and Aliasing

— Energy conservation applies to the unfiltered signal —

Input signal (unfiltered wide-band noise)

Reconstructed signal (aliased)

\[ f_N = \frac{1}{2} f_s \quad \text{Nyquist frequency} \]

\[ f_N = \frac{1}{2} f_s \]

• Multiple aliases overlap to the main part of the spectrum
• With white noise, the PSD increases by \( B/f_N \) (Bandwidth / Nyquist \( f \))

Downsampling increases the (PM) noise spectrum

High \( f_N \)

\[ N = \sigma^2/f_N \]

Low \( f_N \)

\[ N = \sigma^2/f_N \]
Aliasing and $1/f$ Noise

Proportionally lower power in the higher-$f$ aliases

Small effect on the overall noise spectrum
PM-Noise Aliasing in the Input Stage

- Edge-sampling at $2v_i$ inherent in the sin-to-square conversion
- Full-bandwidth ($B$) noise is taken in
- The phase-noise Nyquist frequency is $v_i$
- The sampling process increases the noise by $B/v_i$

Eventually, clipping removes the AM noise [Pfaff 1974]
Aliasing in Π Divider

Regular synchronous divider
The Greek letter Π recalls the square wave

• The gearbox scales \( S\varphi \) down by \( 1/D^2 \)

• The divider takes 1 edge out of \( D \)
  • Raw decimation without low-pass filter
  • Aliasing increases \( S\varphi \) by \( D \)

• Overall, \( S\varphi \) scales down by \( 1/D \)

input sampling frequency \( 2\nu_i \)
output sampling frequency \( \nu_o = 2 \frac{1}{D}\nu_i \)

\[ \frac{1}{10} \]

\[ \Pi \]
The $\Lambda$ Divider – Little/no Aliasing

New divider architecture
Series of Greek letters $\Lambda\Lambda\Lambda\Lambda\Lambda$ recalls the triangular wave

- Gearbox and aliasing $\rightarrow$ $1/D$ law
- Add $D$ independent realizations shifted by $1/2$ input clock,
- reduce the phase noise by $1/D$,
- … and get back the $1/D^2$ law

The names $\Pi$ and $\Lambda$ derive from the shape of the weight functions in our article on frequency counters
E. Rubiola, On the measurement of frequency ... with high-resolution counters, RSI 76 054703, 2005
Experimental Method

Large input PM noise is used to emphasize the effect of aliasing

- Intentionally high PM noise at the input
- The scaled-down input noise is higher than the output-stage noise

\[ S_\phi(f) \]

\[ 1/D^2 \]

\[ 1/D^2 \]

- Large attenuation/ampli → noise
- Digital instruments for phase-noise measurement can handle \( f_{\text{input}} \neq f_{\text{reference}} \)
- Correlation reduces the background
Dividers Under Test

EPM3064A CPLD (Altera MAX 3000 Series, 64 macro-cells, speed grade 7 ns)

Π divider
- the one everybody knows -

Multi-buffer Π divider

The outputs are arguably independent
Try to reduce the output-stage noise

Λ divider

White noise:
The clock edges are independent
Correct for aliasing
As Simple as That...
Results – Test on Aliasinging

- **White region**
  - Negligible aliasing
  - $1/D^2$ law (-20 dB)

- **Flicker region**
  - $1/D$ law
  - $1/D^2$ law (-20 dB)

**Graphical Representation**

- 10 Divider, 100 MHz ck

- Phase noise PSD, dB/Hz
- Fourier frequency, Hz

- 0.5 dB discrepancy
- -20 dB
- -100 dB
- -130 dB

- 100 MHz input
- 100 MHz int. ck.
- 10 MHz $\Pi$ div.
- 10 MHz $\Lambda$ div.

- Internal clock
- Sin input
- $\Pi$ divider output
- $\Lambda$ divider output

- +4 dB
- -9.3 dB (theory -10)
- -18.7 dB (theory -20)
Phase Noise of Real Dividers

- **Flicker region** -> Negligible aliasing
- The multibuffer Π divider is still not well explained
- The Λ divider exhibits low 1/f and low white noise

![Diagram of the Π divider and the Λ divider](image)
Allan Deviation in Real Dividers

- Slope $1/\tau$, typical of white and flicker PM noise
- The $\Lambda$ divider performs $2\times10^{-14}$ at $\tau = 1$ s, 10 MHz output
Noise of the Λ divider and two DDSs

<table>
<thead>
<tr>
<th>noise</th>
<th>Λ div.</th>
<th>AD9854</th>
<th>AD9912</th>
</tr>
</thead>
<tbody>
<tr>
<td>(b_0)</td>
<td>(-165)</td>
<td>(-160)</td>
<td>(\approx -163)</td>
</tr>
<tr>
<td>(b_{-1})</td>
<td>(-130.5)</td>
<td>(-121.5)</td>
<td>(-129) inferred</td>
</tr>
<tr>
<td>(b_{-2})</td>
<td>—</td>
<td>—</td>
<td>— plot not shown</td>
</tr>
<tr>
<td>(b_{-3})</td>
<td>—</td>
<td>—</td>
<td>(-134) (seen at lower (v_0))</td>
</tr>
</tbody>
</table>
The $\Lambda$ Divider Versus the DDS

- The $\Lambda$ divider performs $2 \times 10^{-14}$ at $\tau = 1$ s, 10 MHz output
- Thermal effects make the DDS worse at $\tau > 1$ s
- The $\Lambda$ divider is free from thermal effects – at the scale shown
The Bottom Line

• Aliasing in traditional dividers
  • Increases white noise
  • Has little effect on flicker

• Flicker in multi-buffer Π divider not understood yet

• The new Λ divider
  • Is little/no affected by aliasing
  • Exhibits the lowest PM noise
    flicker: $b_{-1} \approx -130$ dB
    white: $b_0 \approx -165$ dB
  • Features $2 \times 10^{-14}$ at $\tau = 1$ s, 10 MHz output
  • Is free from the thermal effects seen in DDSs at $\tau > 1$ s

home page http://rubiola.org

Thanks – J. Groslambert, V. Giordano, M. Siccardi, J.-M. Friedt
Grants from ANR (Oscillator IMP and First-TF network), and Region Franche Comte
Microwave Dividers
NB7L32M ÷2 μWave Divider

10 GHz ÷ 2 = 5 GHz

Method

- Compare two dividers
- Use 5.01 GHz as a common oscillator, and beat
- Digital PM noise measurement at 10 MHz
- O-I: Two equal dividers
- O-O: Two outputs of the same divider
- Shown: spectrum of one divider
NB7L32M ÷2 μWave Divider

Phase noise vs input frequency

[Graph showing phase noise vs. Fourier frequency for different input frequencies, with annotations for 'x-type', 'φ-type', 'too large Δ', and 'output stage: 5 GHz'].

(NB7L32M ÷2 μWave Divider)
**NB7L32M ÷2 µWave Divider**

Works fairly well even at low input power (useful)

**Notes**

- At –16 dBm the white noise increases by 3 dB.
- The critical power where \((b_0)_\varphi = (b_0)_x\) is –16 dBm.
- Hence \((b_0)_{x\text{-type}} \approx -140 \text{ dB}\).
NBSG53A SiGe $\div 2$ $\mu$Wave Divider

Method

- Use 5.01 (2.51) GHz as a pivot oscillator, and mixers
- Digital PM noise measurement at 10 MHz
- One divider shown

- $1/f \rightarrow$ pure gearbox model (as expected)
- White $\rightarrow$ aliased gearbox model (as expected)
- Likely, 1 dB discrepancy in $w$ and $1/f$ (mixer response)

Debugged: $-97.5$ and $-137$
NBSG53A SiGe ÷2 μWave Divider

- Compares unfavorably to the NB7L32M
- More noise and less tolerance to low power

Common belief: SiGe has low 1/f noise.
NBSG53A SiGe ÷2 μWave Divider

Output vs Output gives info about the output stage

The problem seems in the gear box, rather in the output stage
Hittite HMC-C040, $\div 10$ Divider

2 Hittite divider by 10 HMC–C040, Fin=10GHz

2 dividers by 10, input power: $-9$ dBm
2 dividers by 10, input power: $-3$ dBm
2 dividers by 10, input power: $5$ dBm

Take away 3 dB for one divider
## Microwave Dividers Compared

<table>
<thead>
<tr>
<th></th>
<th>10 GHz ÷2</th>
<th>5 GHz ÷2</th>
<th>2.5 GHz ÷2</th>
<th>lower</th>
</tr>
</thead>
<tbody>
<tr>
<td>NB7L32M</td>
<td>–100</td>
<td>–109</td>
<td>–109</td>
<td>600 MHz 1.2 GHz ÷2</td>
</tr>
<tr>
<td>NBSG53A</td>
<td>97.5</td>
<td>–103.5</td>
<td>–104</td>
<td>800 MHz 1.6 GHz ÷2</td>
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<tr>
<td>HMC-C040</td>
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<td></td>
<td>–113</td>
<td>1 GHz 10 GHz ÷10</td>
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<tr>
<td>HMC705LP4</td>
<td></td>
<td></td>
<td>–121</td>
<td>0.5 GHz 2.5 GHz ÷5</td>
</tr>
</tbody>
</table>
Suggested Readings
Suggested Reading

Bernard Widrow, Istvan Kollar

Quantization Noise

Cambridge 2008

- Chapter 15: Roundoff noise in FIR digital filters and in FFT calculations
- Appendix G: Quantization of a sinusoidal input
Suggested Reading

Walt Kester (editor)

Analog-Digital Conversion

Analog Devices 2004

Suggested Reading

Marcel J. M. Pelgrom
Analog-to-Digital Conversion
Springer 2010