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Phase Noise and Jitter in Digital Electronic Components

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Outline

- Noise mechanisms
- Phase noise in selected devices
- Some facts related to phase and noise
- Phase noise in microwave devices

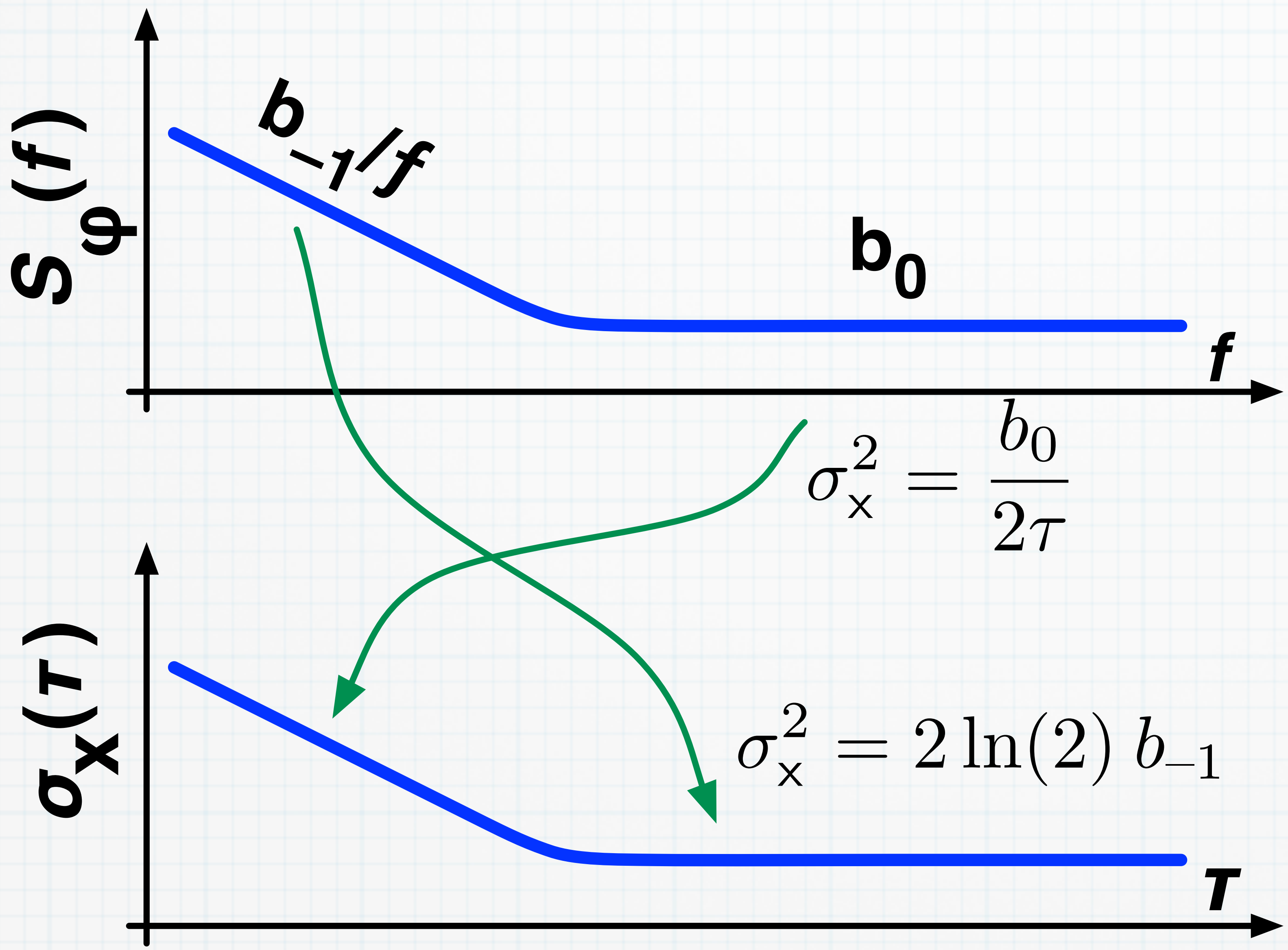
home page http://rubiola.org

Motivations

- Low-noise frequency synthesis
  - Started with the Λ dividers on a CPLD (10 phases)
    - Successful, and ridiculously simple
  - Hoped a 1 GHz –> 5 MHz divider (200 phases) on FPGA kills the noise, and compete with the analog dividers
    - No way!
- The world goes digital
  - IC manufacturers / users only care about total jitter
  - We all want
    - Phase noise,
    - ADEV
    - Stability of the delay

Noise Mechanisms

Phase and phase-time



random phase

$$\varphi(t)$$

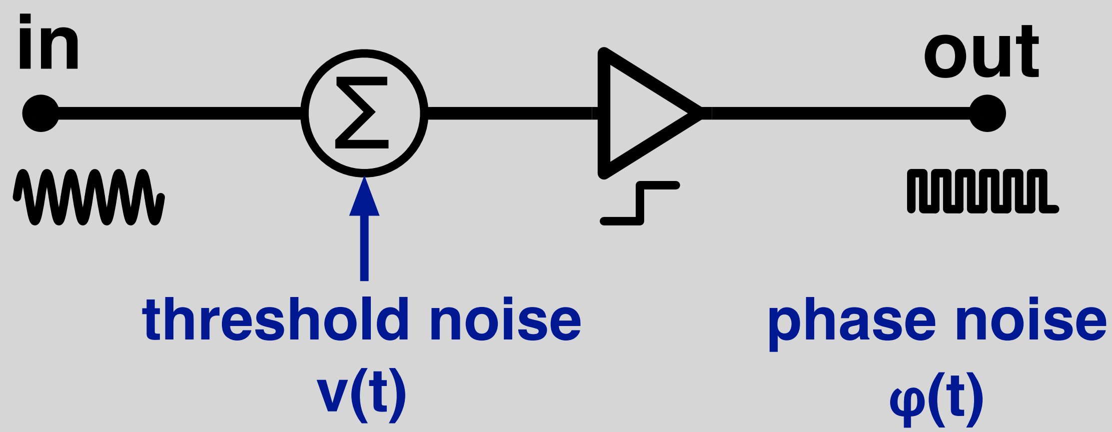
phase-time (fluctuation)

$$\mathrm{x}(t) = \frac{\varphi(t)}{2\pi\nu_0}$$

TDEV $\sigma_x(\tau)$ same as ADEV, but we use x(t) instead of y(t)

You may be more familiar to $\sigma_y^2(\tau) = h_0/2\tau + 2\ln(2)h_{-1}$

Phase noise in the input stage

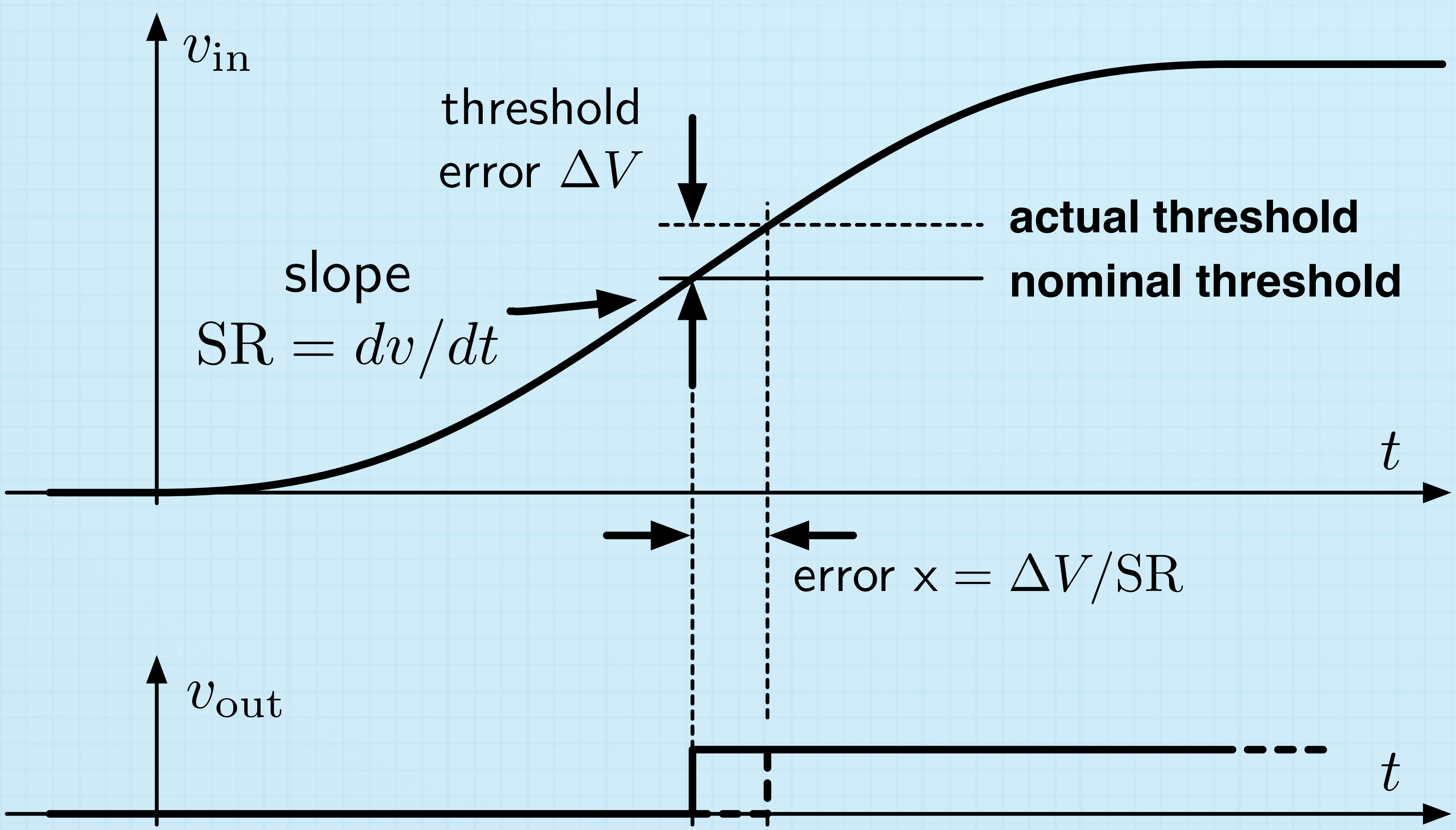


φ-type noise

$$S_\varphi(f) = \frac{S_V(f)}{V_0^2}$$

constant vs ν_0

Threshold fluctuation

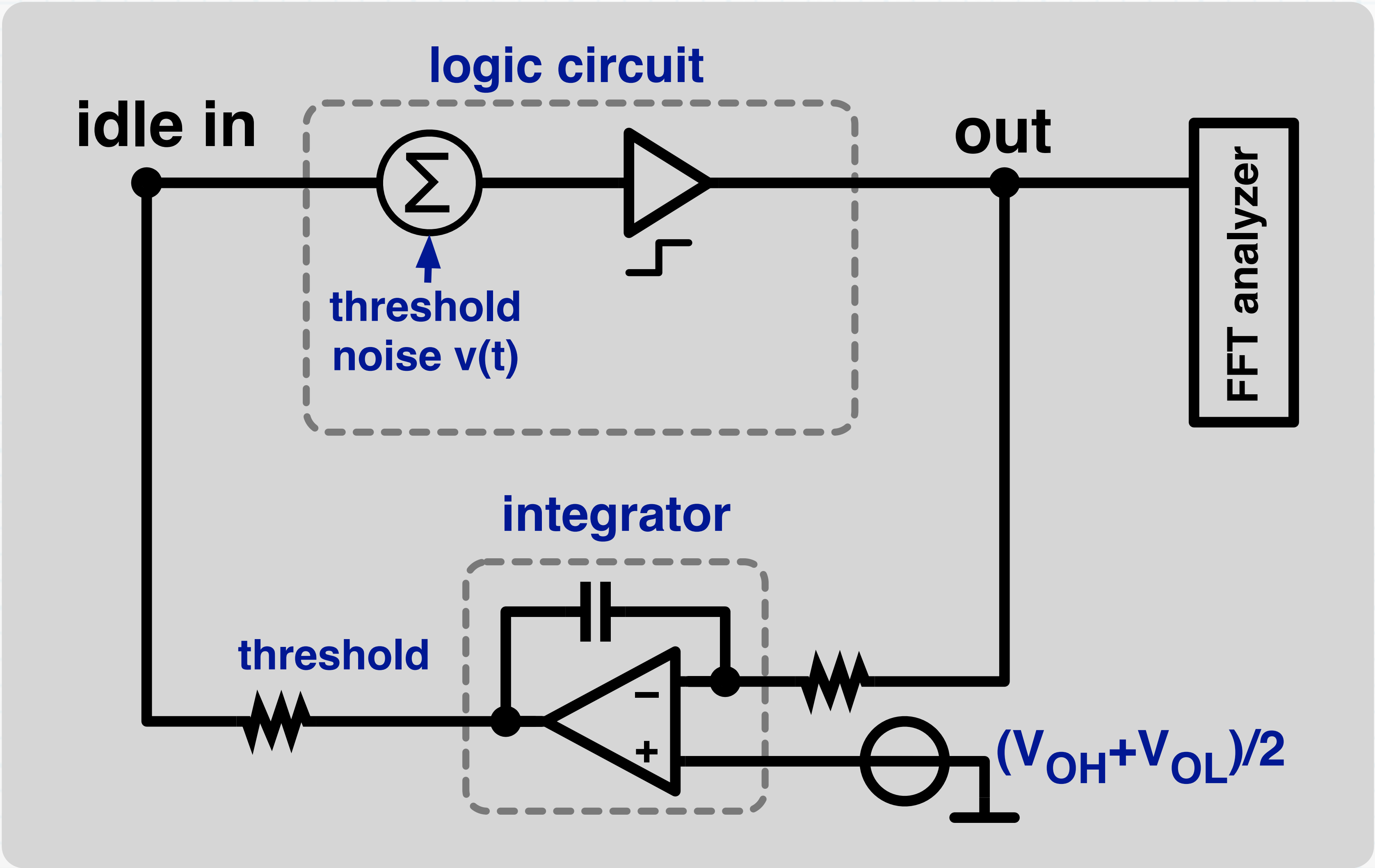


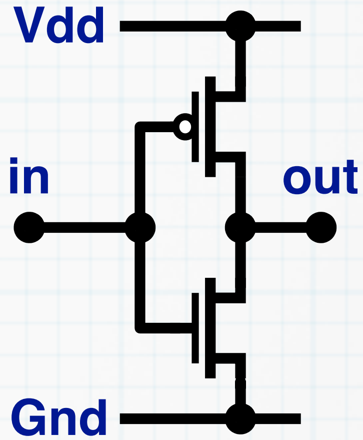
mechanism

$$\mathsf{x}(t) = \frac{(\Delta V)(t)}{(\text{SR})(t)}$$

$$\varphi(t) = \frac{2\pi\nu_0(\Delta V)(t)}{(\text{SR})(t)}$$

Threshold-noise measurement

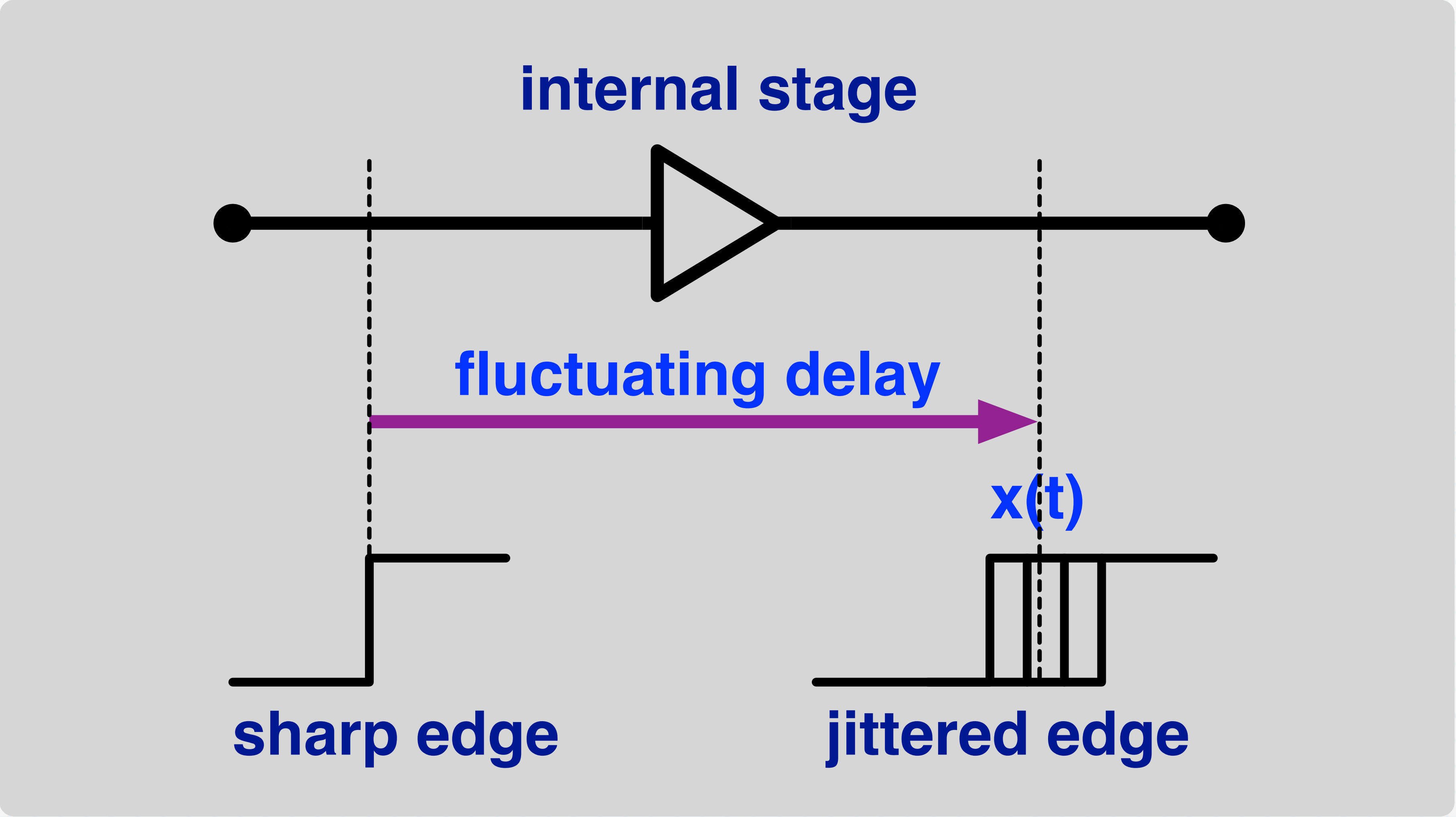




- Keep the logic at the threshold, where it shows analog gain
- Measure the voltage (current) fluctuation needed to stabilise at the threshold
- Works only on simple (old) circuits
- Threshold-mismatched cascade –> gain not accessible
- FPGAs complexity make the analog gain inaccessible

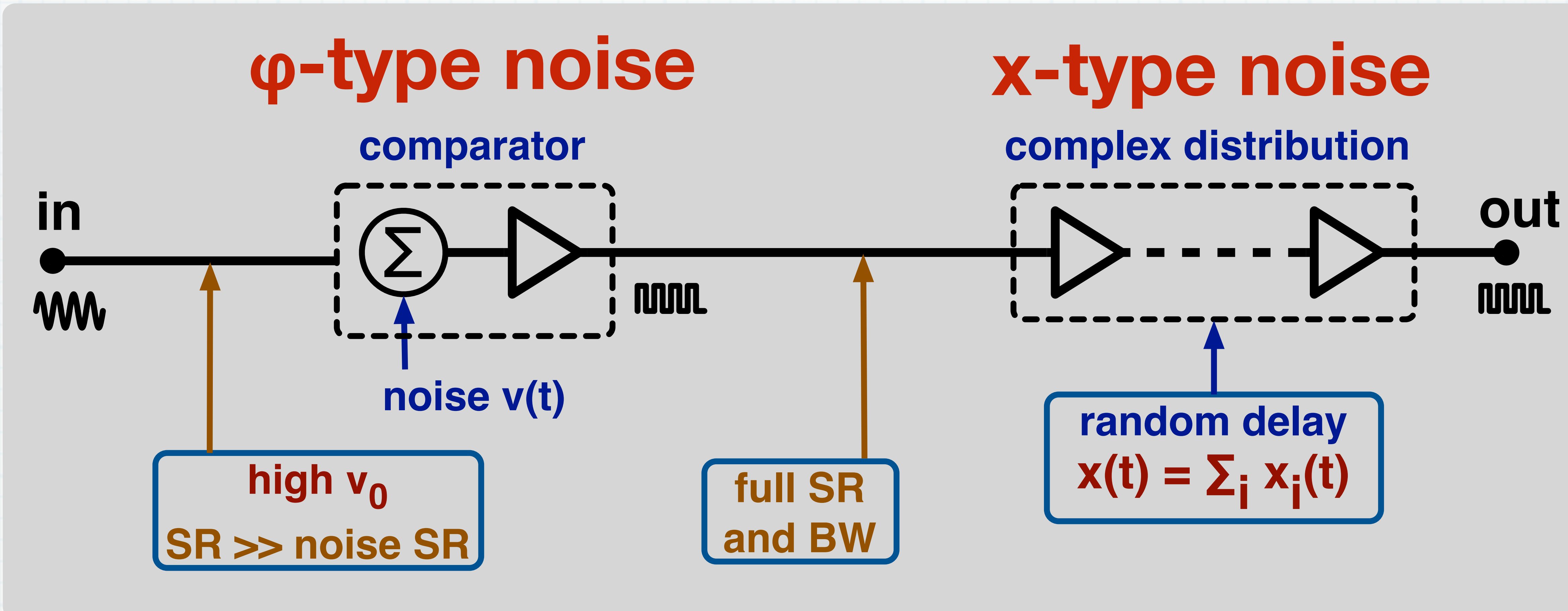
Internal delay fluctuation

x-type noise



- The internal delay fluctuates by an amount x(t)
- This has nothing to do with the threshold and to the frequency – if any

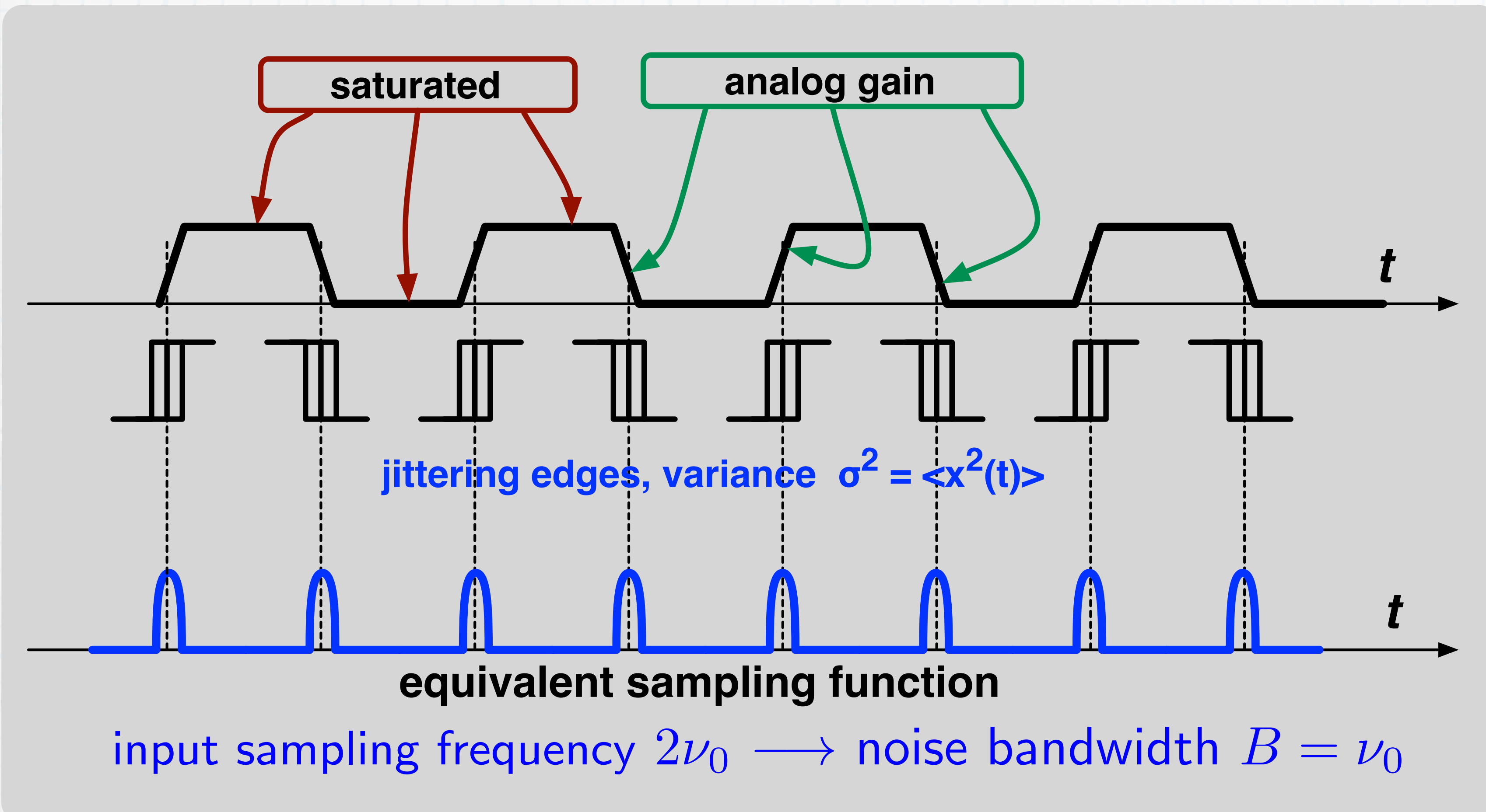
Full noise mechanism

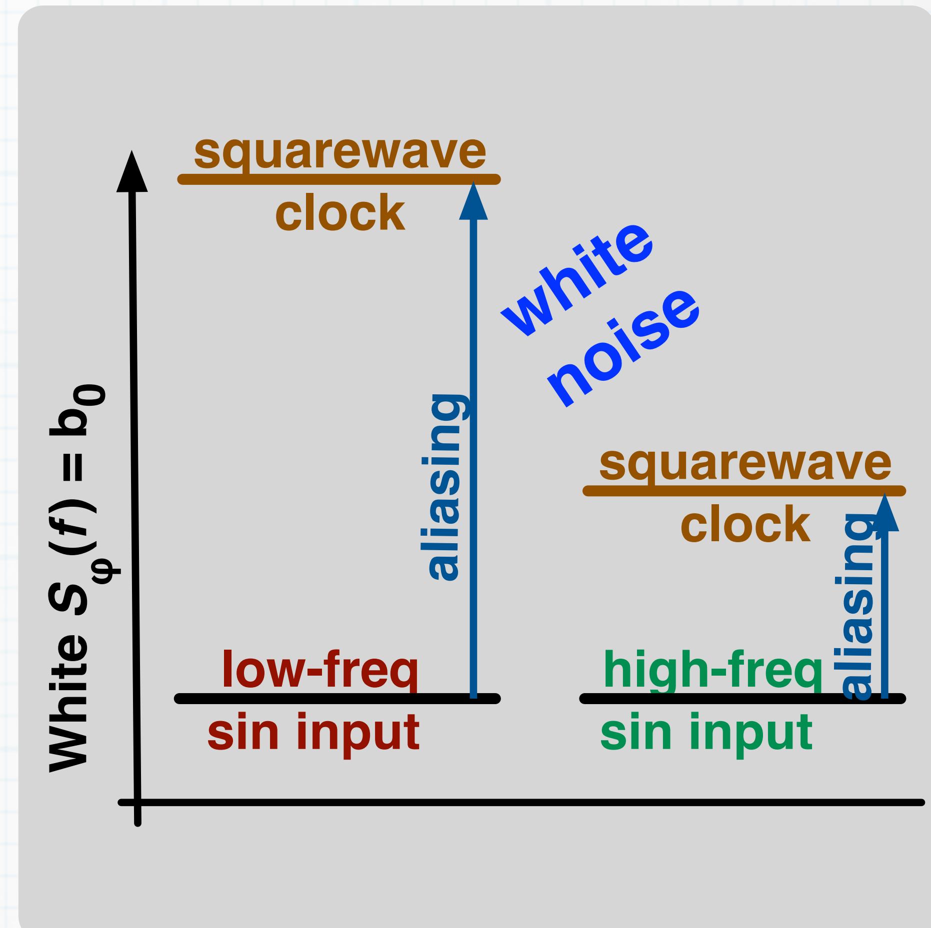


- The φ-type noise noise may show up or not, depending on input noise and SR
- At the comparator out, the edges attain full SR and bandwidth of the technology
- Complex distribution –> independent fluctuations add up

$$x(t) = \sum_i x_i(t) \quad \text{and} \quad \langle x^2(t)\rangle = \sum_i \langle x_i^2(t)\rangle$$

Aliasing mechanism





Flicker and slow noise types

- Too low power at high frequency
- No aliasing

White noise

- The variance σ^2 is independent of frequency
- Parseval theorem applies

$$\sigma^2 = b_0 B = b_0 \nu_0$$

- Aliasing –> higher phase noise at lower carrier frequency

Summary of the noise types

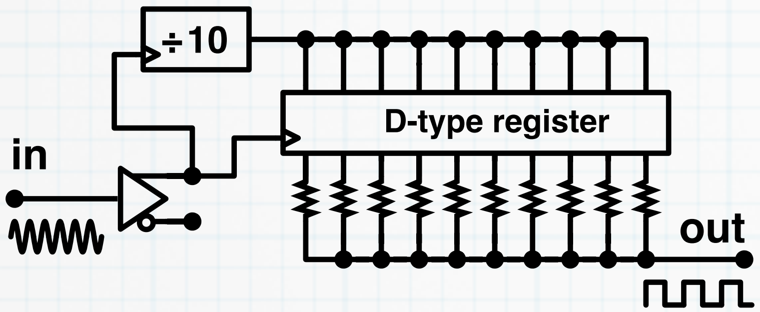
Noise type	**Dependence on ν_0**		
	$S\varphi(f)$	$Sx(f)$	
3 Pure x-type	ν_0^2	C vs. ν_0	1/*f*
4 Aliased x-type	ν_0	$1/\nu_0$	seldom
1 Pure φ-type	C vs. ν_0	$1/\nu_0^2$	1/*f*
2 Aliased φ-type	$1/\nu_0$	$1/\nu_0^3$	white

Phase Noise in Selected Devices

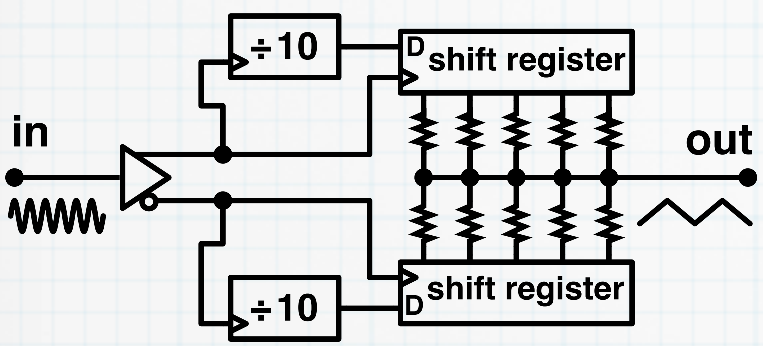
Measurements are performed with the Symmetricom (Microsemi) DS 5125 and 5120 dual-channel phase meter

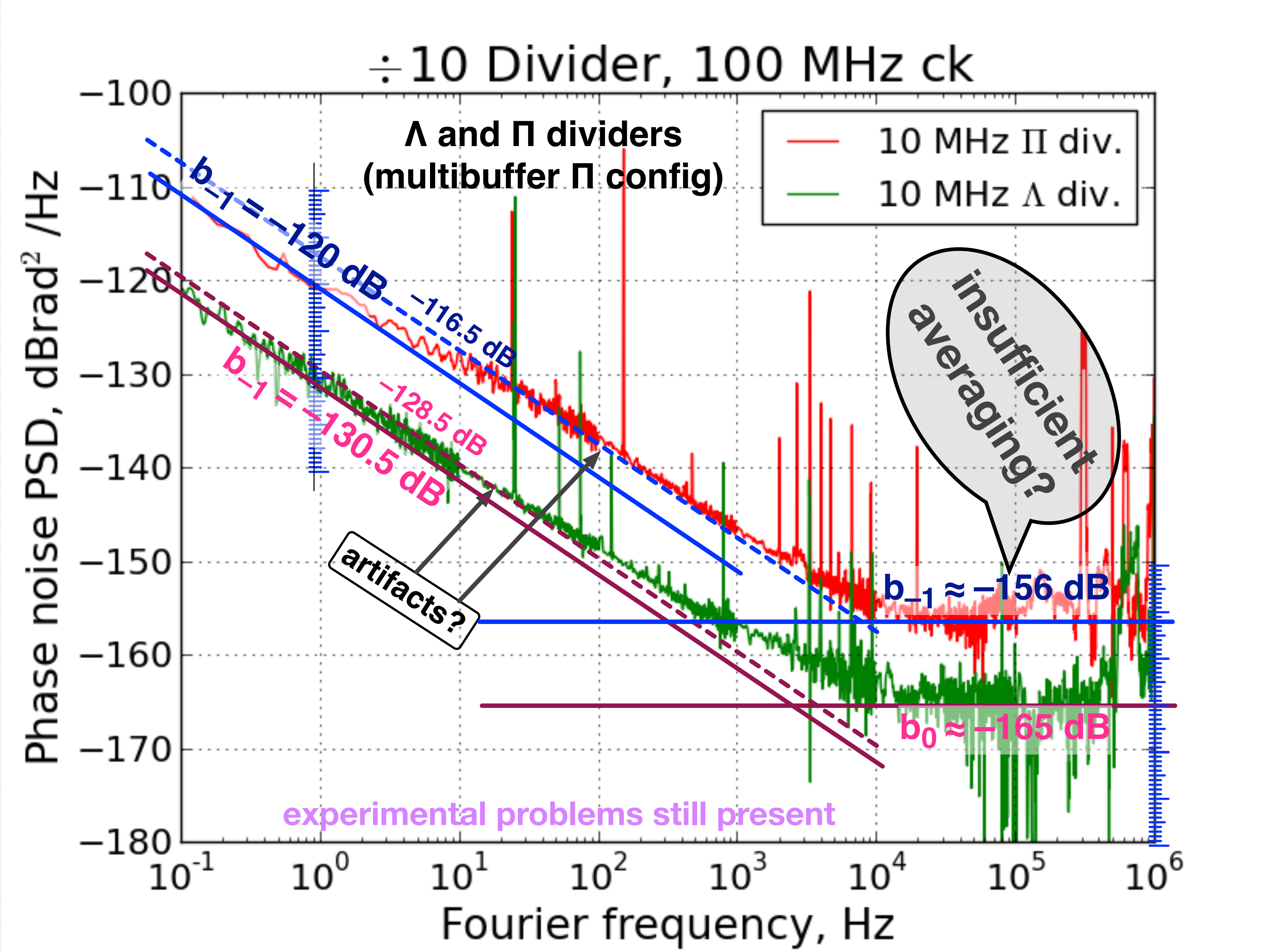
MAX 3000 CPLD [300 nm] (1)

Π divider



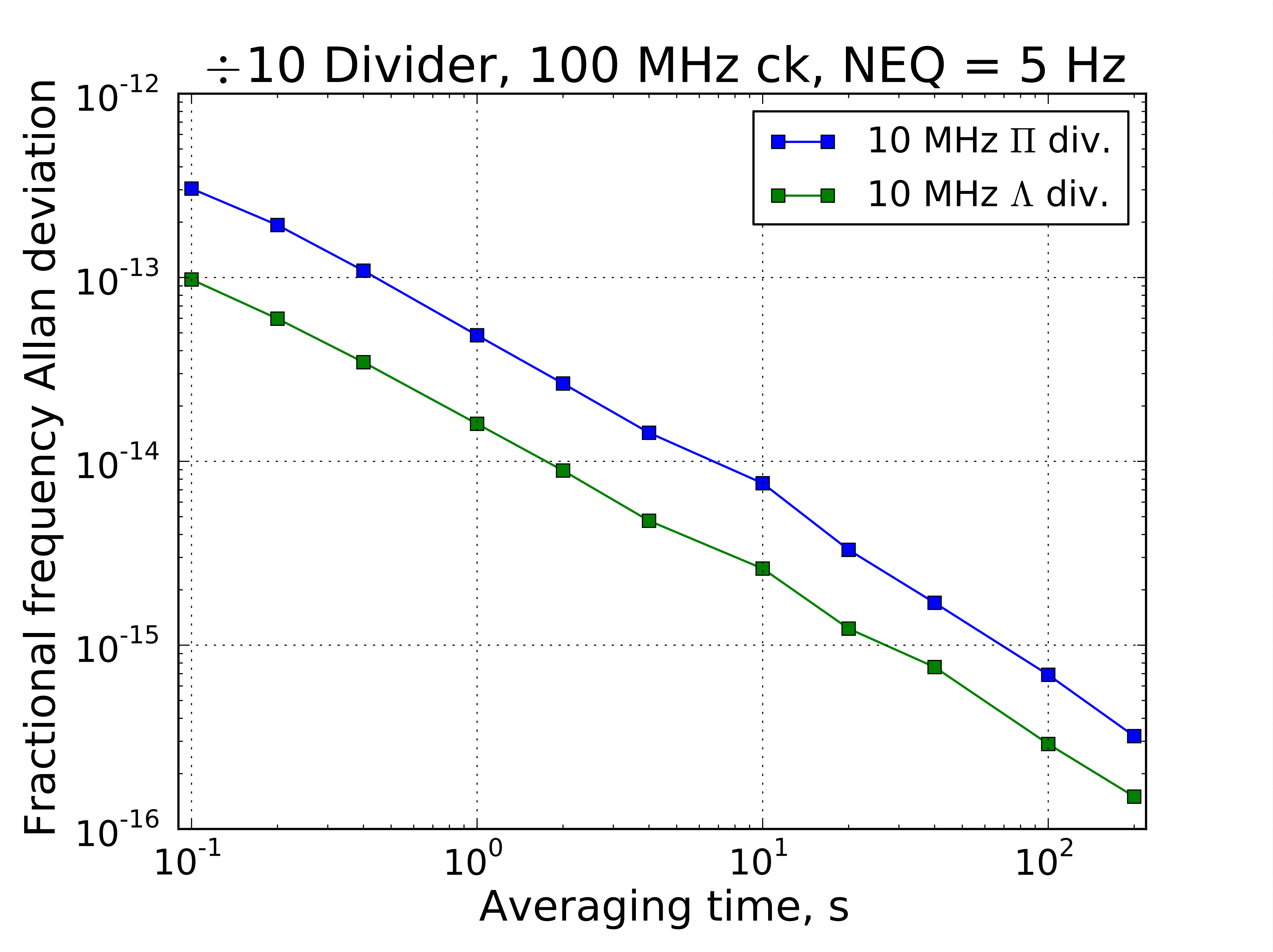
Λ divider





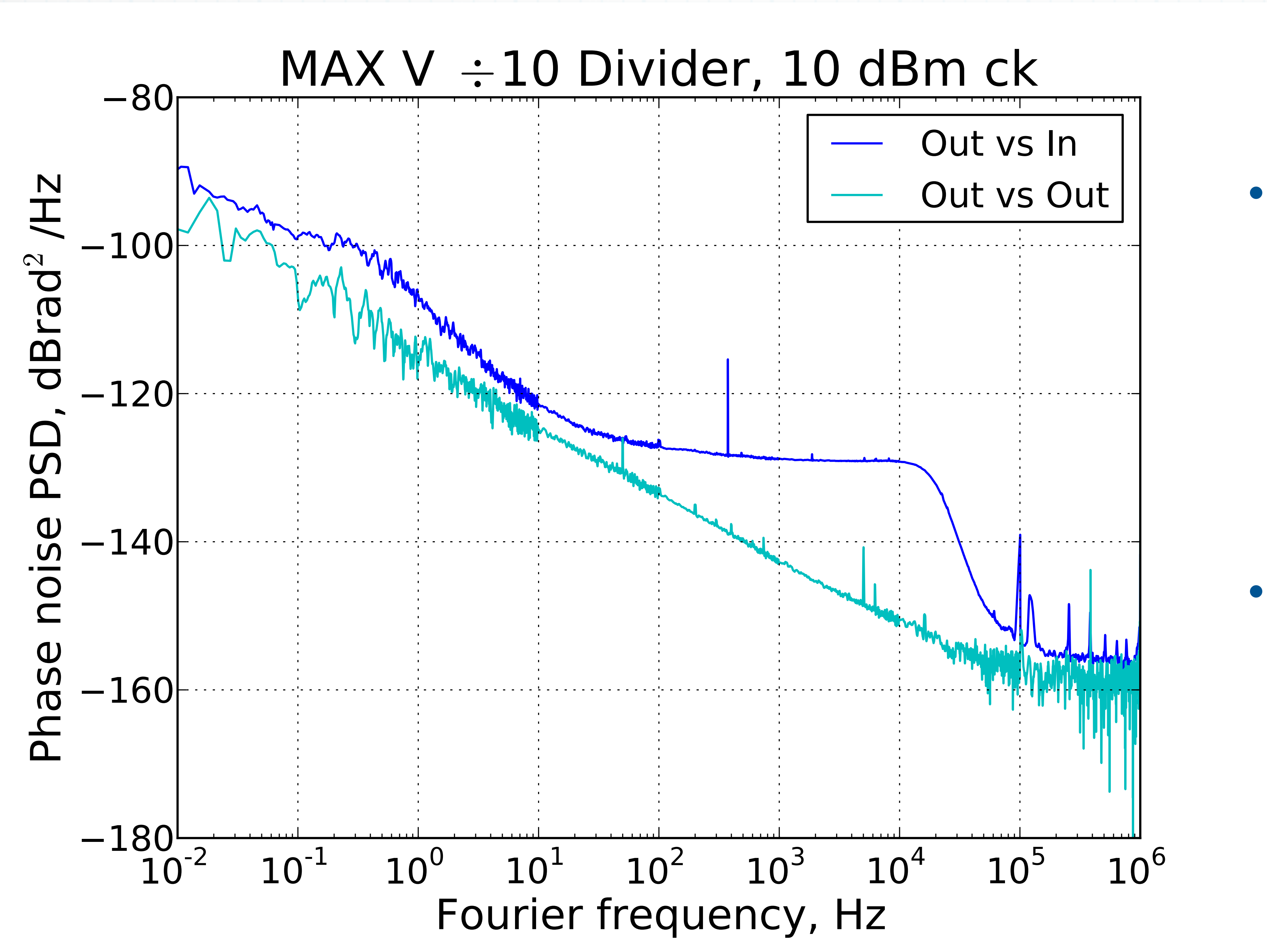
- Flicker region –> Negligible aliasing
- The Π divider is still not well explained
- The Λ divider exhibits low $1/f$ and low white noise

MAX 3000 CPLD [300 nm] (2)



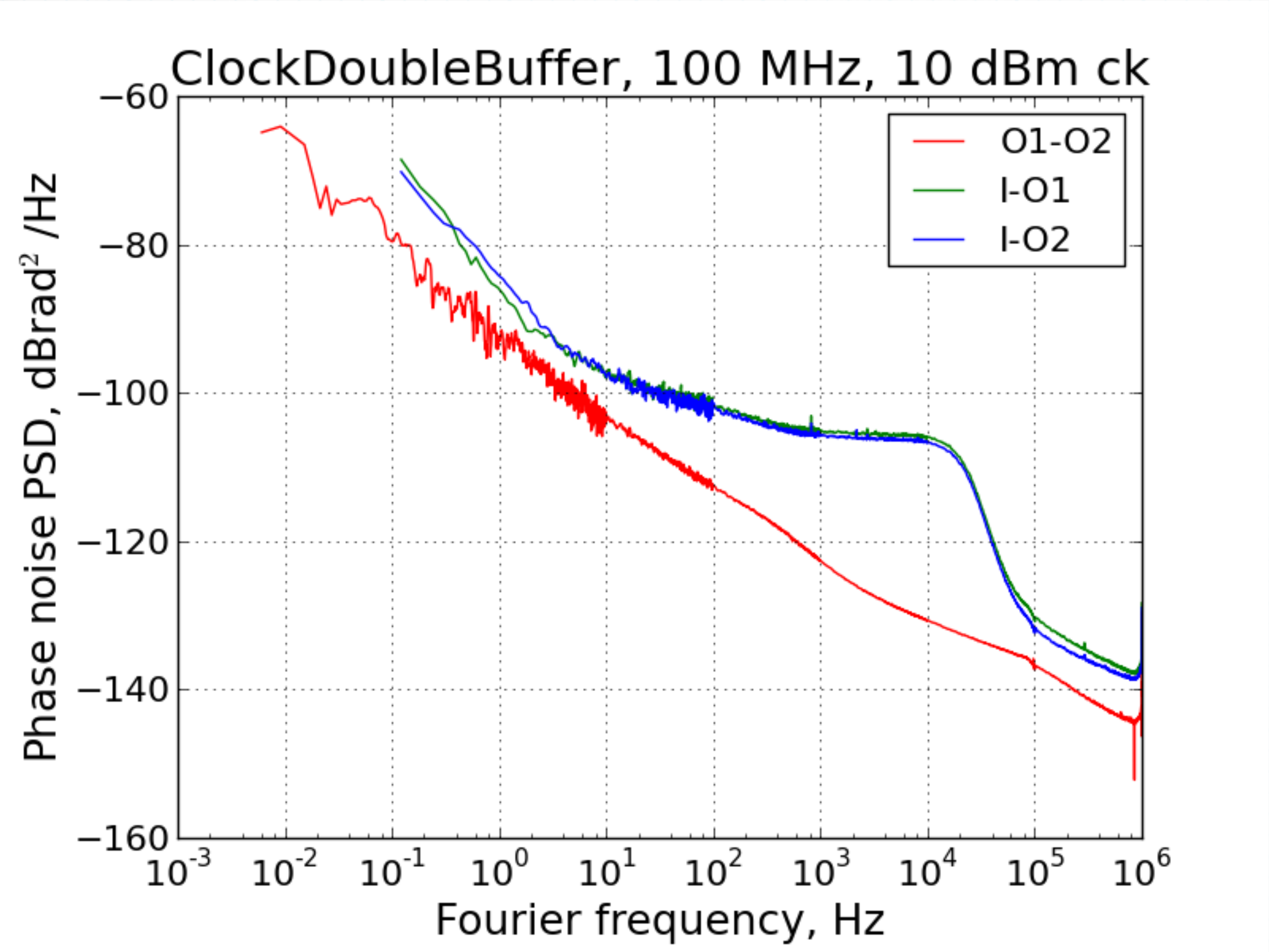
- **Slope 1/τ, typical of white and flicker PM noise**
- **The Λ divider performs $2{\times}10^{-14}$ at $\tau = 1$ s, 10 MHz output**

Max V CPLD [180 mn]



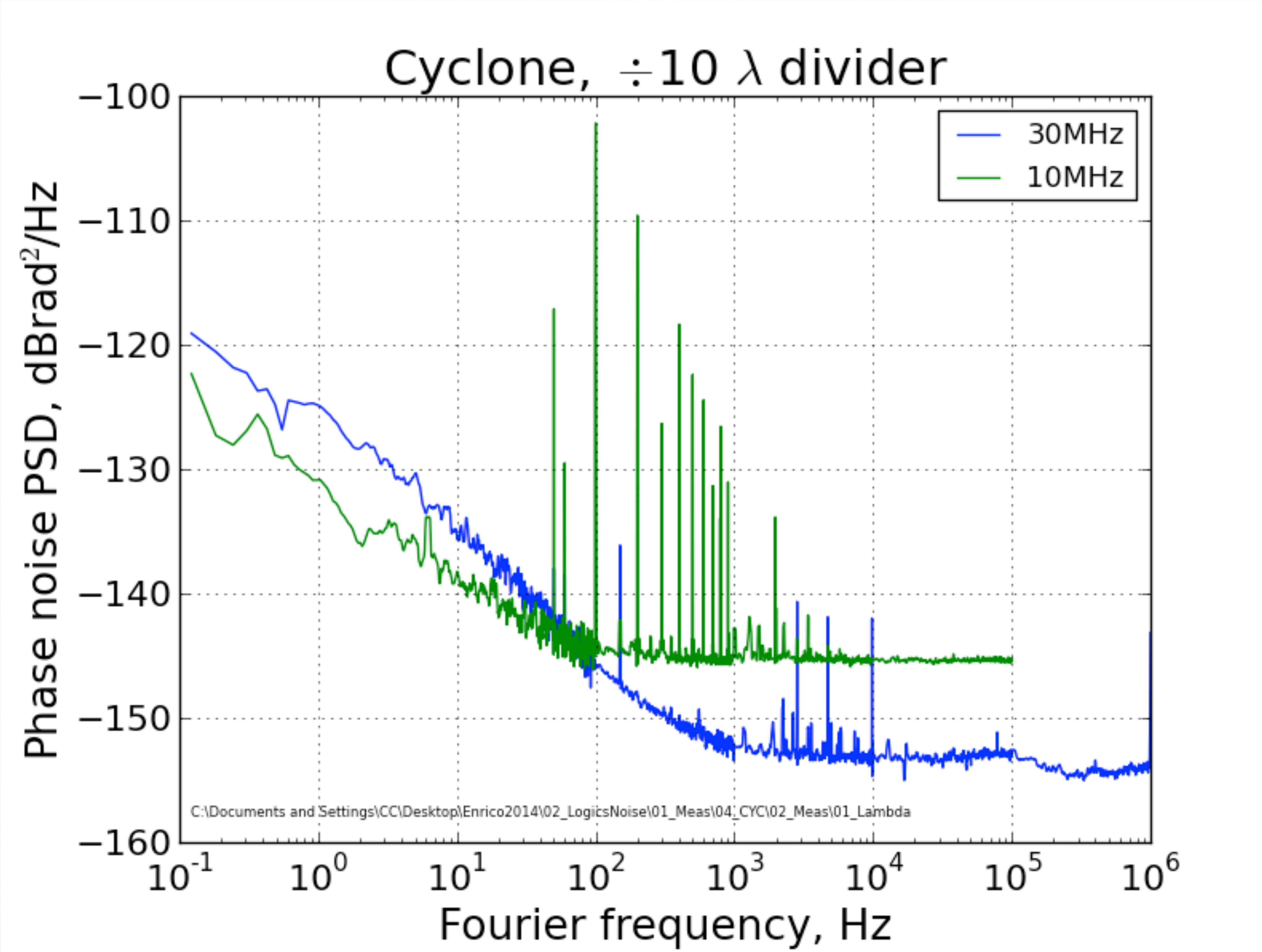
- **Two lambda dividers**
  - **output-to-output and common clock,**
  - **low *f*, emphasizes the 1/f noise**
- **Same, only output-to-output and common clock**

Max V CPLD [180 nm]

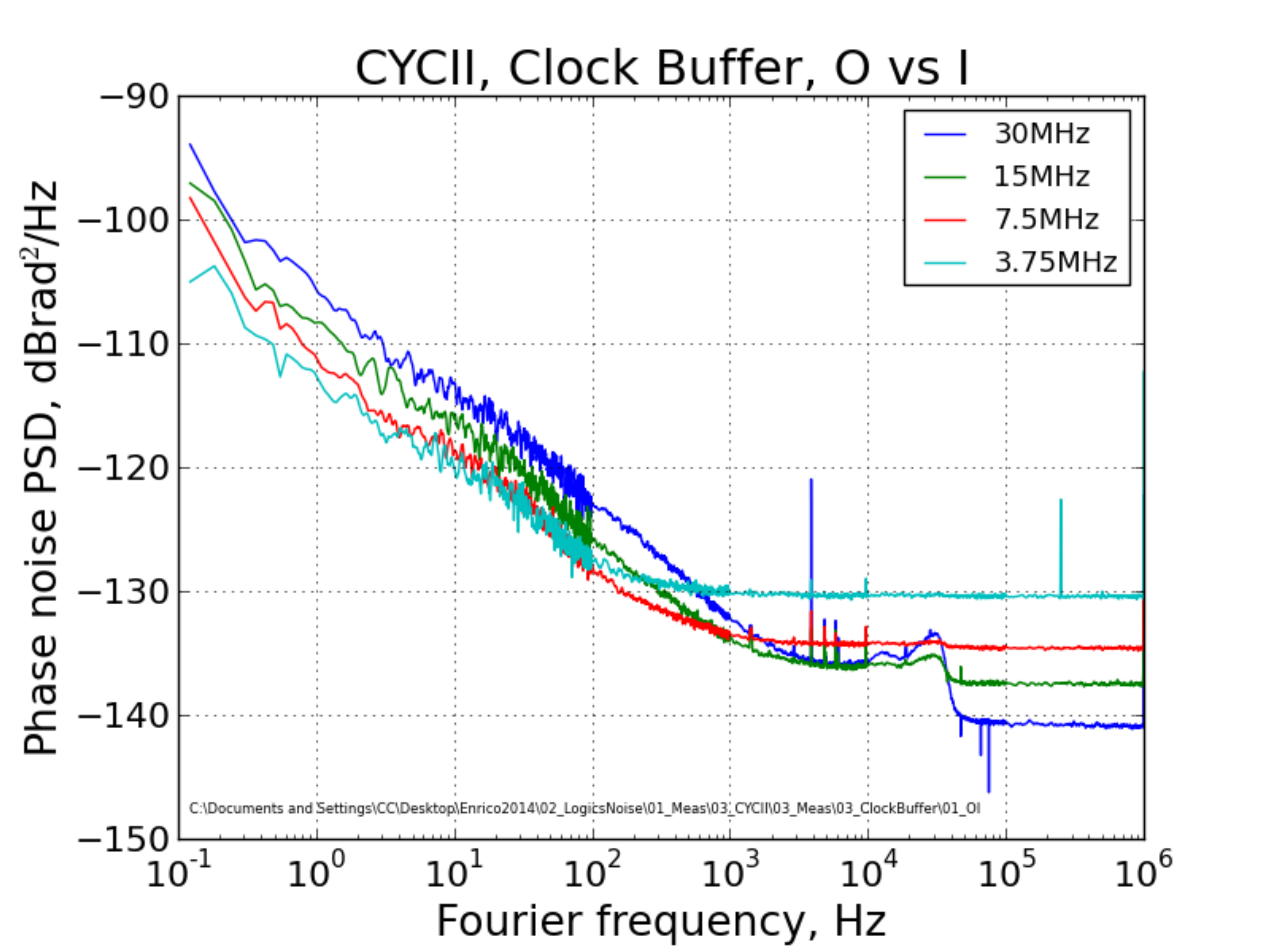


- **Two lambda dividers**
  - **output-to-output and common clock,**
  - **low *f*, emphasizes the 1/f noise**
- **Clock, difference between the two outputs**

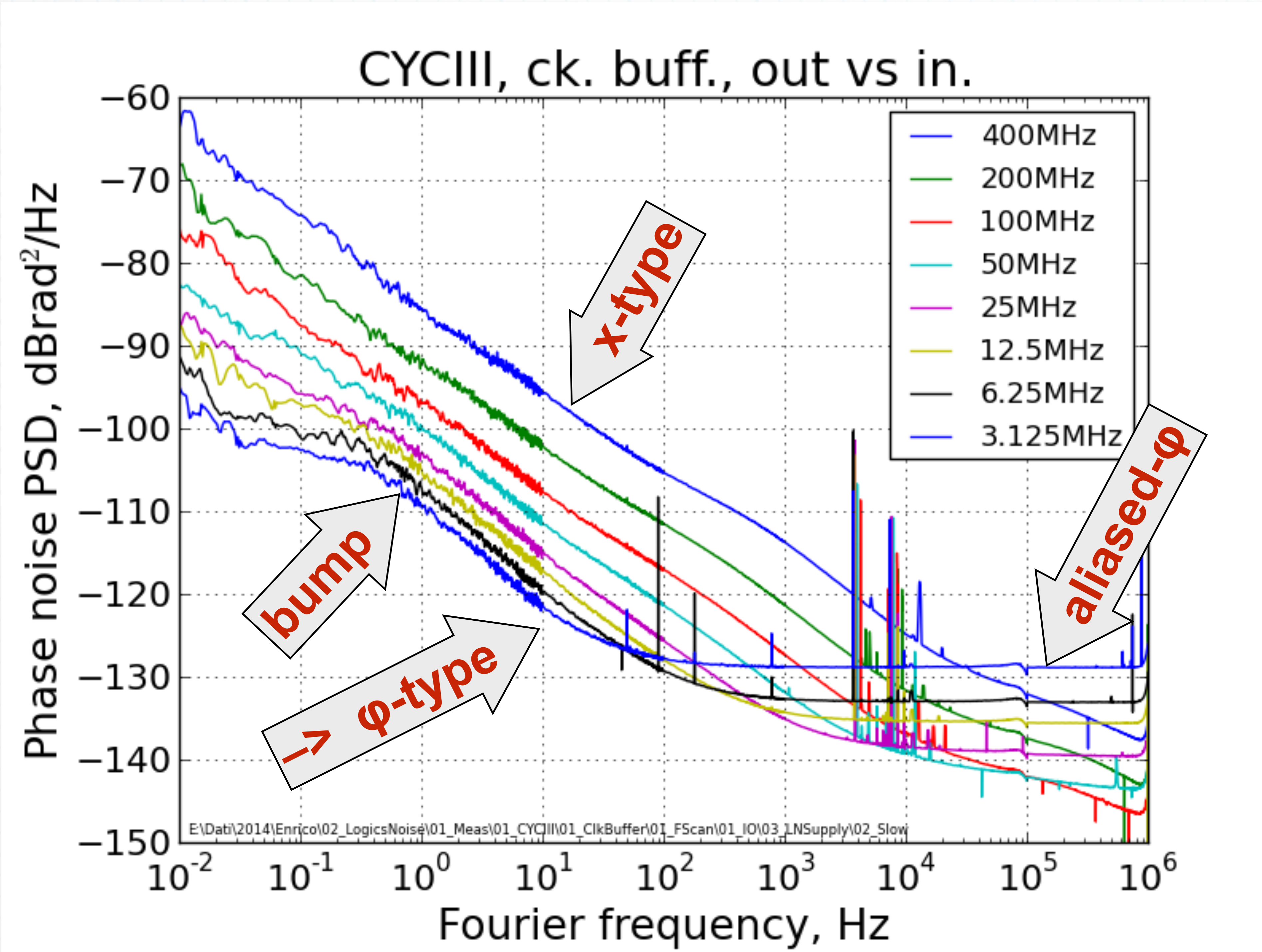
Cyclone Λ divider [90 nm]



Cyclone II Clock Buffer [90 nm]



Cyclone III Clock Buffer



Flicker

- **High ν_0 –> scales as ν_0 (x-type)**
- **Low ν_0**

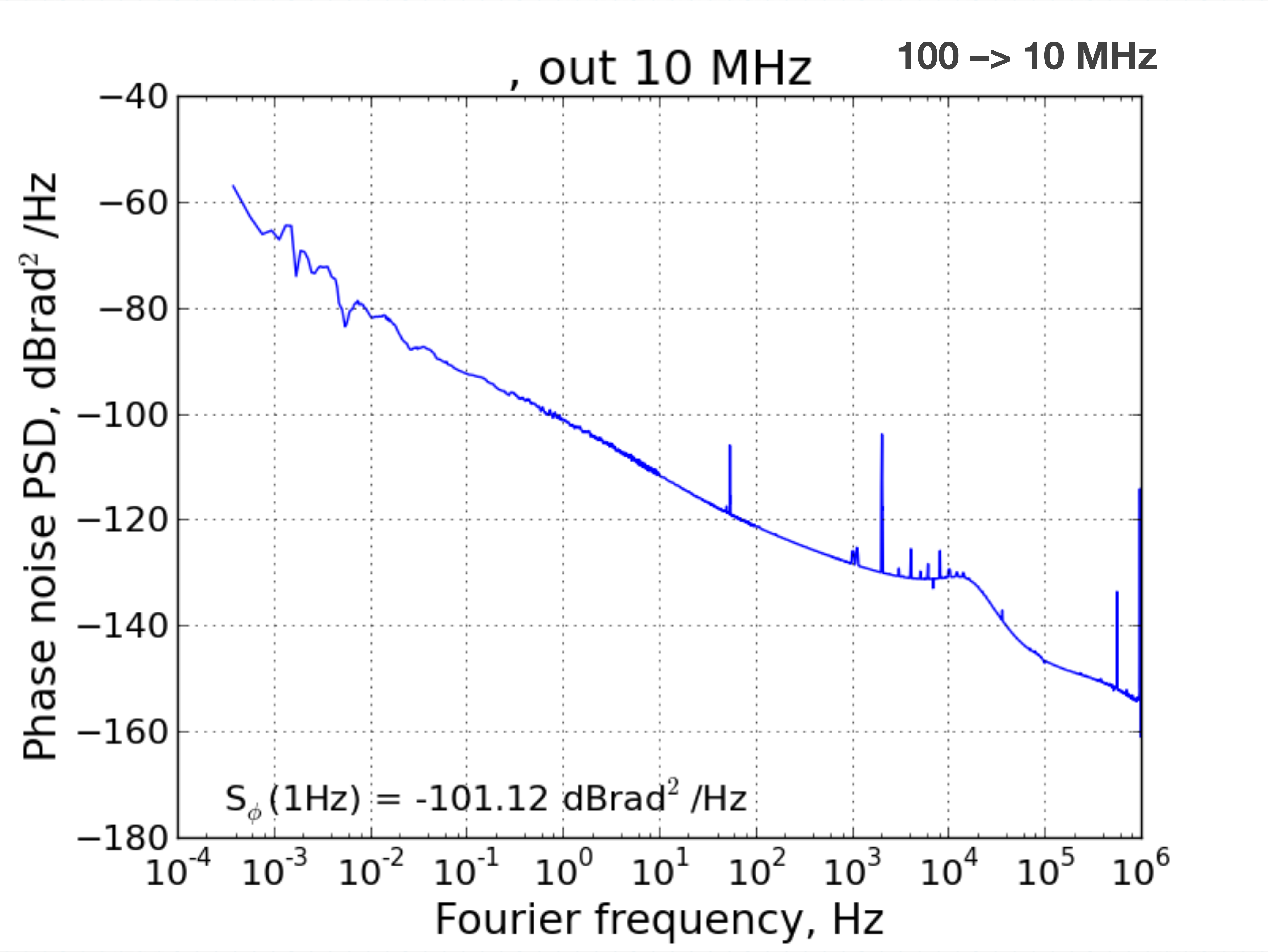
  tends to φ-type

  bumps 0.1–10 Hz

White

- **Aliasing shows up at low ν_0**

Zynq (28 nm) , Λ divider



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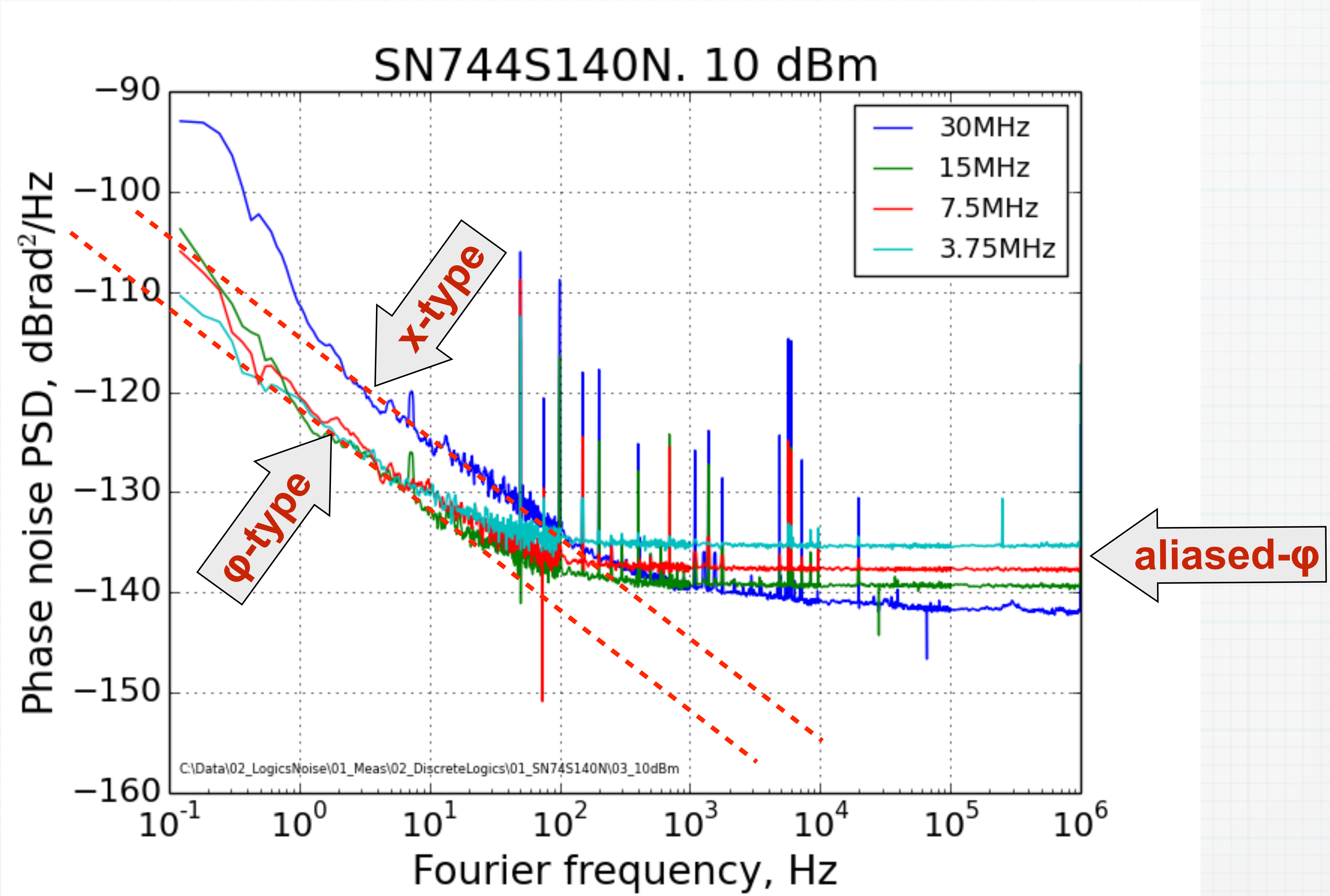
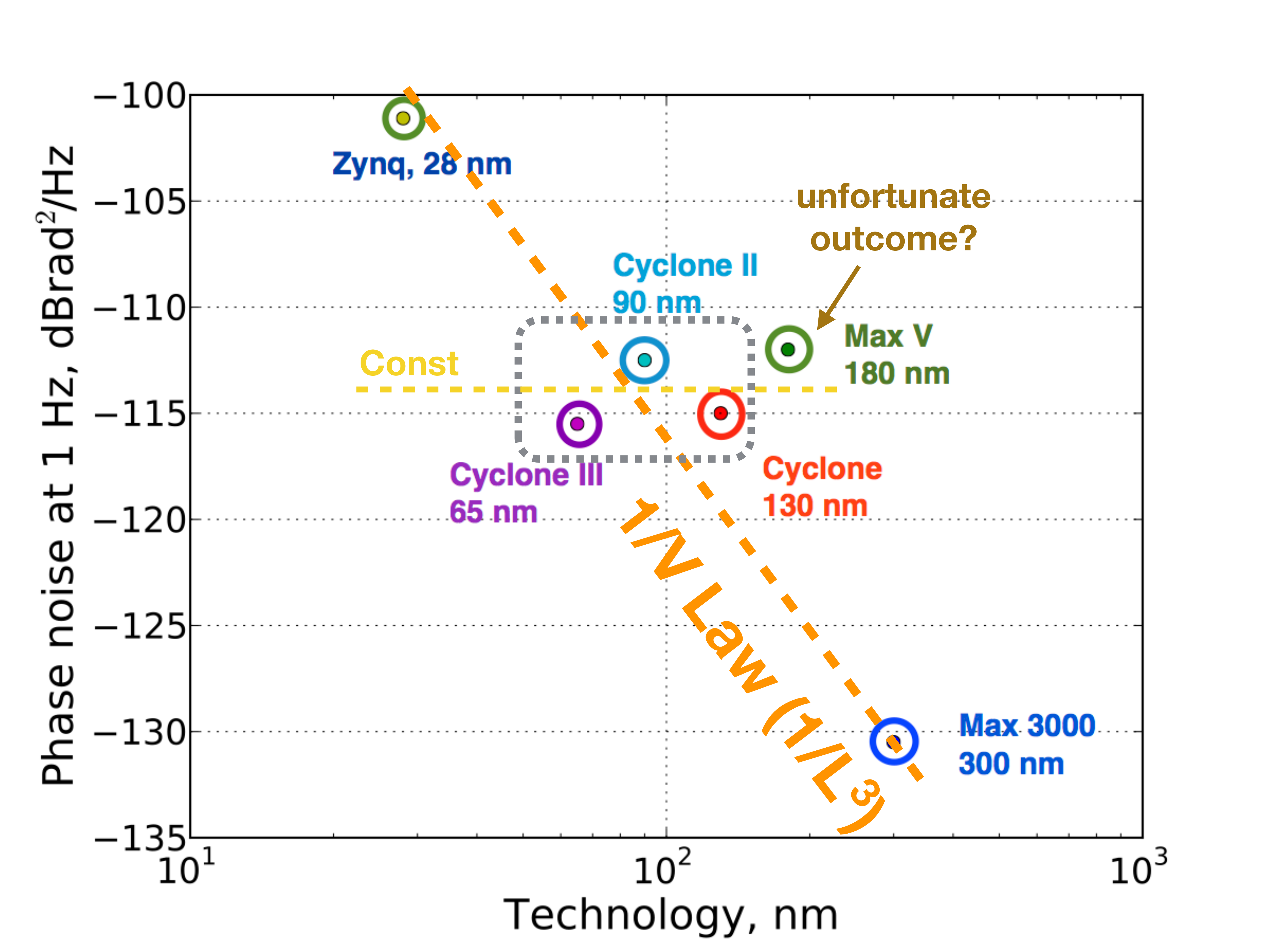
74S140 – Old TTL 50 Ω driver



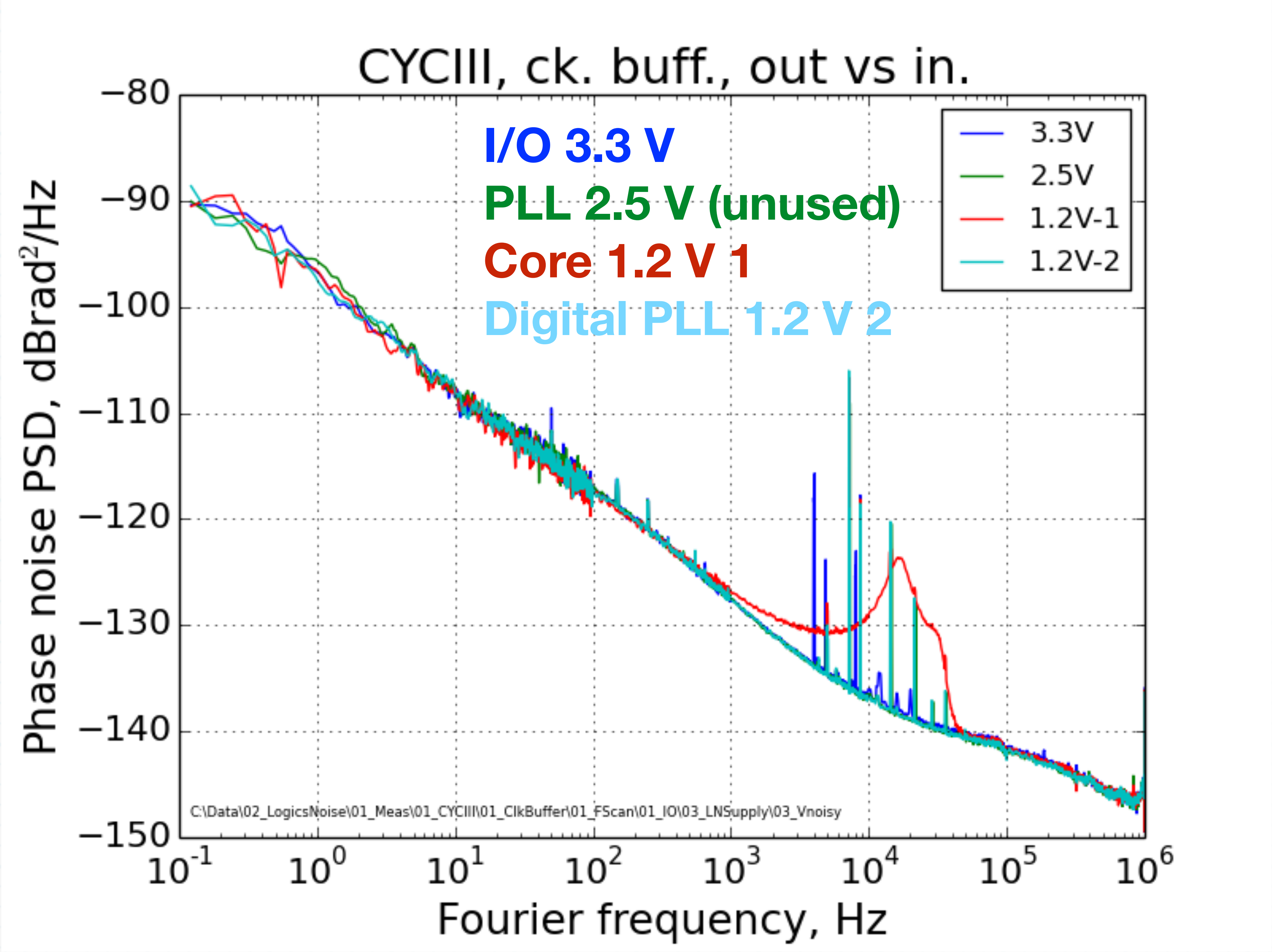
Flicker coefficient b_{-1}



Some Facts

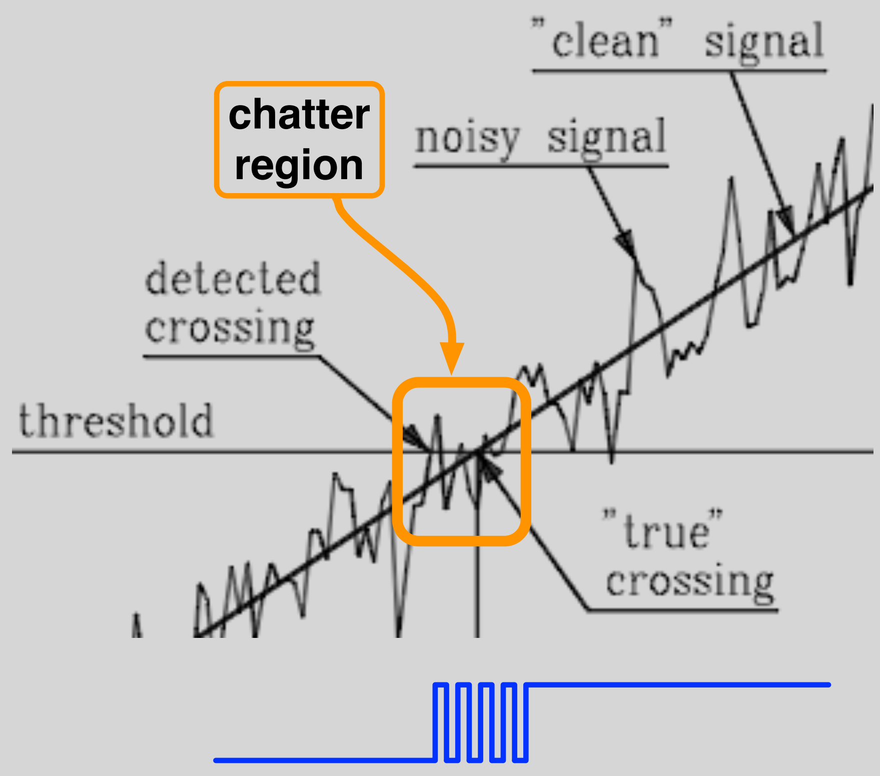
Related to Phase and Noise

Cyclone III, voltage supply



- All but one low-noise voltage supplies
- The noise is critical only in the core supply

Input Chatter (1/3)



Chatter occurs when the RMS Slew Rate of noise exceeds the slew rate of the pure signal

Pure signal

$$x(t) = V_0 \cos(2\pi\nu_0 t)$$

$$\mathrm{SR} = 2\pi\nu_0 V_0$$

Wide band noise

$$\langle \mathrm{SR}^2 \rangle = 4\pi^2 \int_0^B f^2 S_V(f)\, df$$

$$= \frac{4\pi^2}{3}\sigma_V^2 B^2 \quad (\mathrm{rms})$$

Chatter threshold

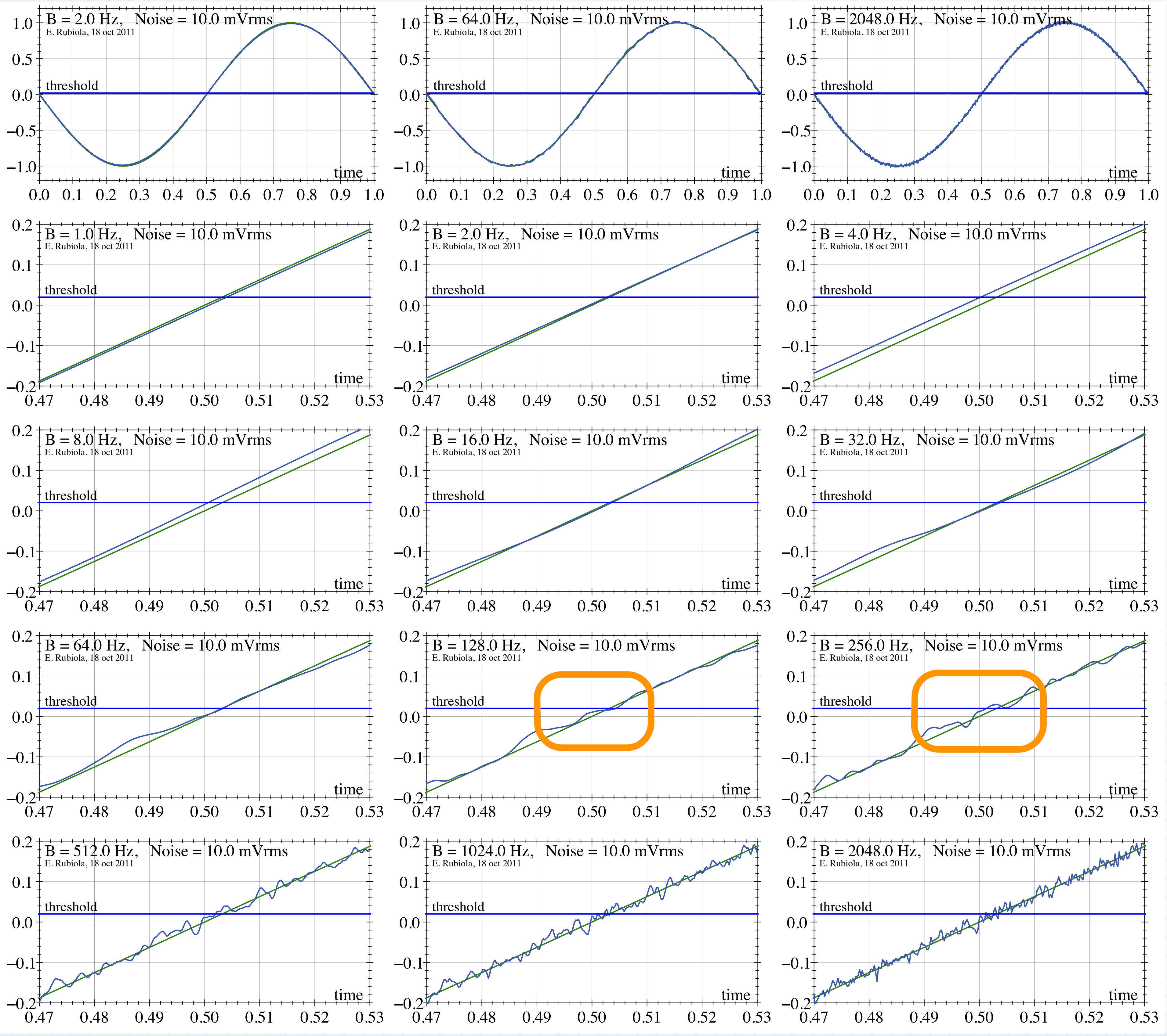
$$\nu_0^2 = \frac{1}{3}\frac{S_v B^3}{V_0^2}$$

Example

- 200 mVp signal
- 10 nV/√Hz noise
- 1 GHz max –> 3 GHz noise BW
- Chatter threshold ν = 4.7 MHz

With high-speed devices, chatter can occur at unexpectedly high frequencies

Simulation of Chatter (2/3)



Conditions

ν_0 = 1 Hz,

V_0 = 1 V_{peak}

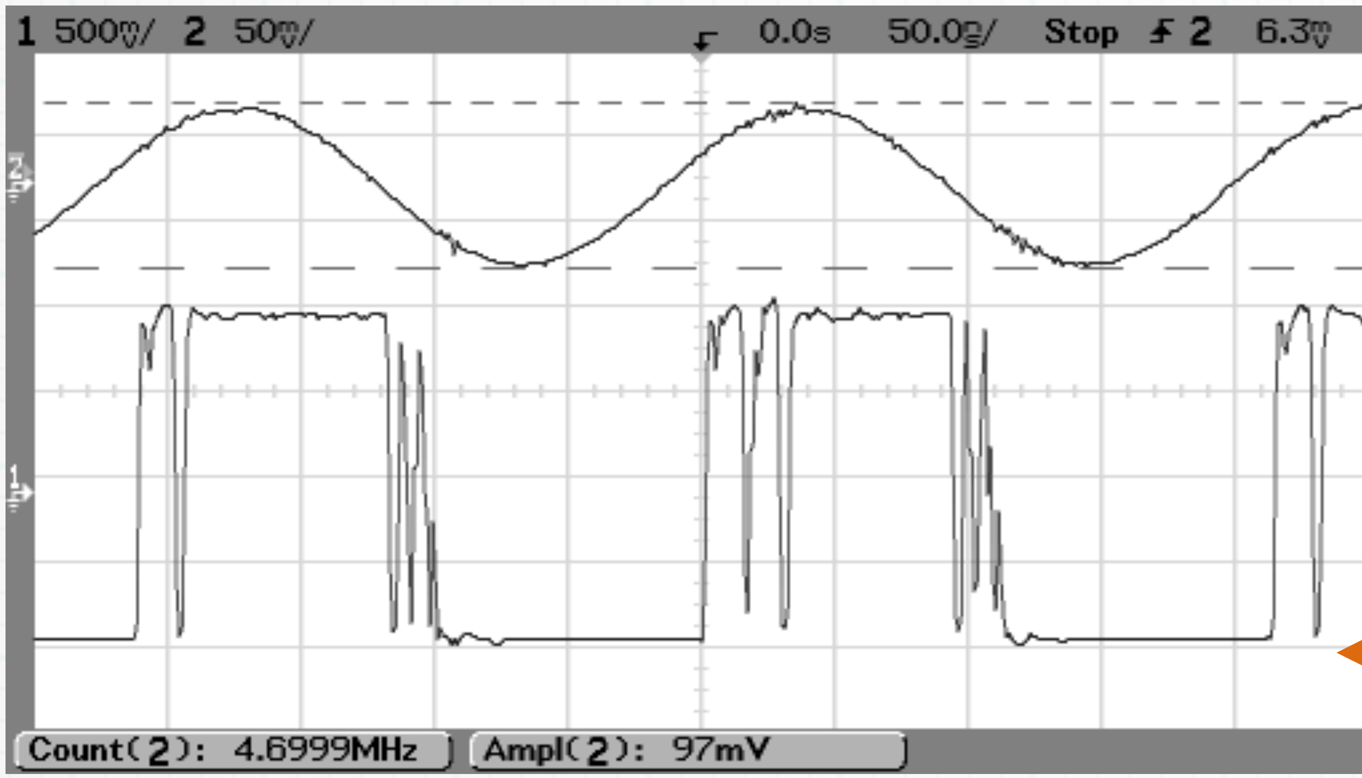
$\sqrt{\langle v_0^2 \rangle}$ = 10 mV rms noise

Noise BW increases in powers of 2

De-normalize for your needs

Input chatter – Example (3/3)

Fairly good agreement with theory

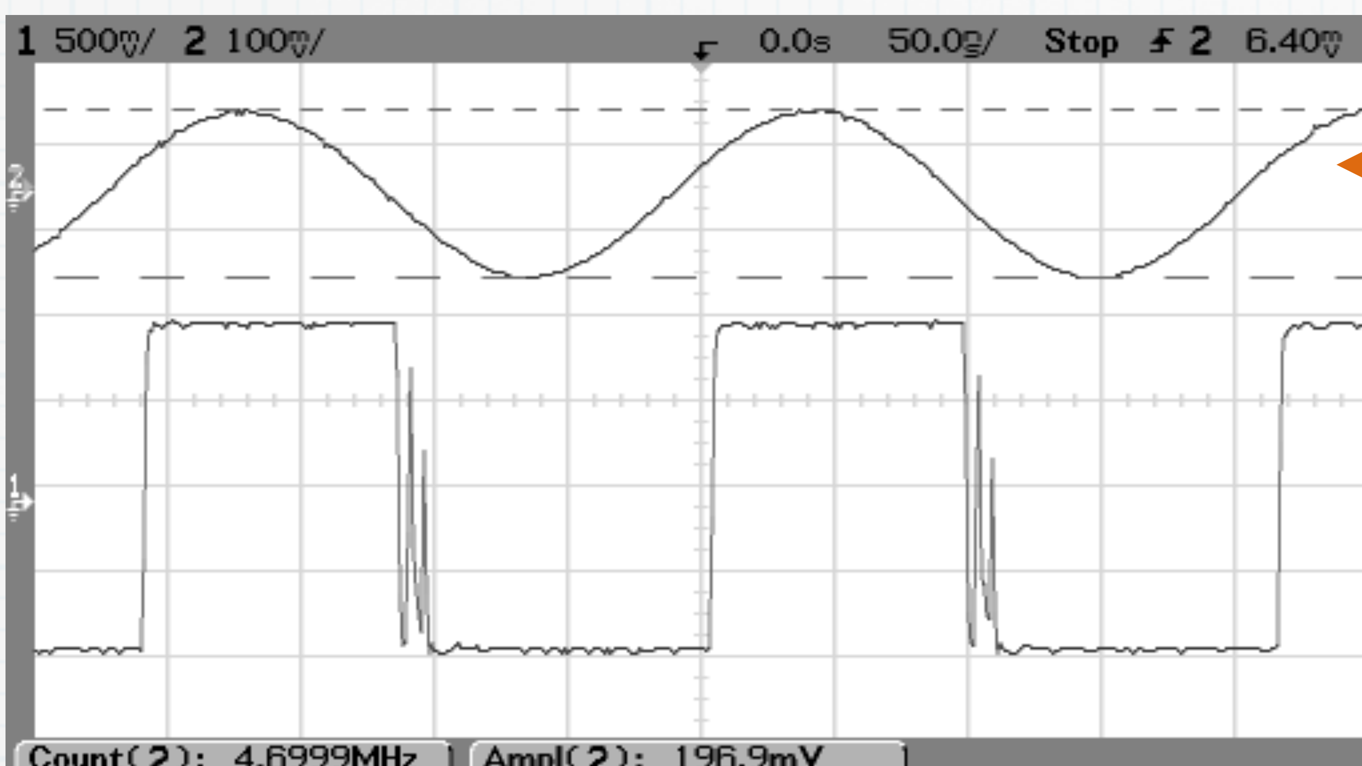


Experiment

- Cyclone III FPGA
- Estimated noise 10 nV/√Hz
- Estimated BW 2 GHz

$2V_0$ = 100 mV_{pp}

ν_0 = 4.7 MHz



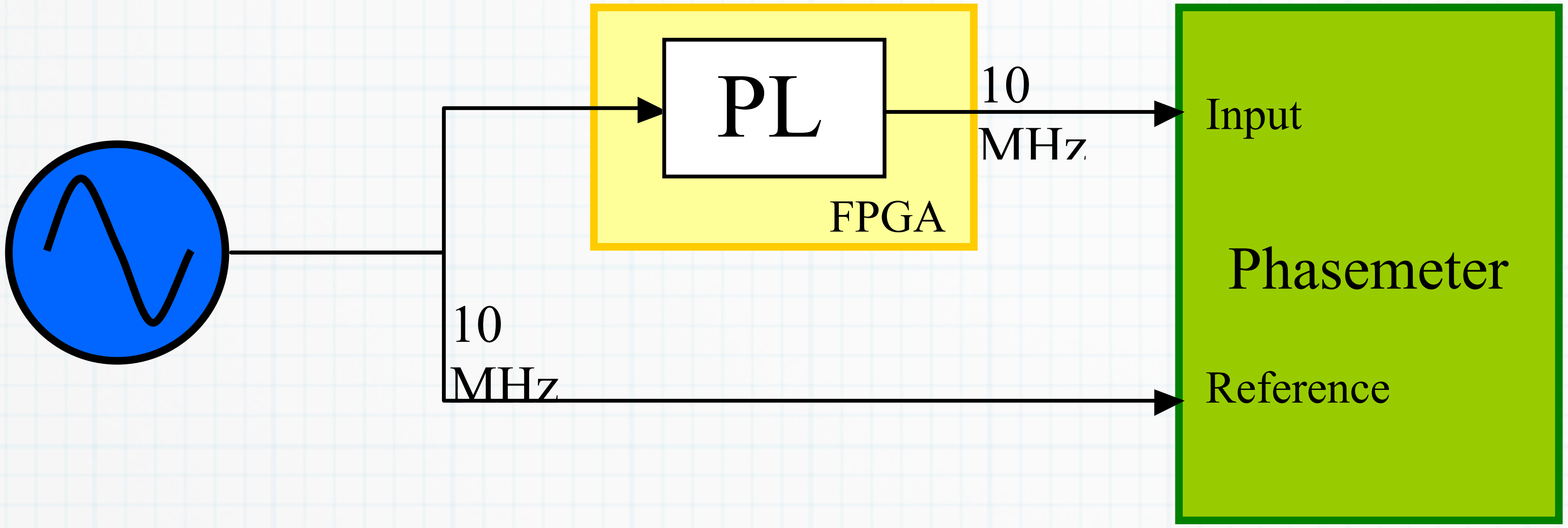
$2V_0$ = 200 mV_{pp}

ν_0 = 4.7 MHz

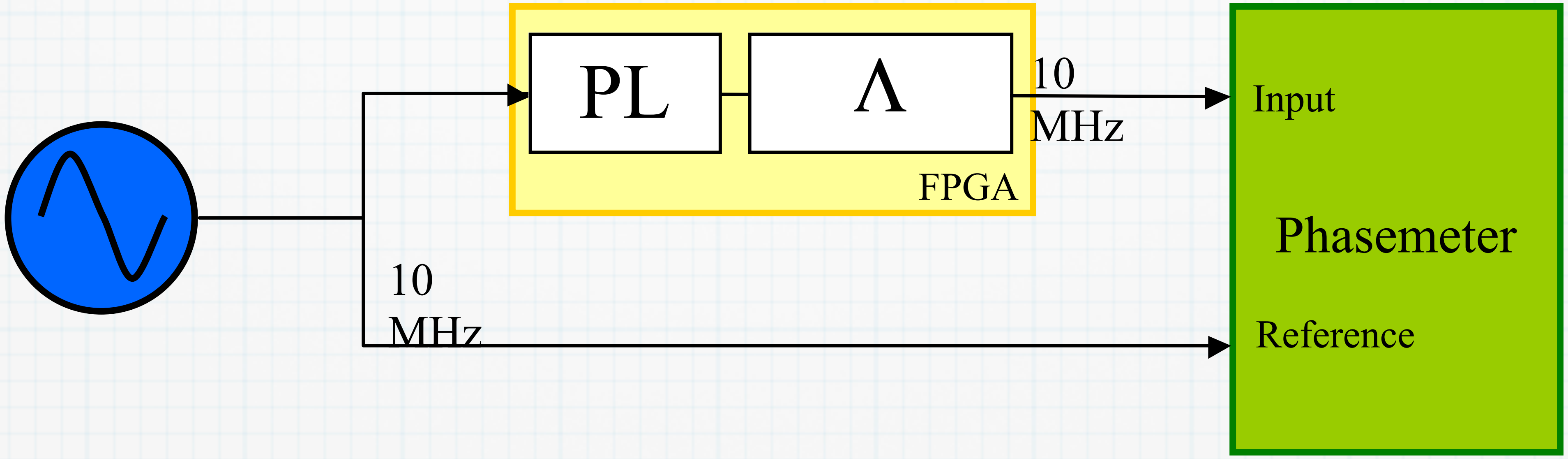
Asymmetry shows up

Explanation takes a detailed electrical model, which we have not

Cyclone III Internal PLL (1/3)

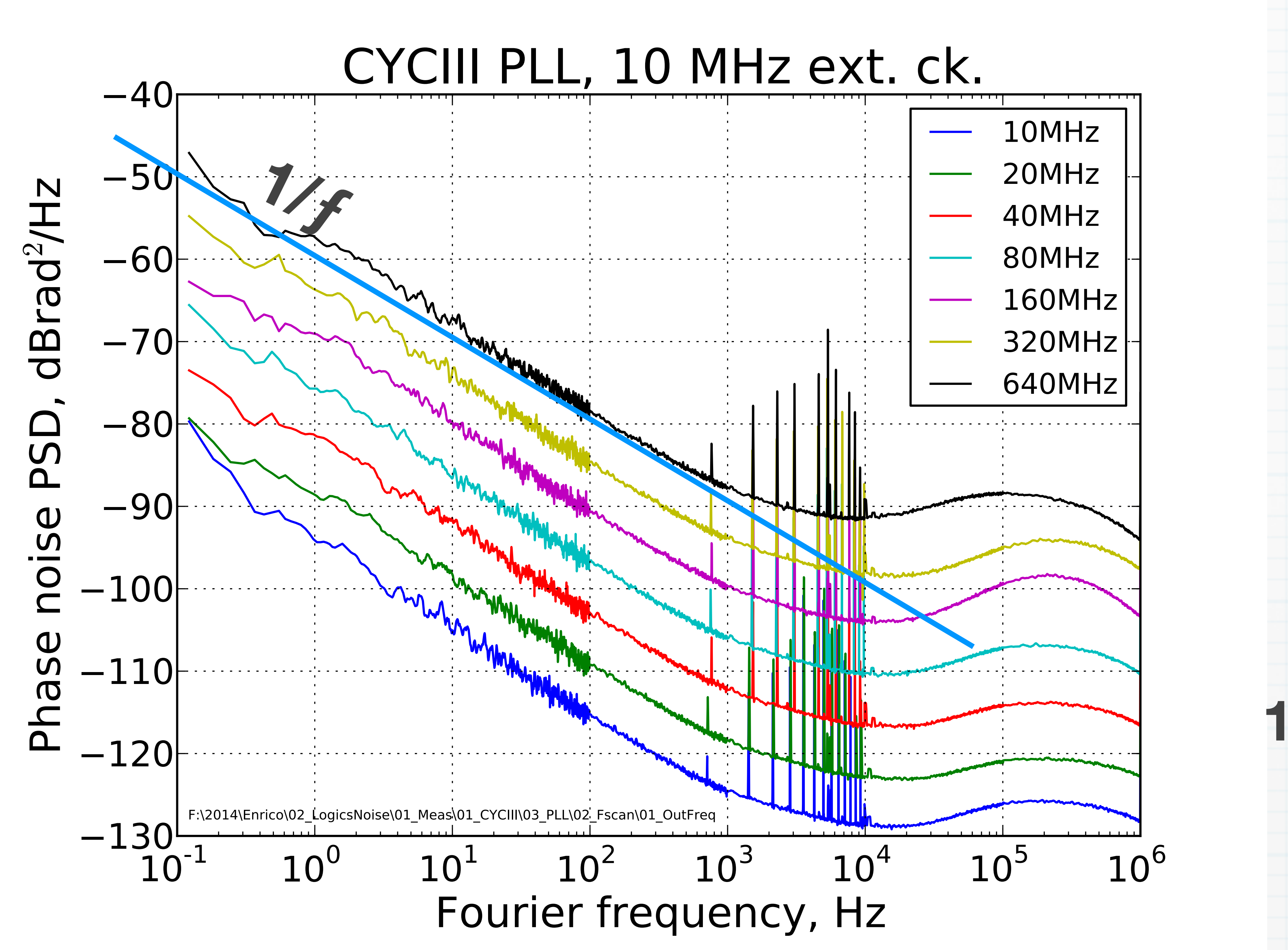


Symmetricom
5120A (30 MHz max)



- **A Λ divider (inside the FPGA) enables the measurement**
  - **The divider noise is low enough**
  - **A trick to work at low frequency**

Cyclone III Internal PLL (2/3)



PLL used as a multiplier

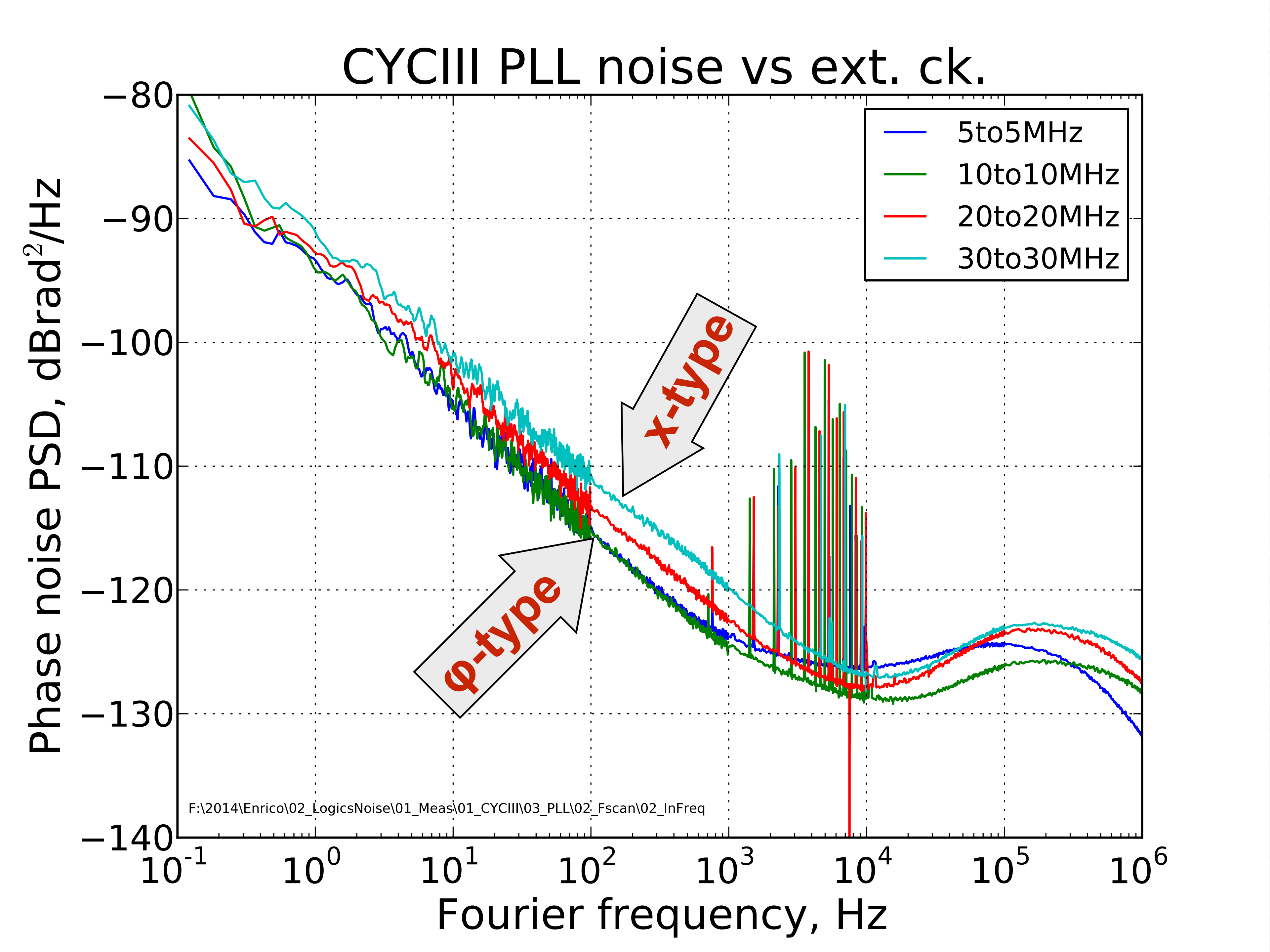
10 MHz input

N x 10 MHz out

Stability
1.5x10–12 @ 1 s
(f_H = 500 Hz)

- **1/ƒ phase noise is dominant**
- **Scales as xN^2 –> gear work**

Cyclone III Internal PLL (3/3)



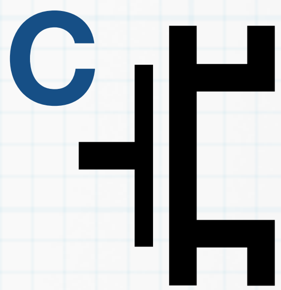
PLL used as a buffer

Same frequency at input and output

Crossover between phi-type and x-type at 20 MHz

- **φ-type 16 μrad/√Hz @ 1 Hz**
- **x-type 220 fs/√Hz @ 1 Hz**

Thermal effects (1/3)

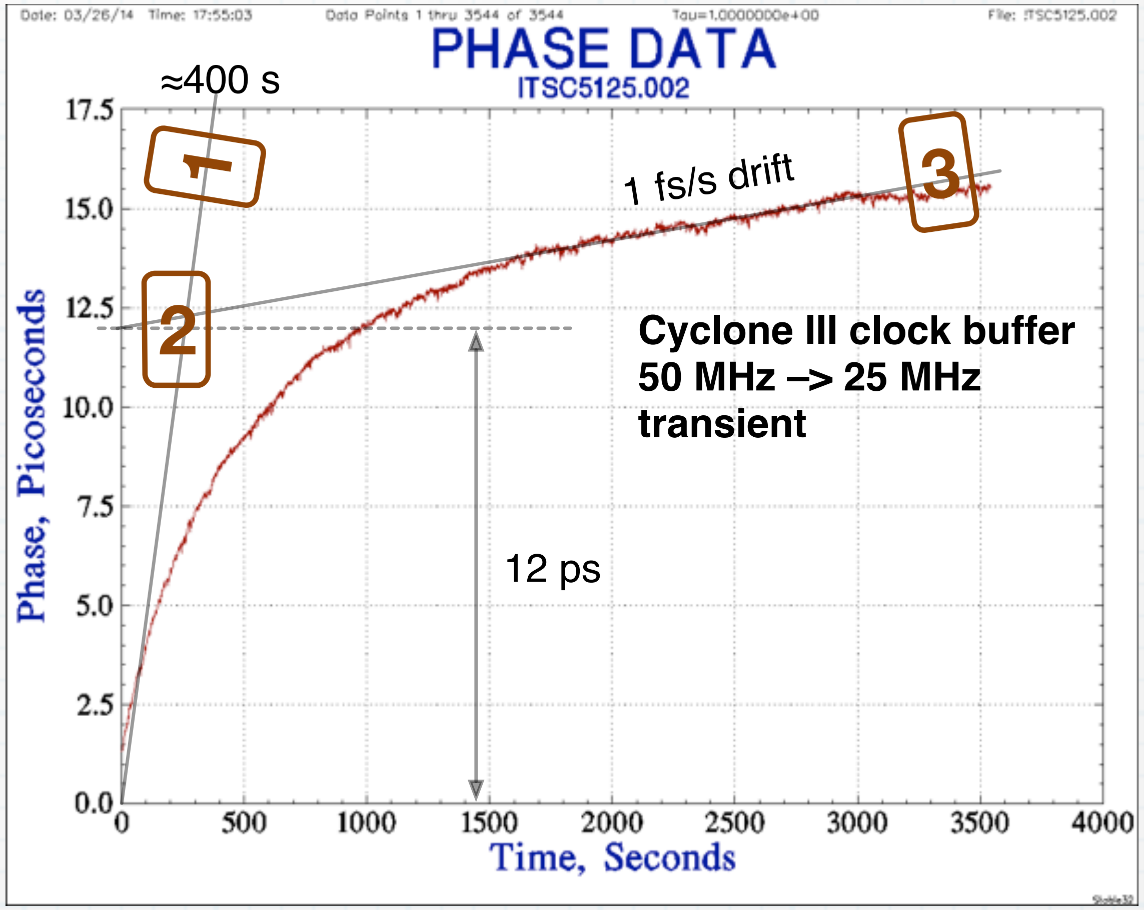


Principle

- FPGA dissipation change ΔP by acting on frequency
- Energy $E = CV^2$ dissipated by the gate capacitor in a cycle

Conditions

- Cyclone III used as a clock buffer
- Environment temperature fluctuations are filtered out with a small blanket (necessary)
- Two separate measurements (phase meter and counter) –> trusted result



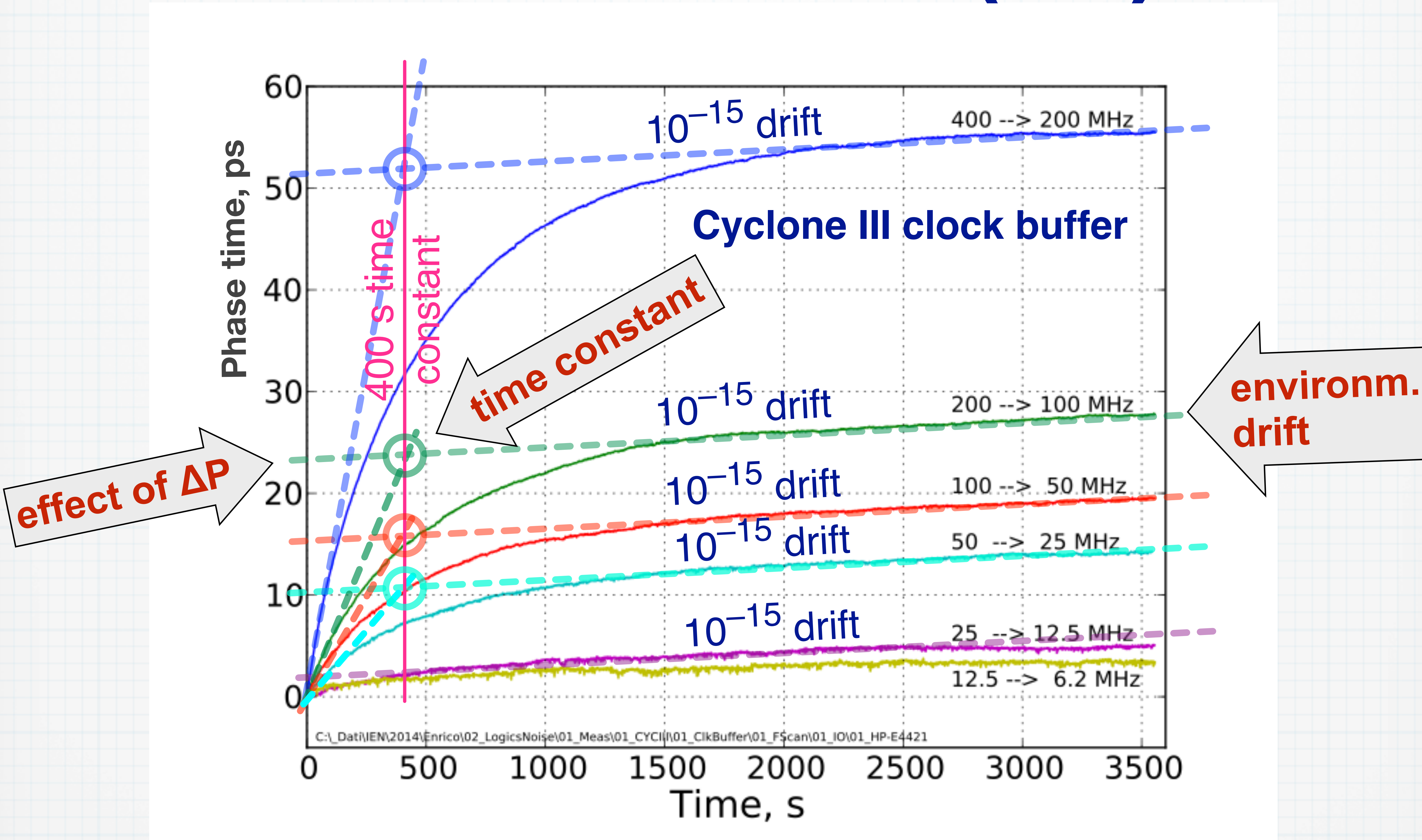
Outcome (Left to right)

(1) Thermal transient, due to the change of the FPGA dissipation

(2) Overall effect of ΔP

(3) Slow thermal drift, due to the environment

Thermal effects (2/3)

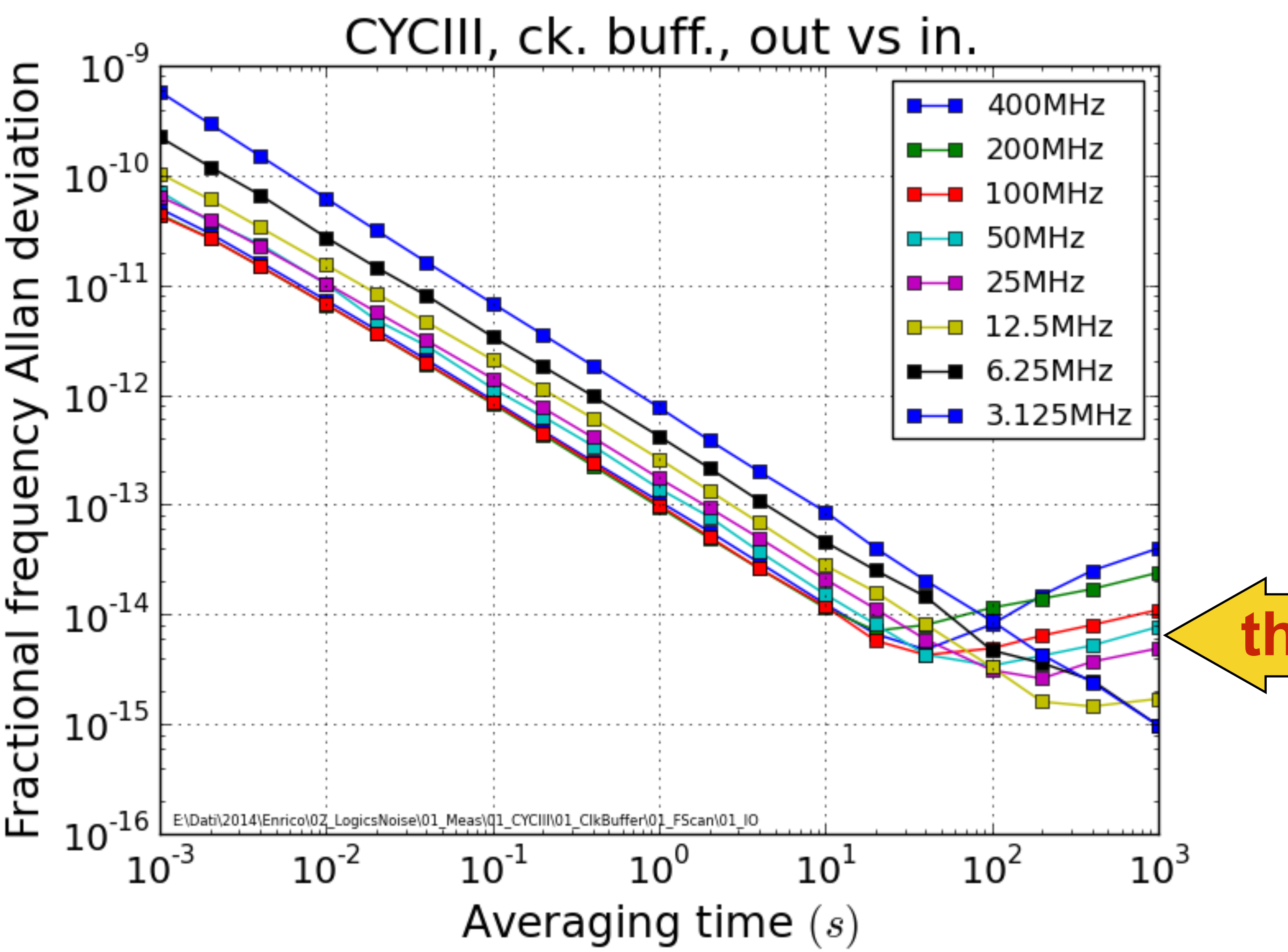


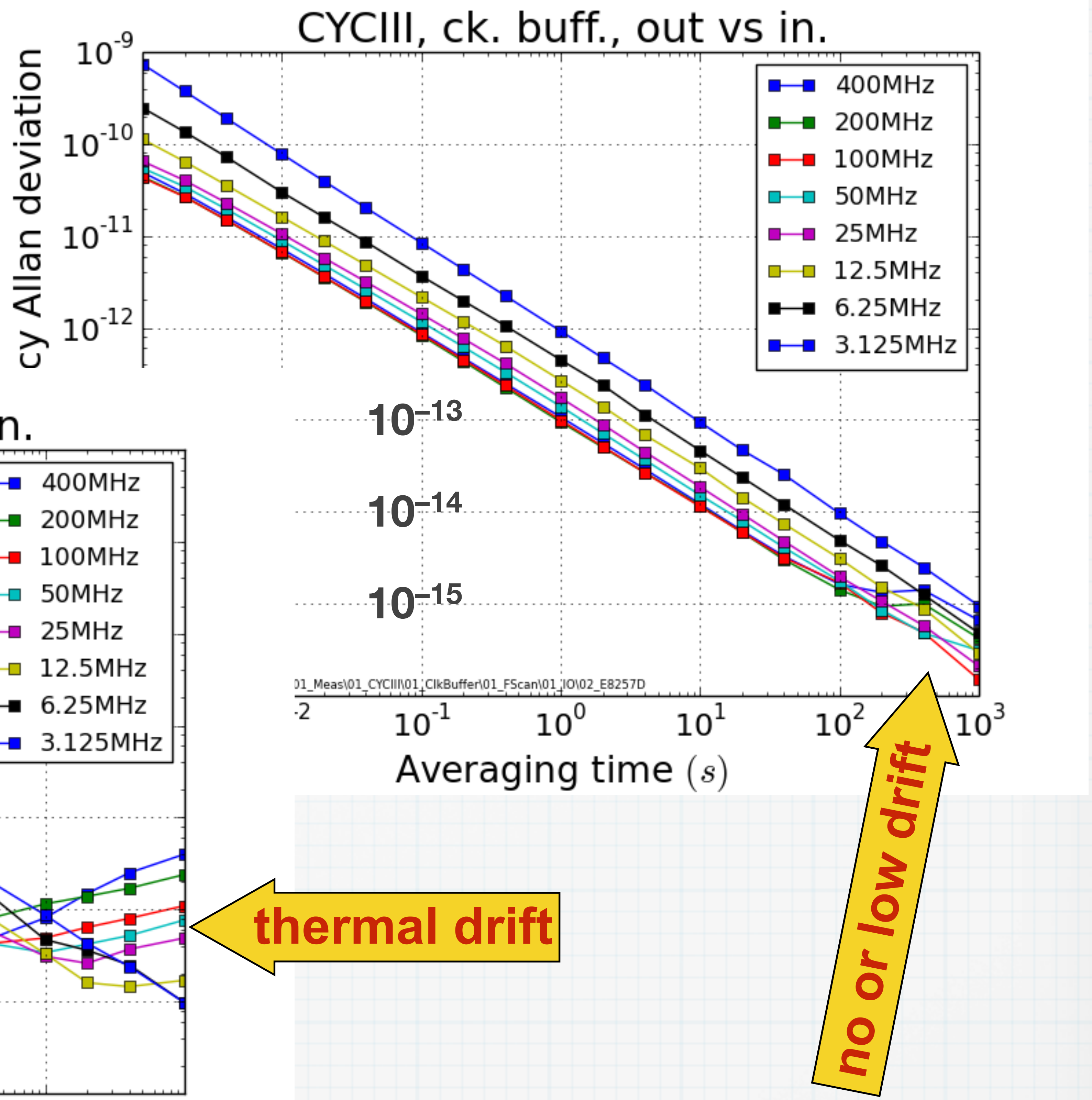
Warning: In real applications, other parts of the same FPGA impact on the temperature, thus on phase – drift is possible

Thermal effects (3/3)

1 H dead time after changing ν_0

Measurement starts immediately after changing ν_0

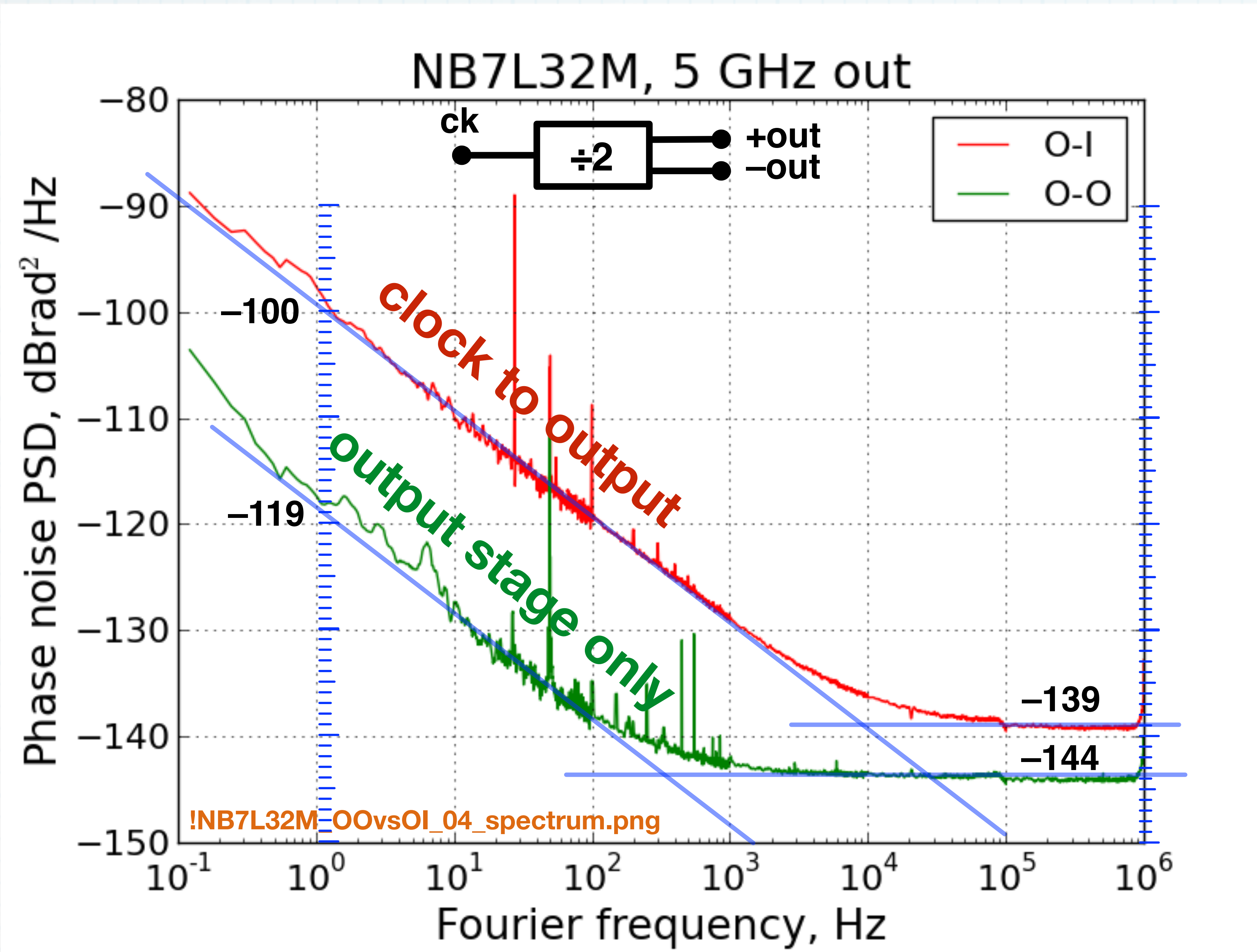




Phase Noise in Microwave Dividers

NB7L32M ÷2 µwave divider

10 GHz ÷ 2 = 5 GHz

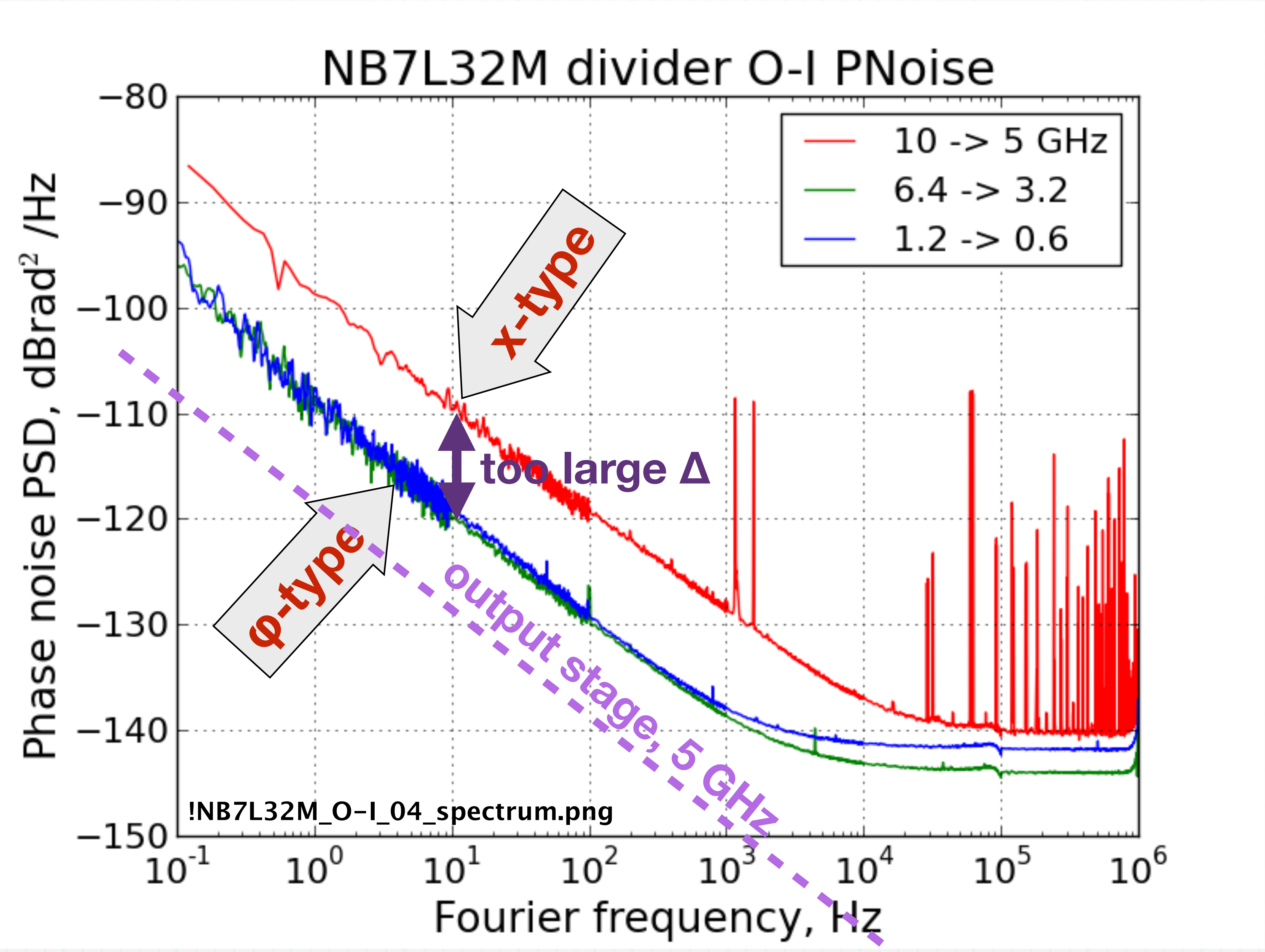


Method

- Compare two dividers
- Use 5.01 GHz as a common oscillator, and beat
- Digital PM noise measurement at 10 MHz
- O-I: Two equal dividers
- O-O: Two outputs of the same divider
- Shown: spectrum of one divider

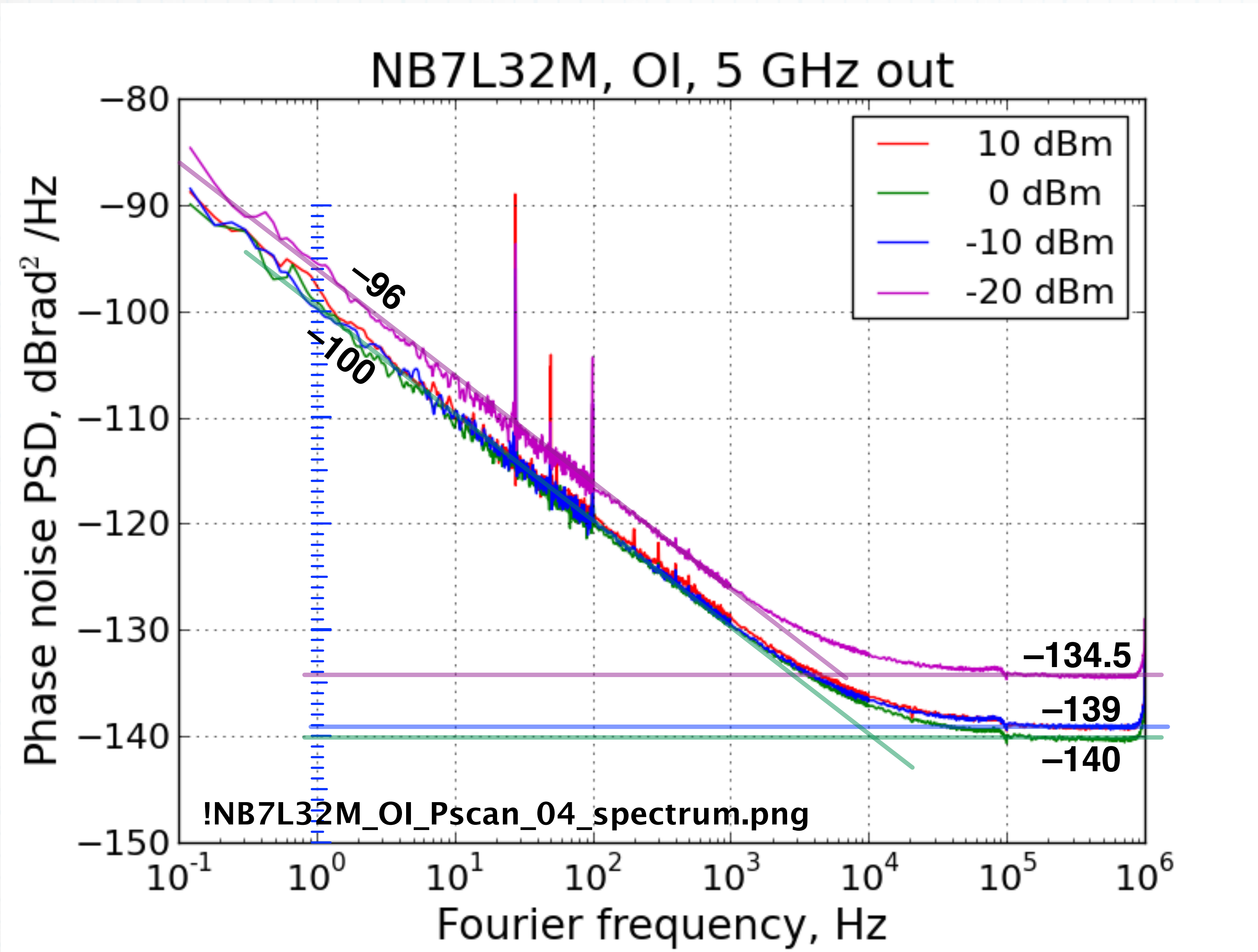
NB7L32M ÷2 µwave divider

Phase noise vs input frequency



NB7L32M ÷2 μwave divider

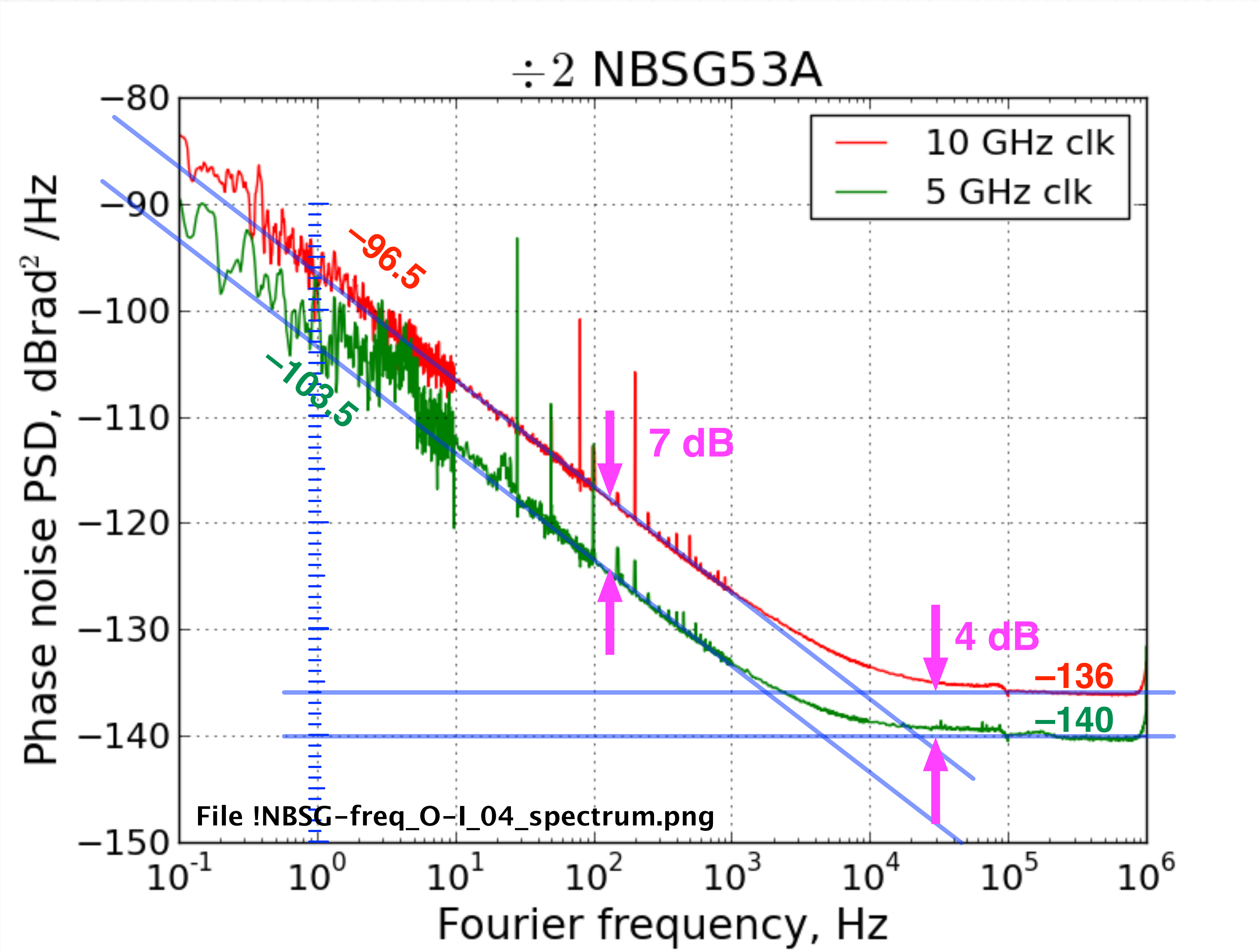
Works fairy well even at low input power (useful)



Notes

- At –16 dBm the white noise increases by 3 dB
- The critical power where $(b_0)_\varphi = (b_0)_x$ is –16 dBm
- Hence $(b_0)_{x\text{-type}} \approx -140$ dB

NBSG53A SiGe ÷2 μwave divider



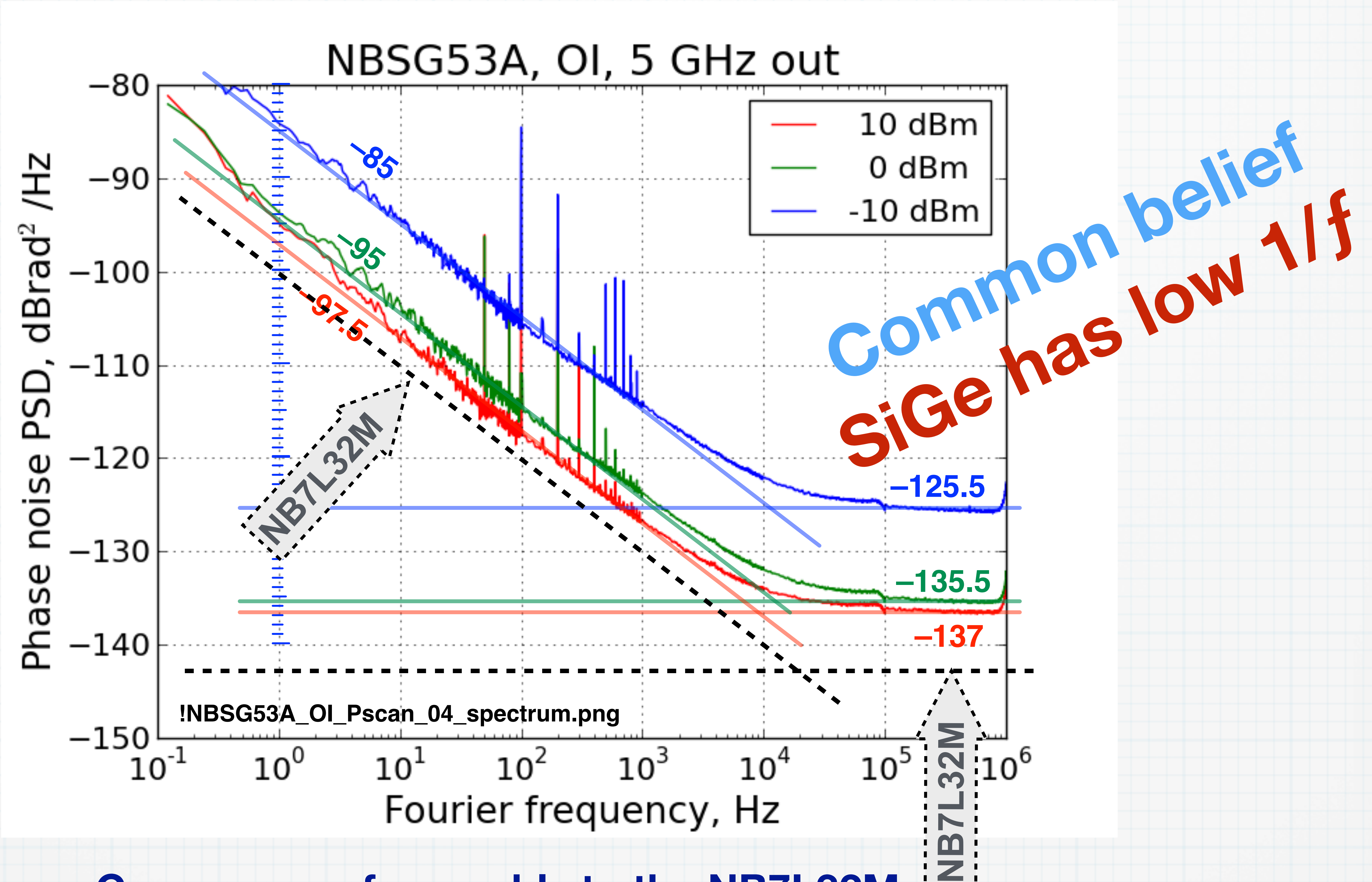
Method

- Use 5.01 (2.51) GHz as a pivot oscillator, and mixers
- Digital PM noise measurement at 10 MHz
- One divider shown

- $1/f$ –> pure gearbox model (as expected)
- White –> aliased gearbox model (as expected)
- Likely, 1 dB discrepancy in w and 1/f (mixer response)

Debugged:
–97.5 and –137

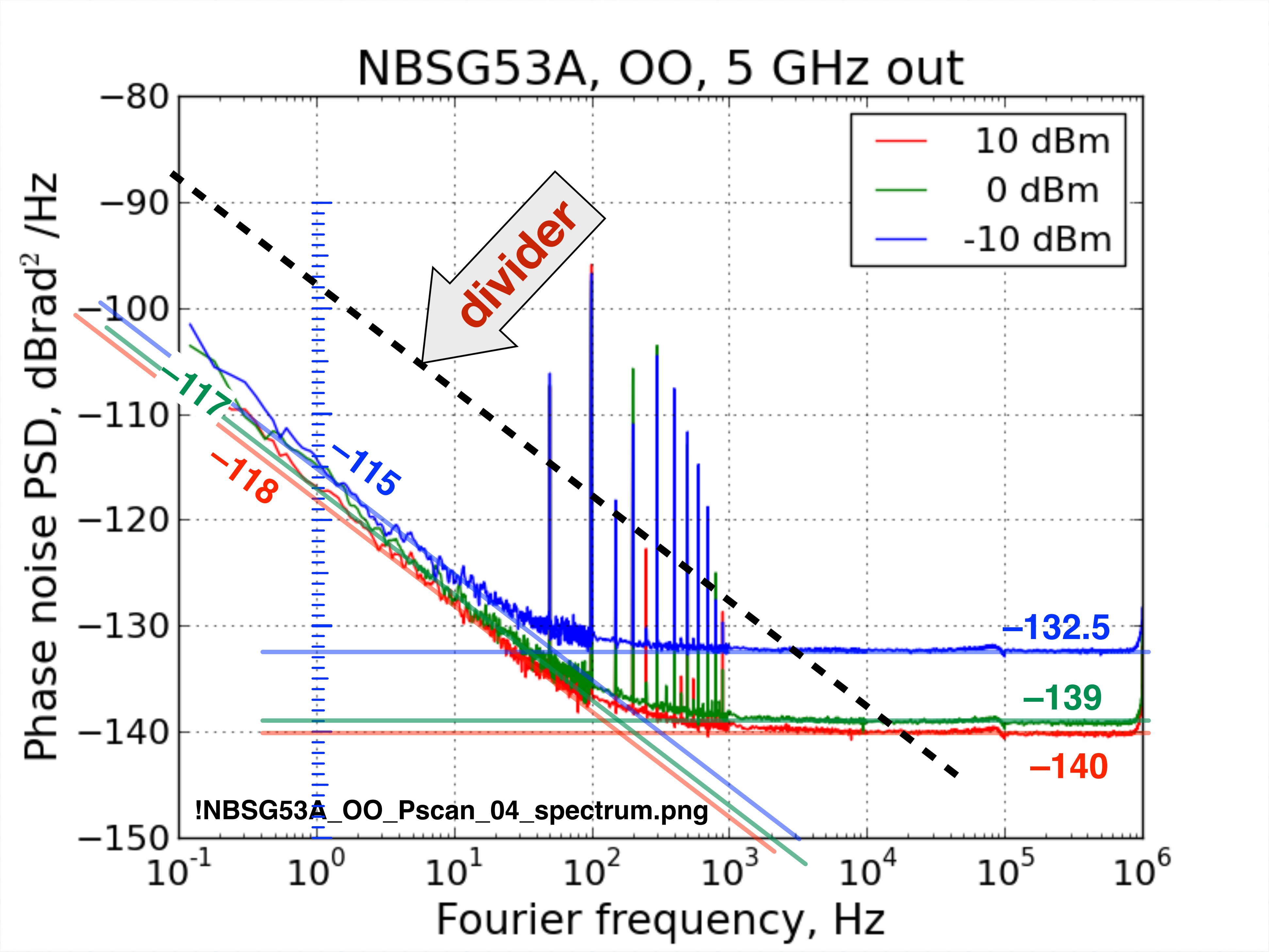
NBSG53A SiGe ÷2 μwave divider



- **Compares unfavourably to the NB7L32M**
- **More noise and less tolerance to low power**

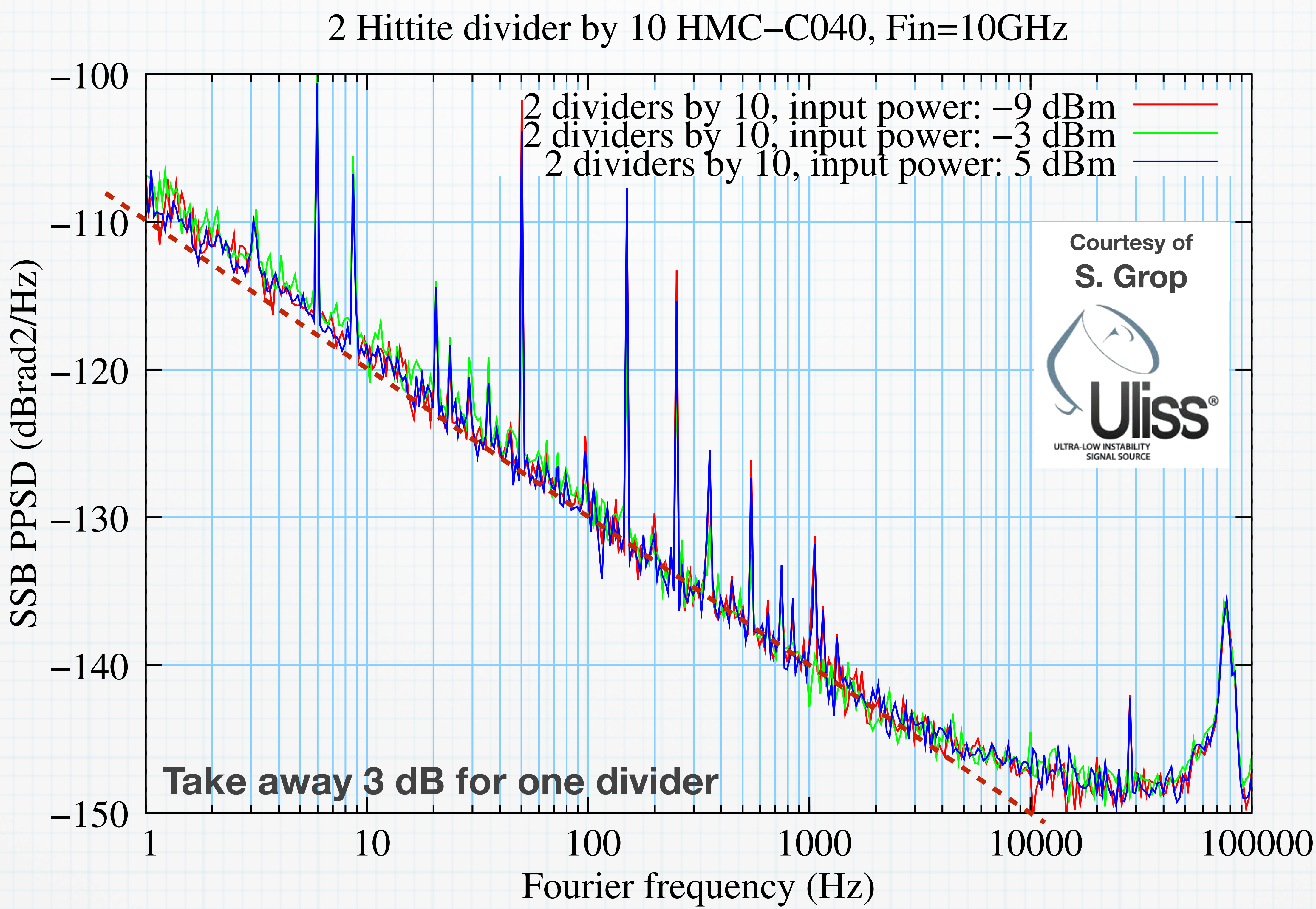
NBSG53A SiGe ÷2 µwave divider

Output vs Output gives info about the output stage



The problem seems in the gear box, rather in the output stage

Hittite HMC-C040, ÷10 divider



Microwave dividers compared

	10 GHz ÷2	5 GHz ÷2	2.5 GHz ÷2	lower	
NB7L32M	–100	–109	–109	–109	600 MHz 1.2 GHz ÷2
NBSG53A	97.5	–103.5		–104	800 MHz 1.6 GHz ÷2
HMC-C040				–113	1 GHz 10 GHz ÷10
HMC705LP4				–121	0.5 GHz 2.5 GHz ÷5

Conclusions

- Two main noise types, x-type and φ-type
  - Observed on a few logic devices and gate arrays
  - Also in microwave dividers
- The 1/Volume law describes $1/f$ (few cases)
- Other effects (chatter, temperature, etc.)
- The choice of devices is independent of this work
  No expressed/implied endorsement on these device

- Funds
  - ANR Oscillator IMP and First-TF
  - Region Franche Comte
  - EMRP Project IND 55 Mclocks

A special thanks to all members of the
Go Digital working group, at FEMTO-ST and INRIM

All slides {are | will be}
on my home page

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