In memoriam of Jacques Groslambert

The sampling theorem in Π and Λ digital dividers

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Outline

- Theoretical introduction
- Π and Λ digital dividers
- Experiments

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Motivations

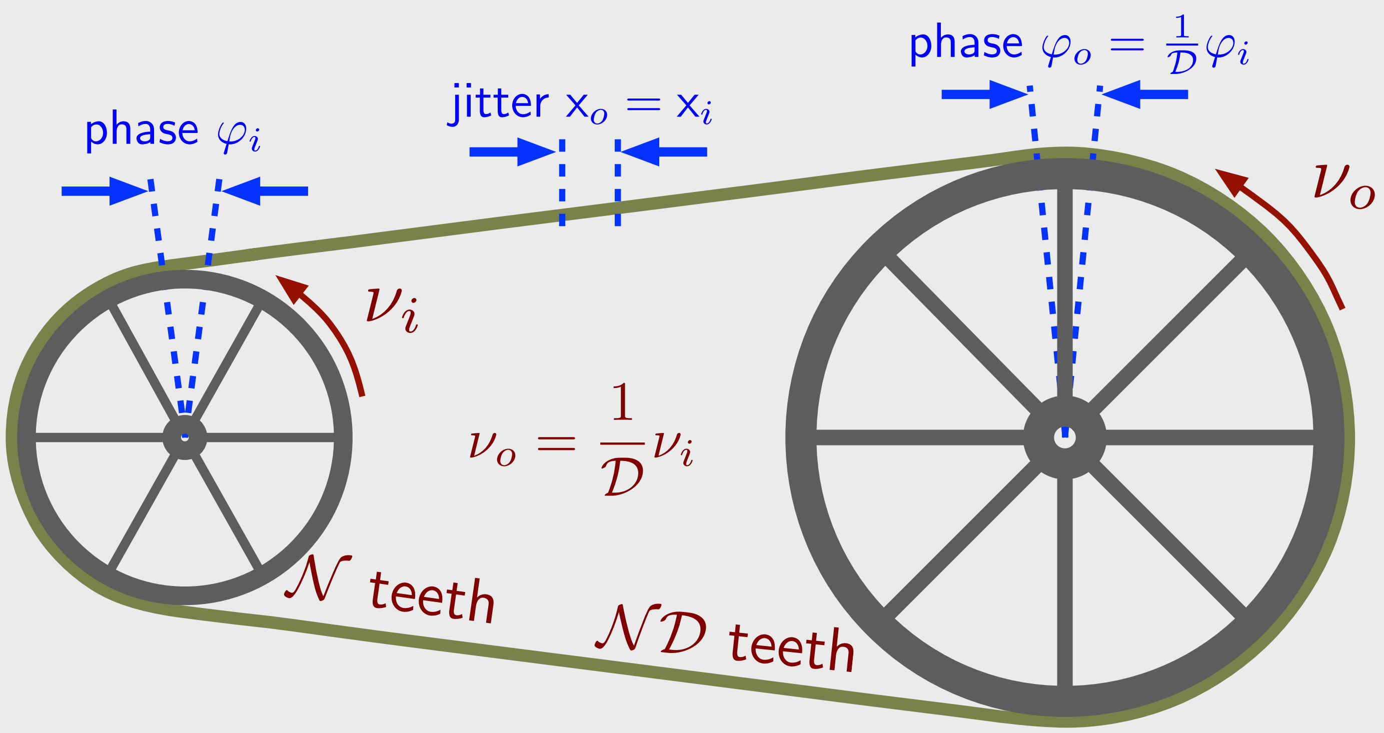
- Seminal article by W. F. Egan (1990)
  - Milestone in the domain, never forget it
  - However, TTL and ECL logic families are now obsolete

- Microwave (photonics) –> highest spectral purity
- Transfer the spectral purity to HF/VHF
  - Dividers are more comfortable than multipliers
    - NIST now uses analog dividers

- Nowadays digital electronics is fantastic
  - CPLD & FPGA –> Easy to duplicate
  - High number of gates for cheap
  - High toggling frequency (1.5 GHz)

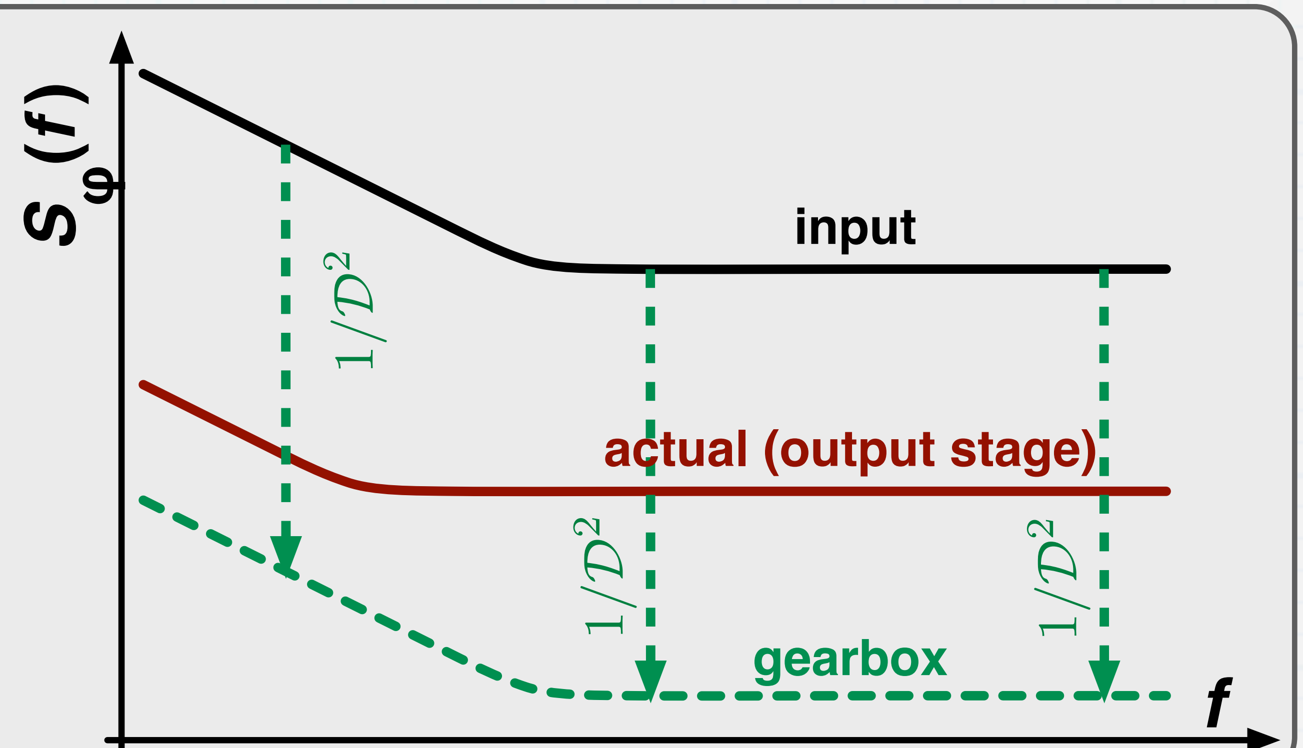
W. F. Egan Egan WF, Modeling phase noise in frequency dividers, IEEE T UFFC 37(4), July 1990
E. Rubiola & al, Phase noise in the regenerative frequency dividers, IEEE T IM 41(3), June 1992
A. Hati & al, Ultra-low-noise regenerative frequency divider…, Proc IEEE IFCS, May 2012

The gearwork model



- **The noise-free divider**
  - **Keeps the input jitter x(*t*) (phase-time fluctuation)**
  - **Scales down**
    - **φ by 1/*D*** [rad]
    - ***S*φ by 1/*D*²** [rad²/Hz]

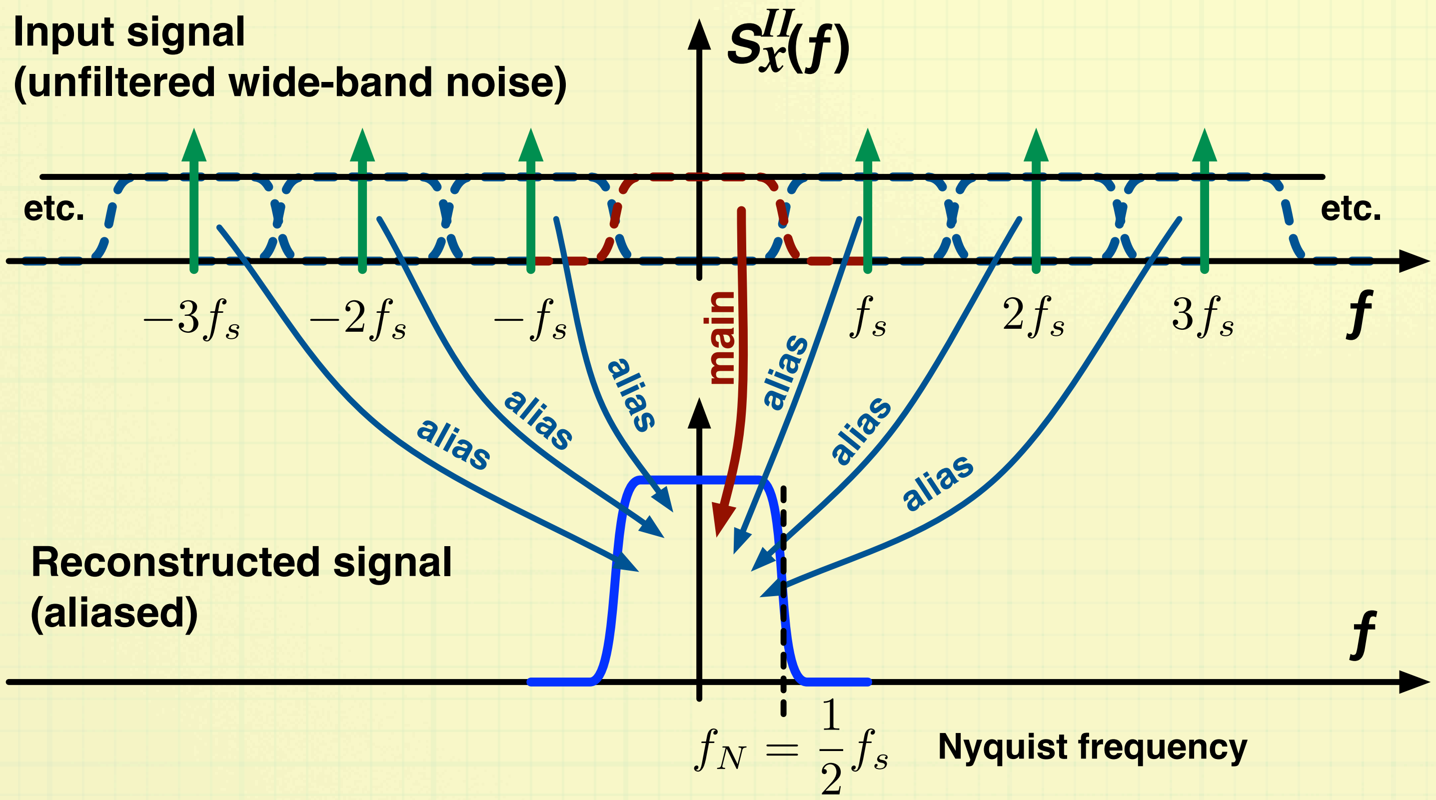
- **In the real divider**
  - **Sφ of the output stage adds up and often dominates**



W. F. Egan Egan WF, Modeling phase noise in frequency dividers, IEEE T UFFC 37(4), July 1990

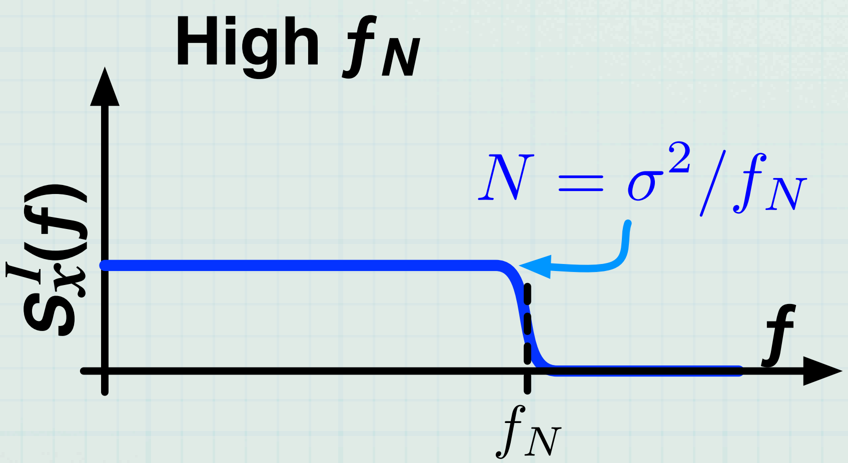
Sampling and aliasing

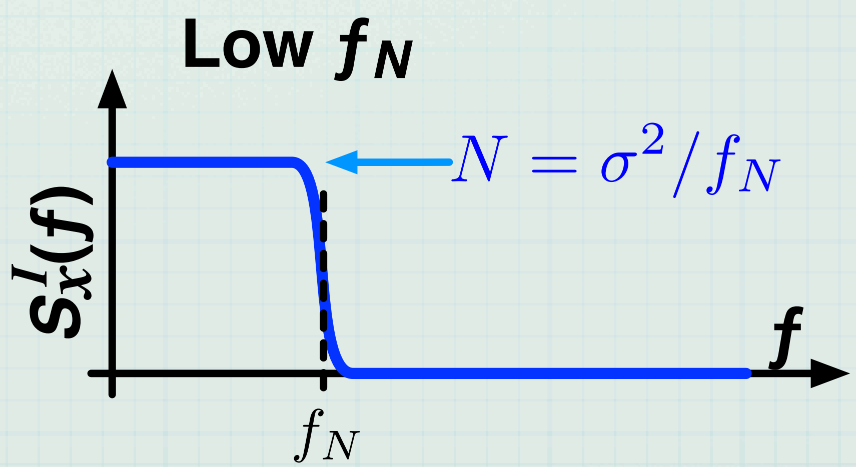
— Energy conservation applies to the unfiltered signal —



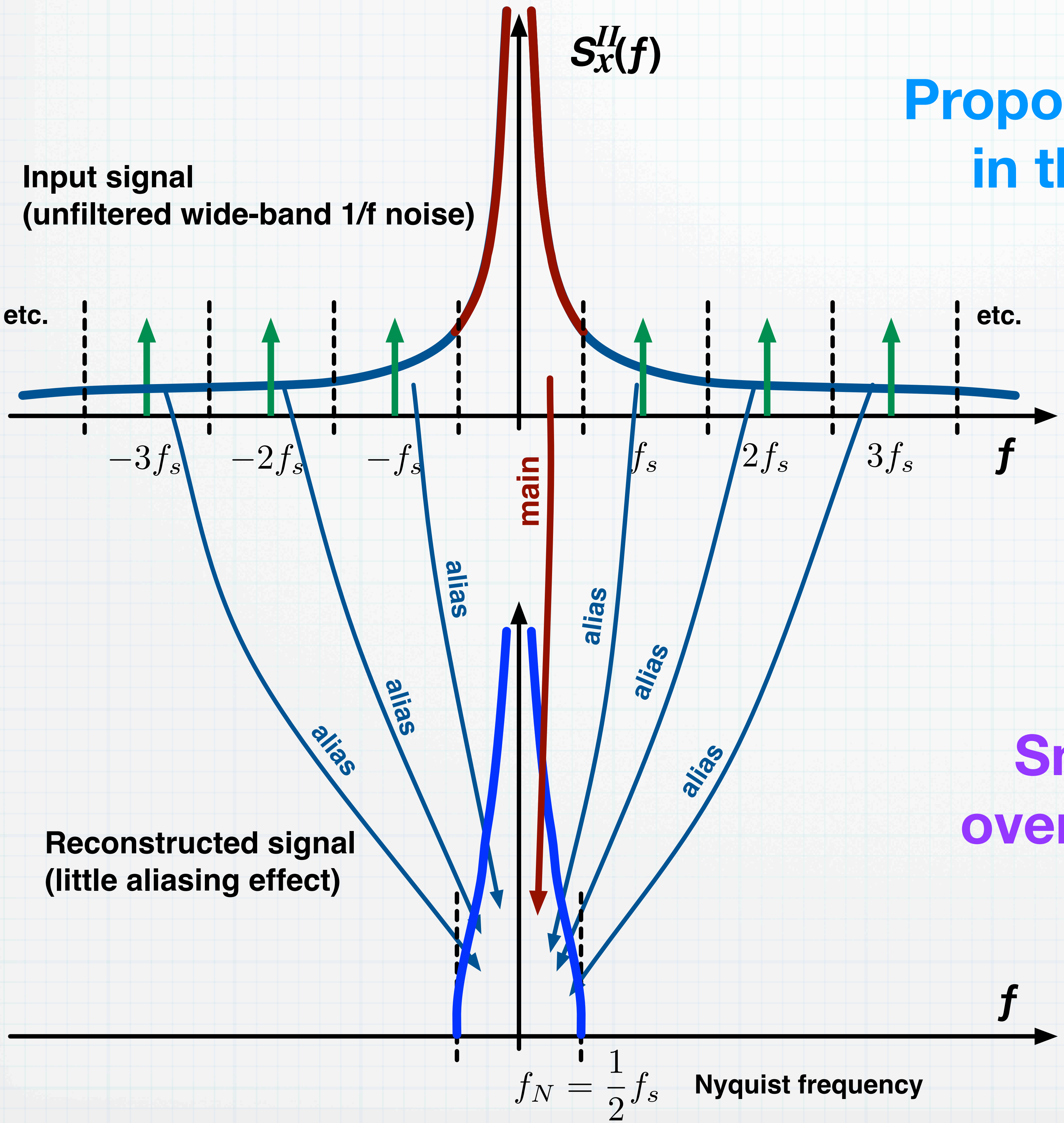
- Multiple aliases overlap to the main part of the spectrum
- With white noise, the PSD increases by B/f_N (Bandwidth / Nyquist f)

Downsampling increases the (PM) noise spectrum





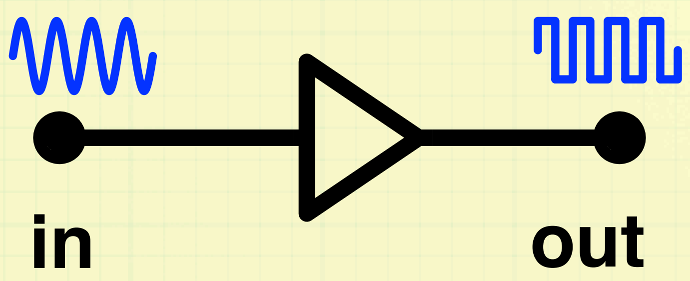
Aliasing and 1/f noise



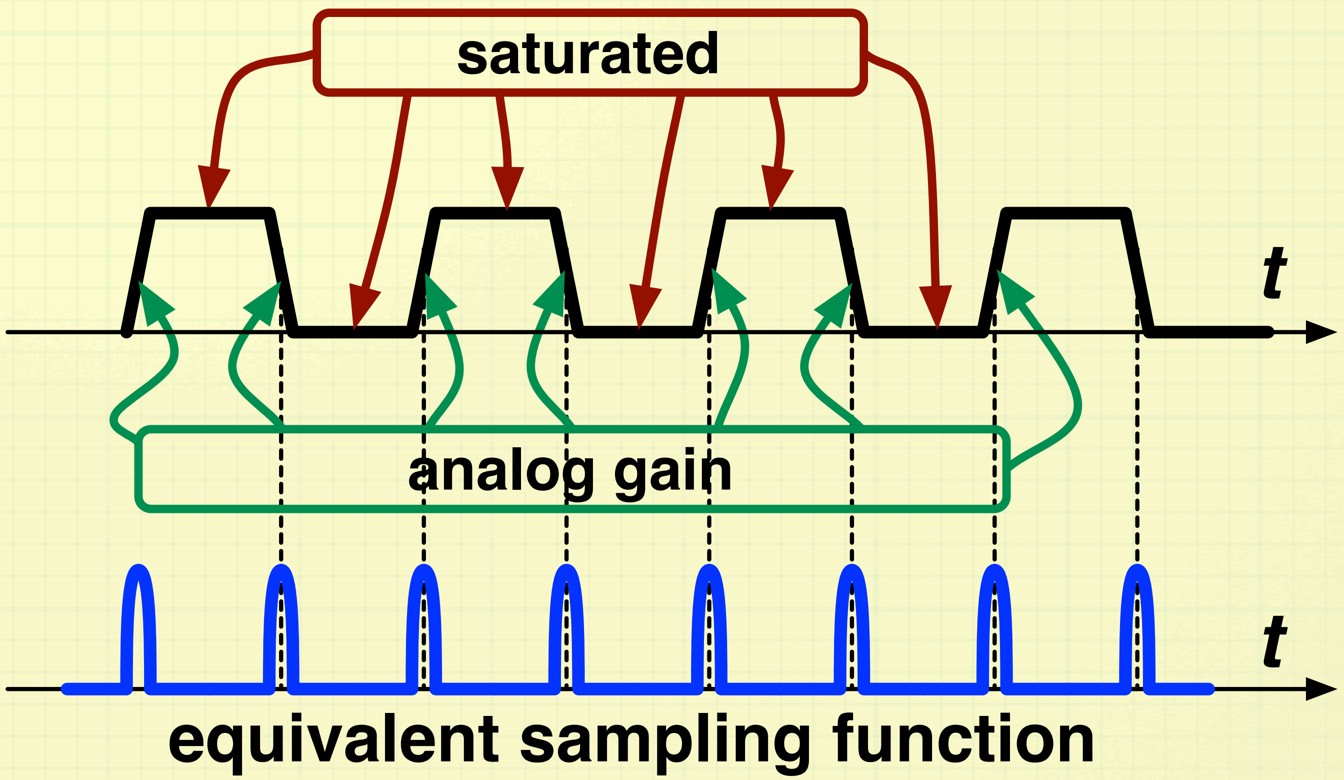
Proportionally lower power in the higher-f aliases

Small effect on the overall noise spectrum

PM-noise aliasing in the input stage



Convert the input sinusoid into a square wave, as appropriate



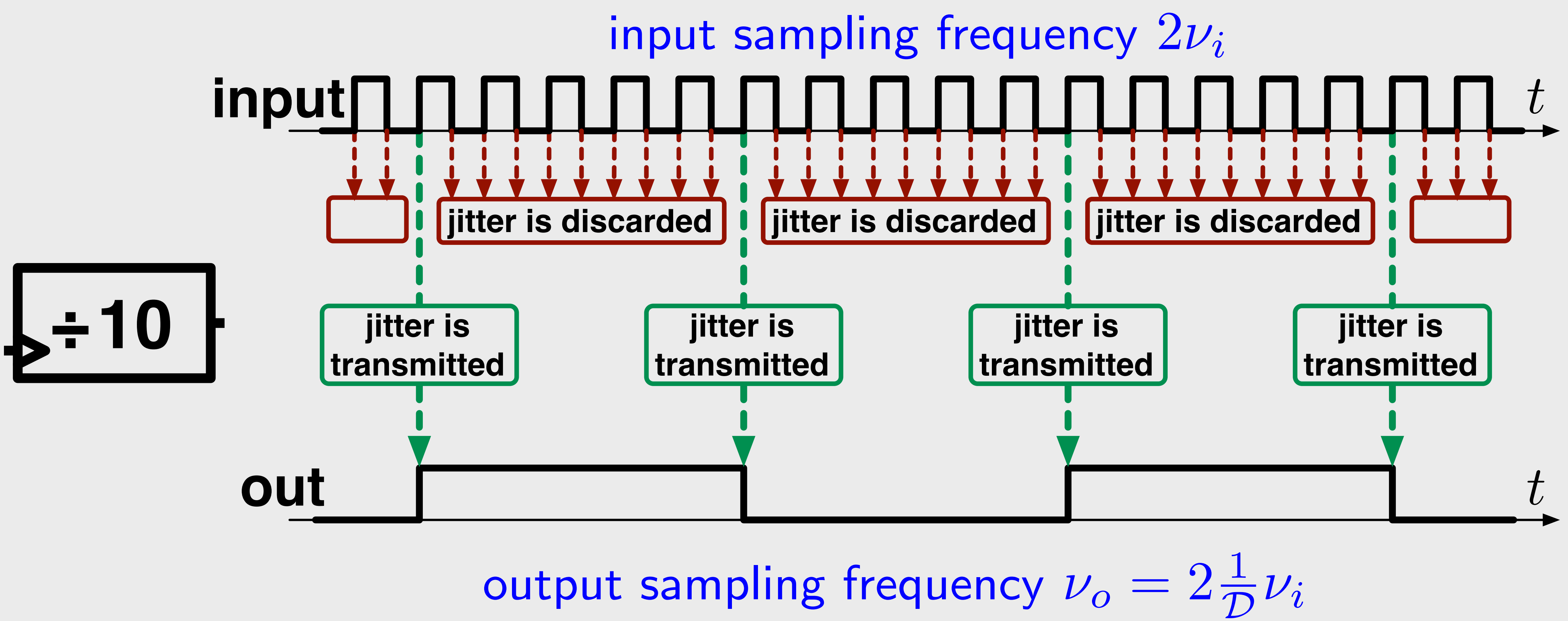
- Edge-sampling at $2\nu_i$ inherent in the sin-to-square conversion
- Full-bandwidth (B) noise is taken in
- The phase-noise Nyquist frequency is ν_i
- The sampling process increases the noise by B/ν_i

Eventually, clipping removes the AM noise [Pfaff 1974]

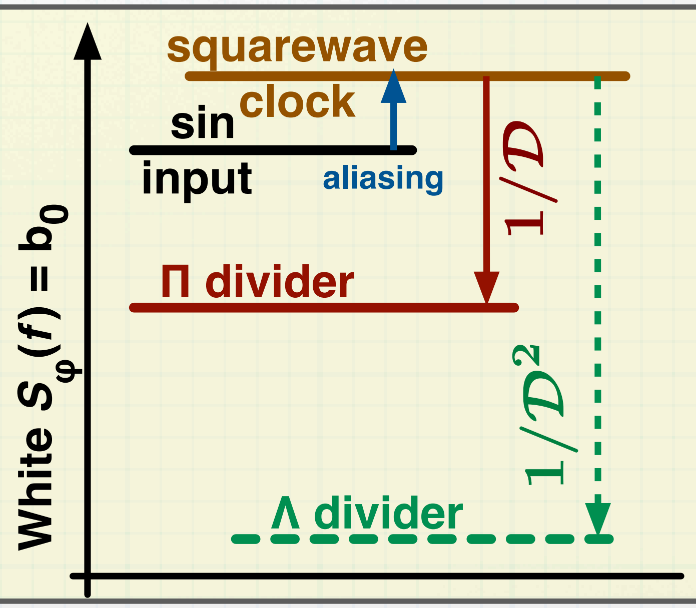
Aliasing in Π divider

Regular synchronous divider

The Greek letter Π recalls the square wave ΠΠΠΠ



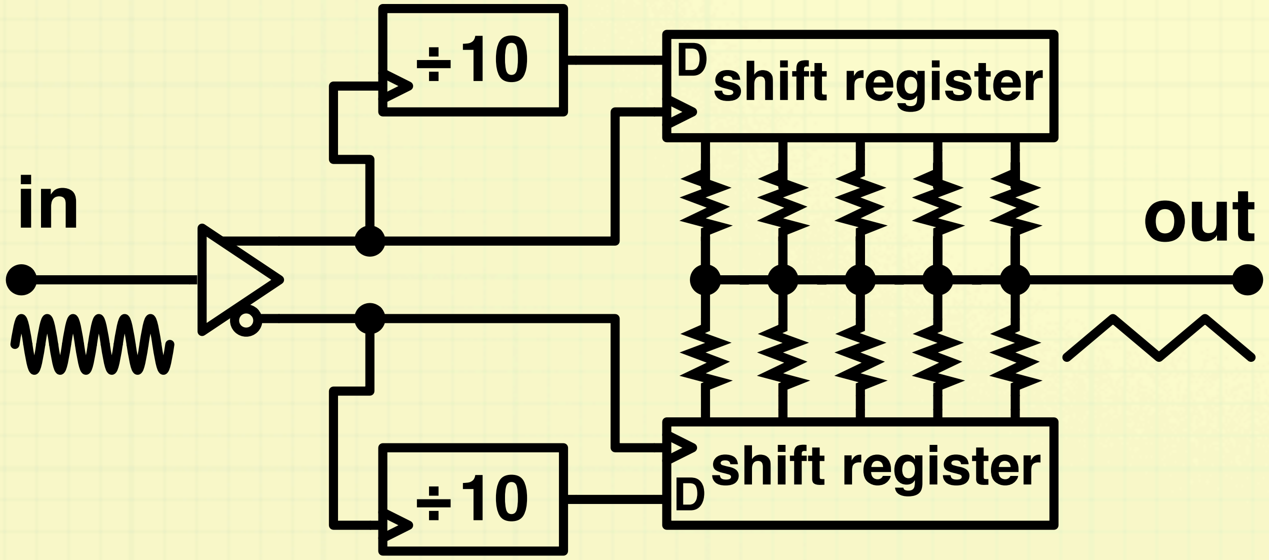
- **The gearbox scales Sφ down by 1/D^2**
- **The divider takes 1 edge out of *D***
  - **Raw decimation without low-pass filter**
  - **Aliasing increases Sφ by *D***
- **Overall, Sφ scales down by 1/*D***



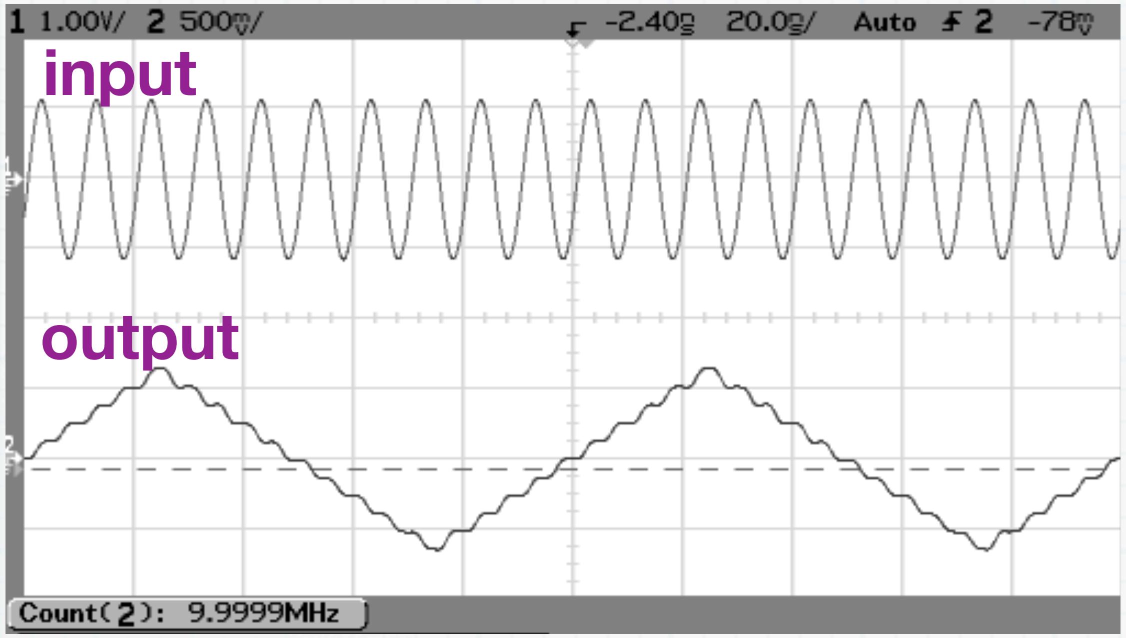
The Λ divider – Little/no aliasing

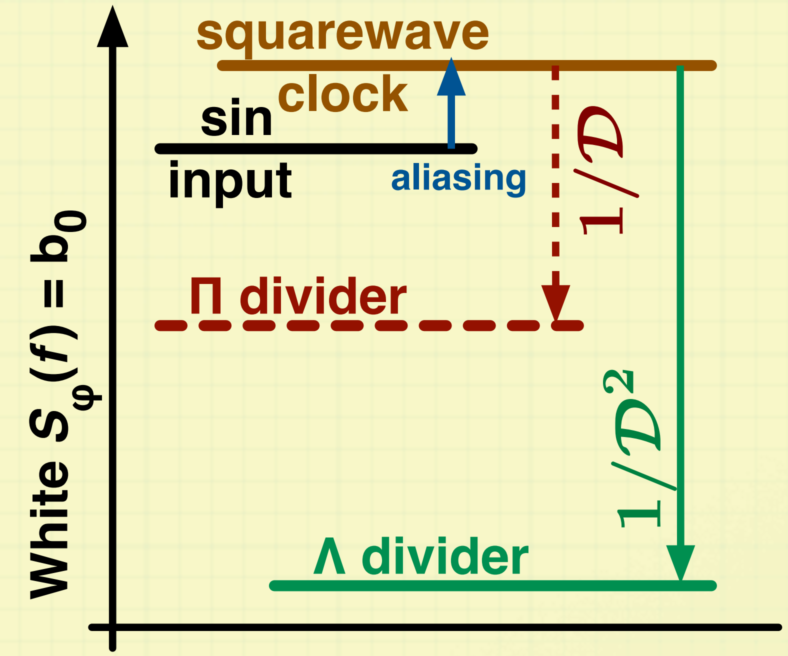
New divider architecture

Series of Greek letters ΛΛΛΛΛ recalls the triangular wave



- Gearbox and aliasing –> 1/*D* law
- Add *D* independent realizations shifted by 1/2 input clock,
- reduce the phase noise by 1/*D*,
- … and get back the $1/D^2$ law





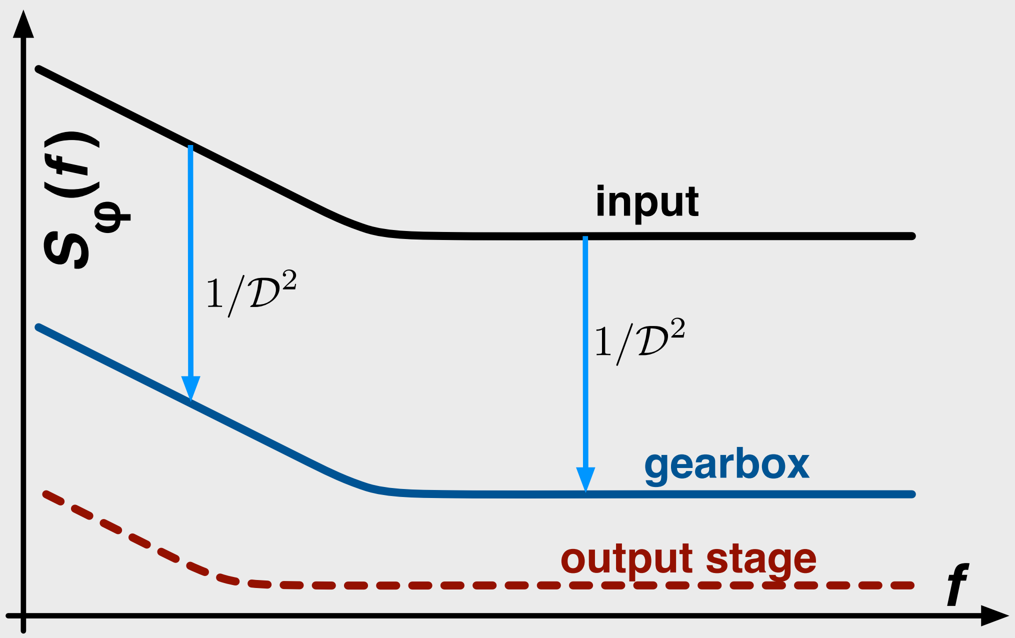
The names Π and Λ derive from the shape of the weight functions in our article on frequency counters

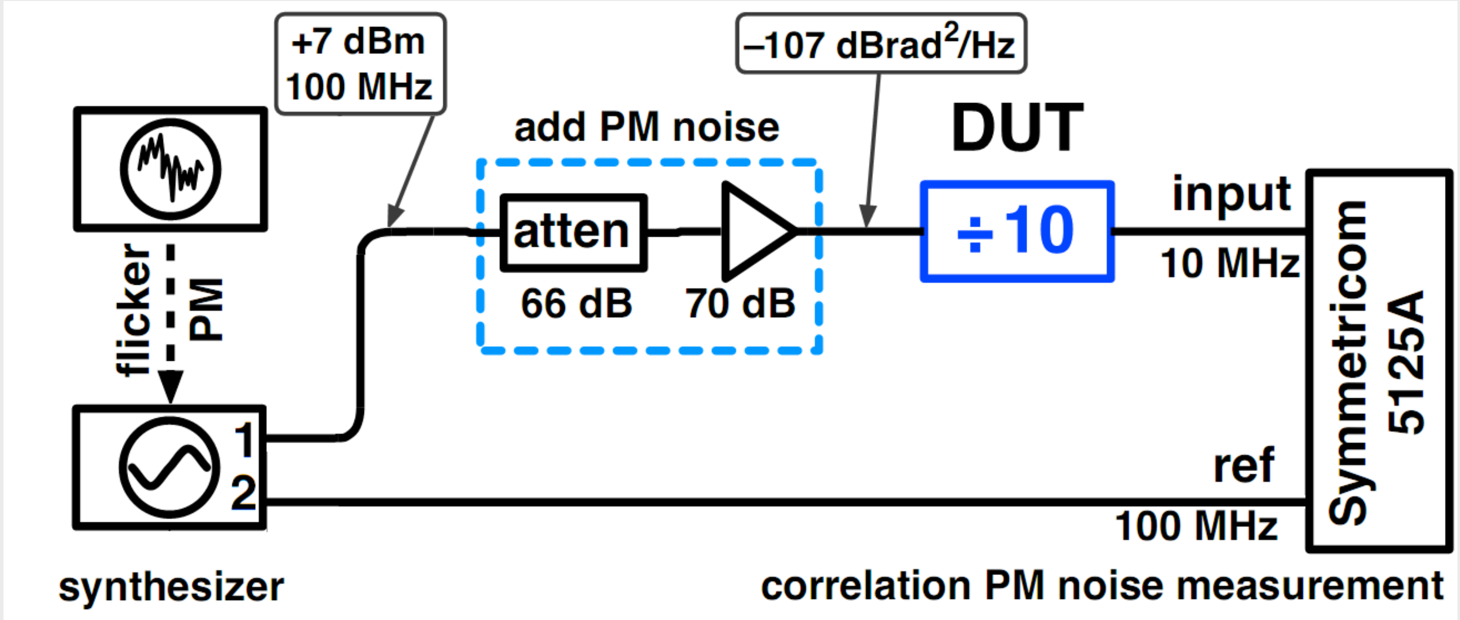
E. Rubiola, On the measurement of frequency … with high-resolution counters, RSI 76 054703, 2005

Experimental method

Large input PM noise is used to emphasize the effect of aliasing

- Intentionally high PM noise at the input
- The scaled-down input noise is higher than the output-stage noise





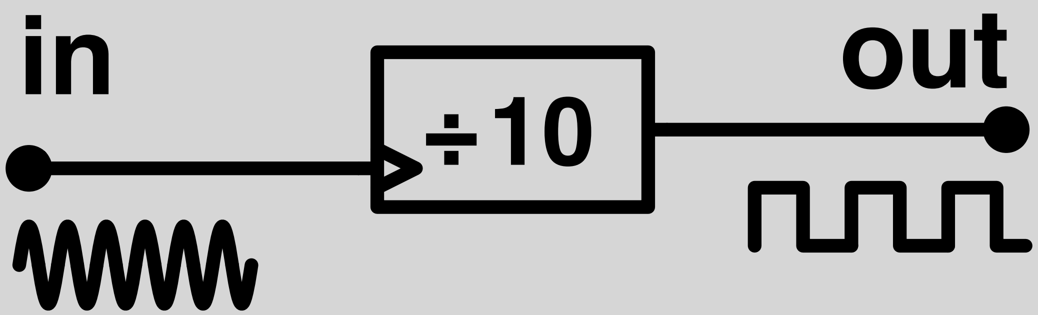
- Large attenuation/ampli –> noise
- Digital instruments for phase-noise measurement can handle

  $f_{\text{input}} \neq f_{\text{reference}}$

- Correlation reduces the background

Dividers under test

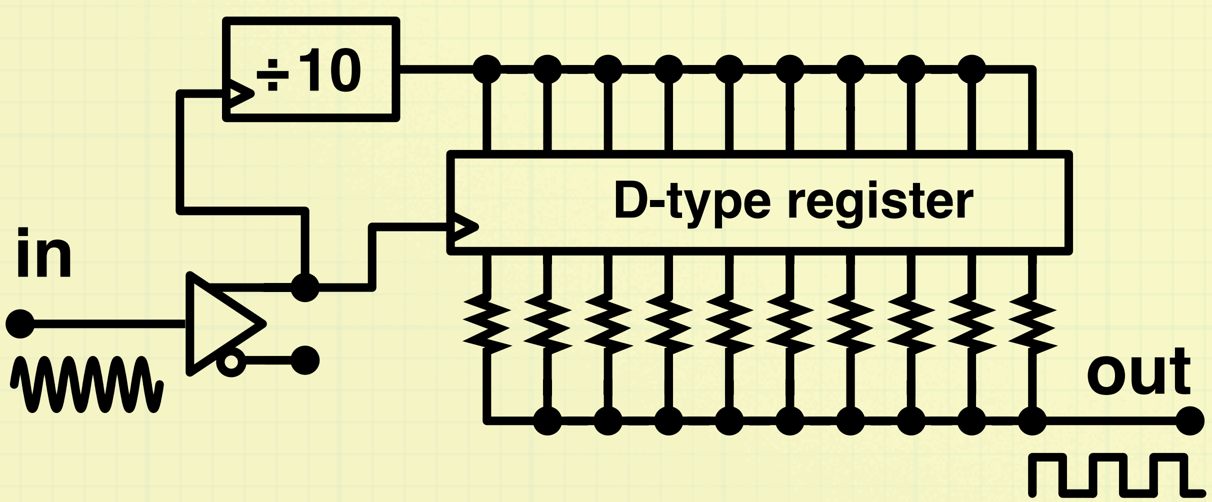
EPM3064A CPLD (Altera MAX 3000 Series, 64 macro-cells, speed grade 7 ns)



Π divider

– the one everybody knows –

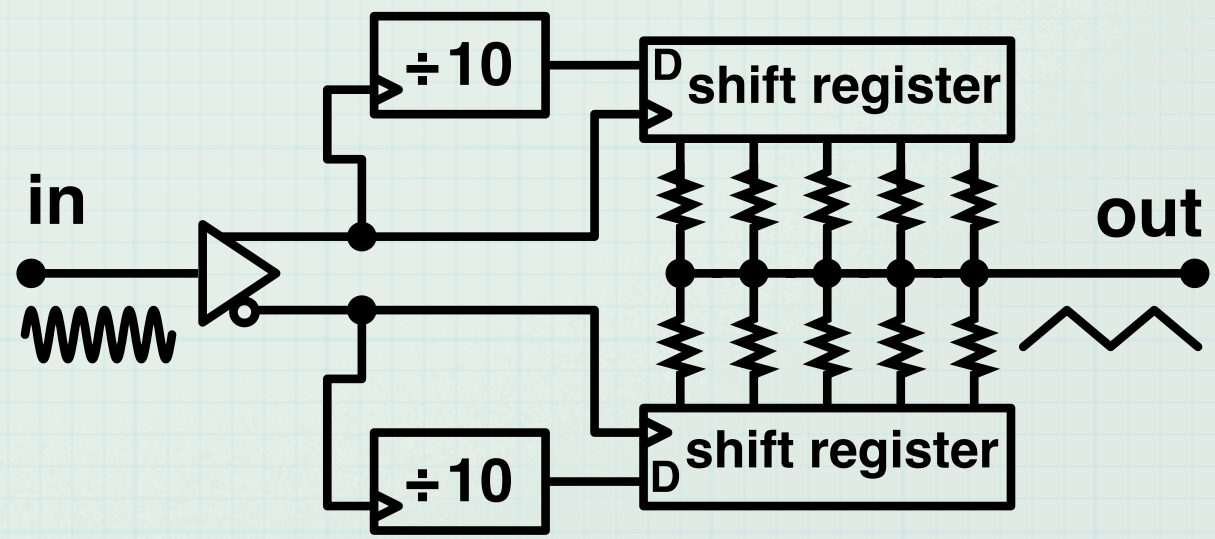
Multi-buffer Π divider



The outputs are arguably independent

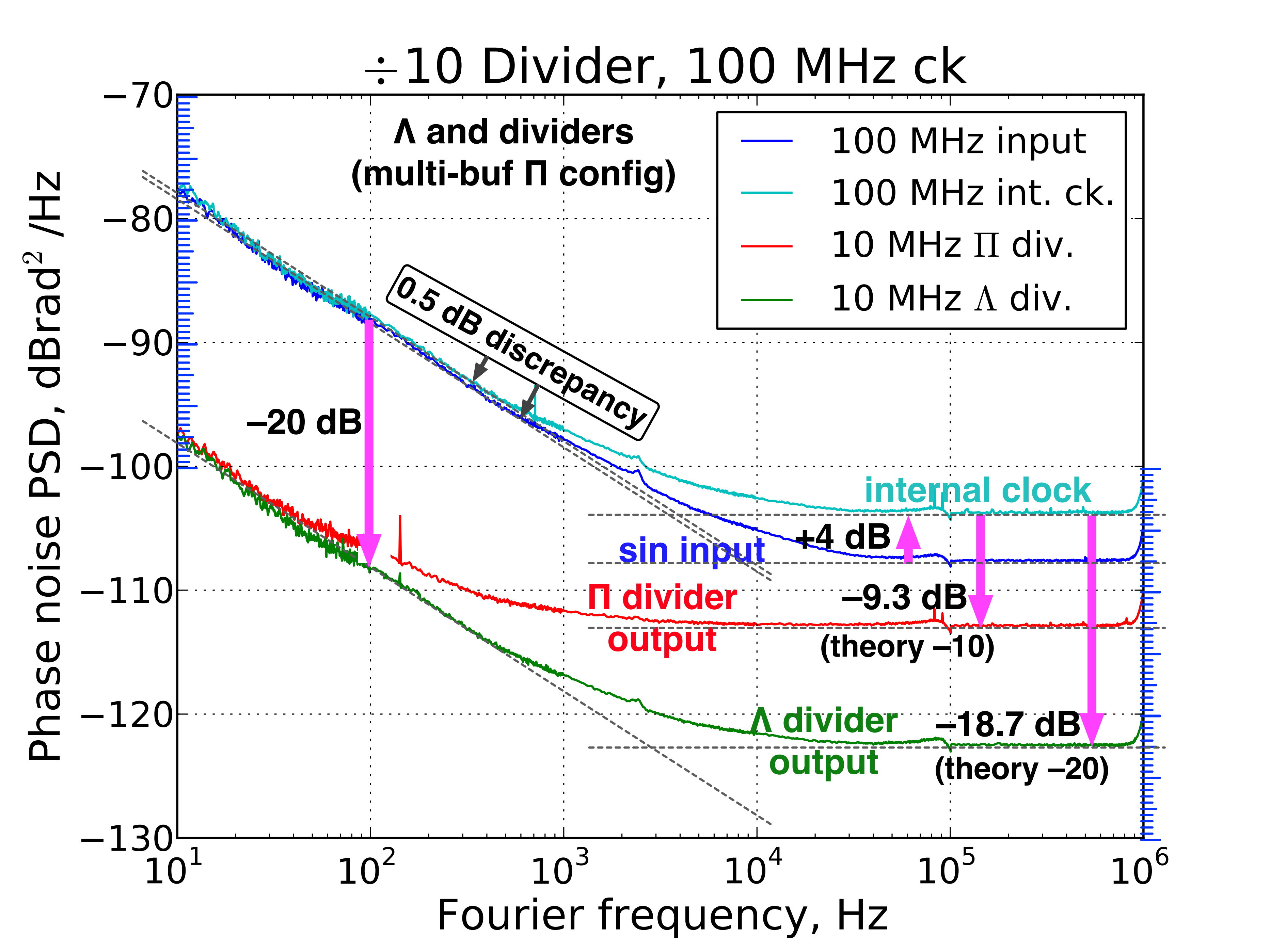
Try to reduce the output-stage noise

Λ divider



White noise:
The clock edges are independent
Correct for aliasing

Results – Test on aliasing

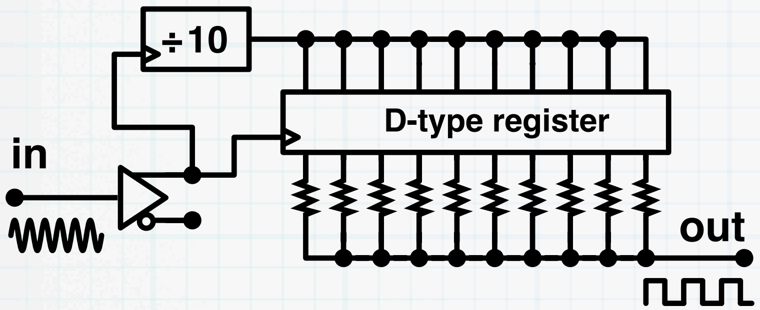


- **Flicker region**
  - **Negligible aliasing**
  - **$1/D^2$ law (–20 dB)**

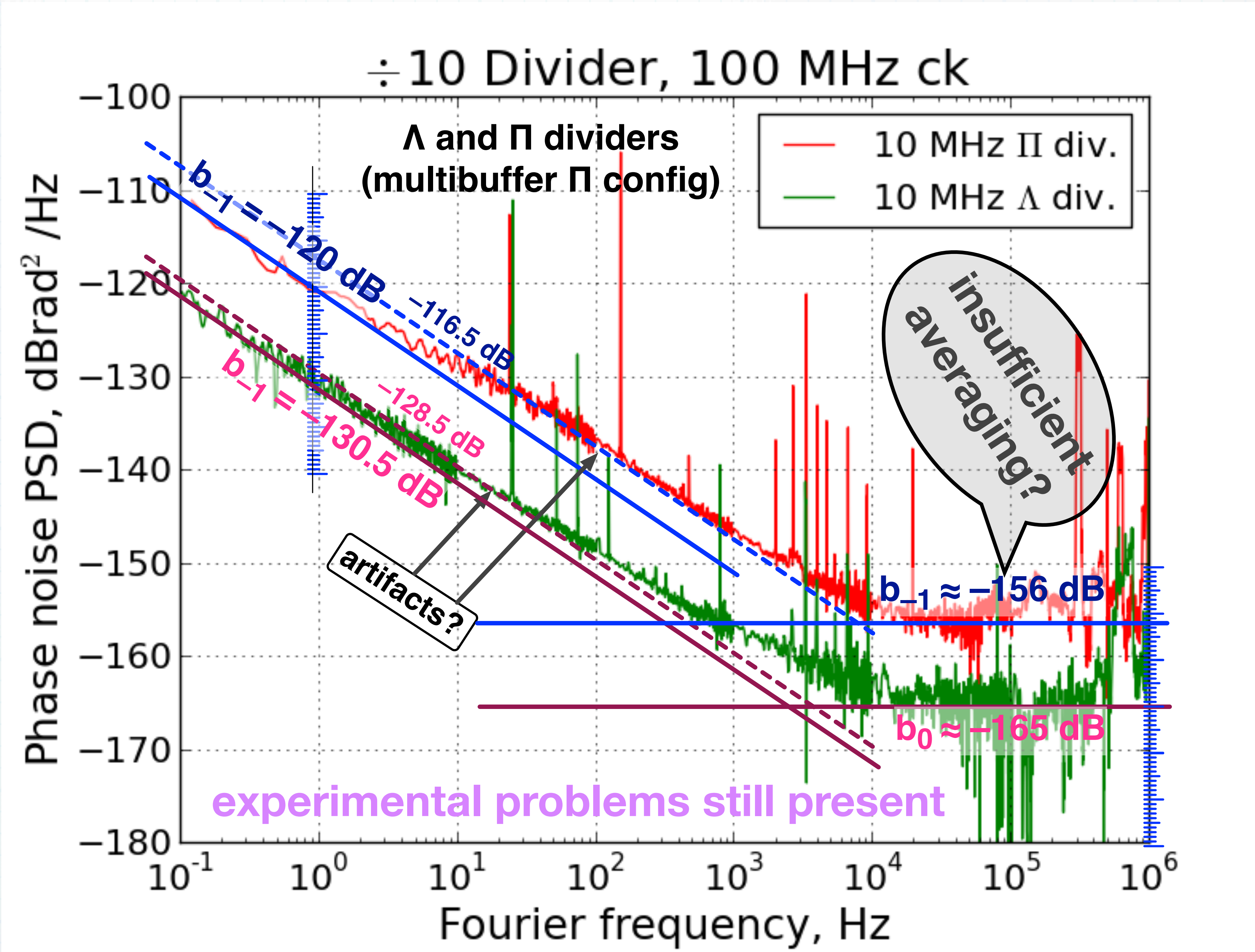
- **White region**
- **Aliasing in the front-end –> +4 dB**
- **$1/D$ law and $1/D^2$ law**

Phase noise of real dividers

Multibuffer Π divider

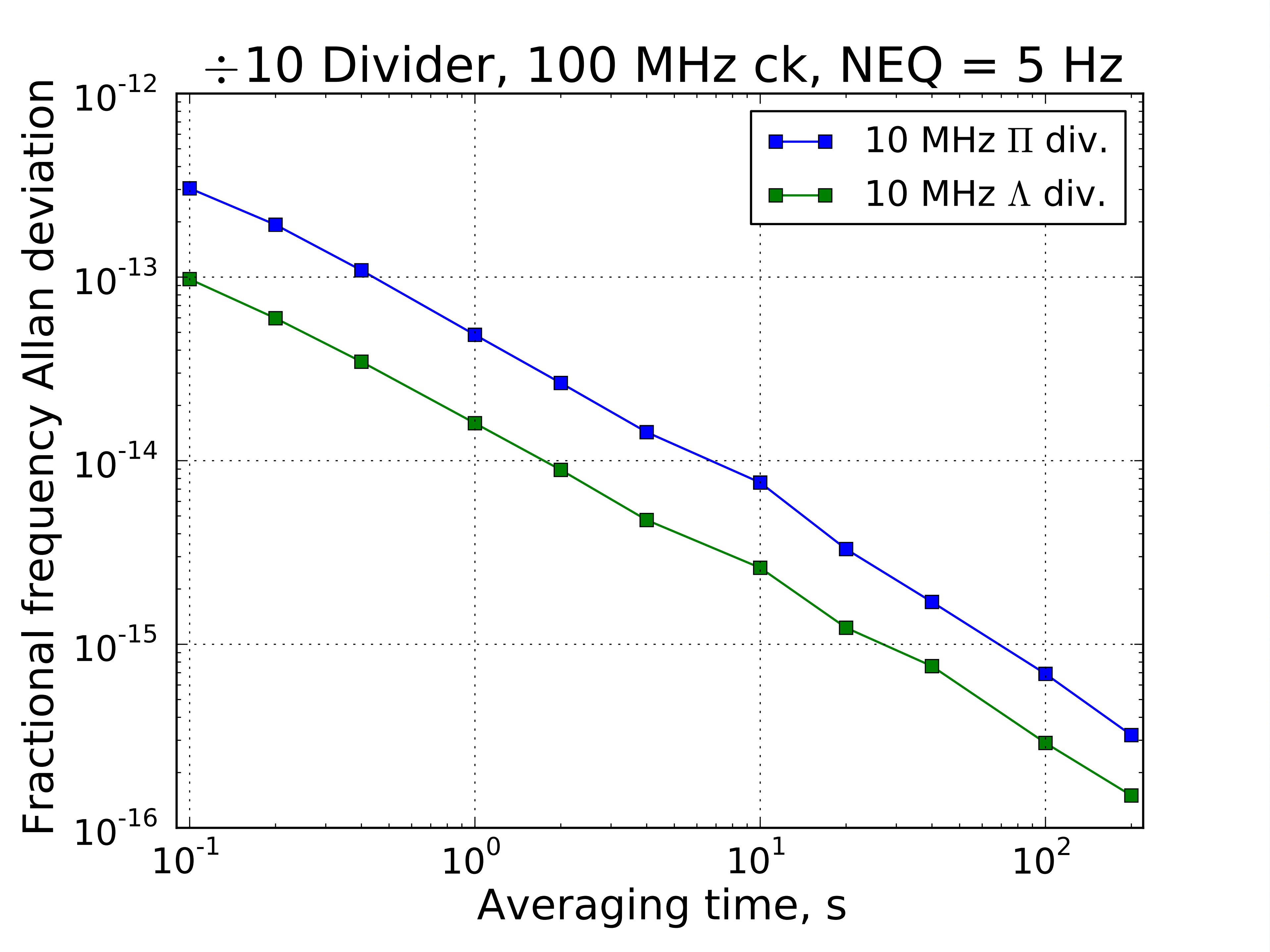


multiple outputs are expected to reduce the output-stage noise
– not happened, why? –



- Flicker region –> Negligible aliasing
- The multibuffer Π divider is still not well explained
- The Λ divider exhibits low $1/f$ and low white noise

Allan deviation of real dividers



- **Slope 1/τ, typical of white and flicker PM noise**
- **The Λ divider performs $2{\times}10^{-14}$ at $\tau = 1$ s, 10 MHz output**

The bottom line

- Aliasing in traditional dividers
  - Increases white noise
  - Has little effect on flicker
- Flicker in multi-buffer Π divider not understood yet
- The new Λ divider
  - Is little/no affected by aliasing
  - Exhibits the lowest PM noise
    flicker: $b_{-1} \approx -130$ dB
    white: $b_0 \approx -165$ dB
  - Features 2×10^{-14} at $\tau = 1$ s, 10 MHz output

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Thanks – J. Groslambert, V. Giordano, M. Siccardi, J.-M. Friedt
Grants from ANR (Oscillator IMP and First-TF network), and Region Franche Comte