Phase noise in DDS

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Outline

- A short introduction
- Theory
- Experiments

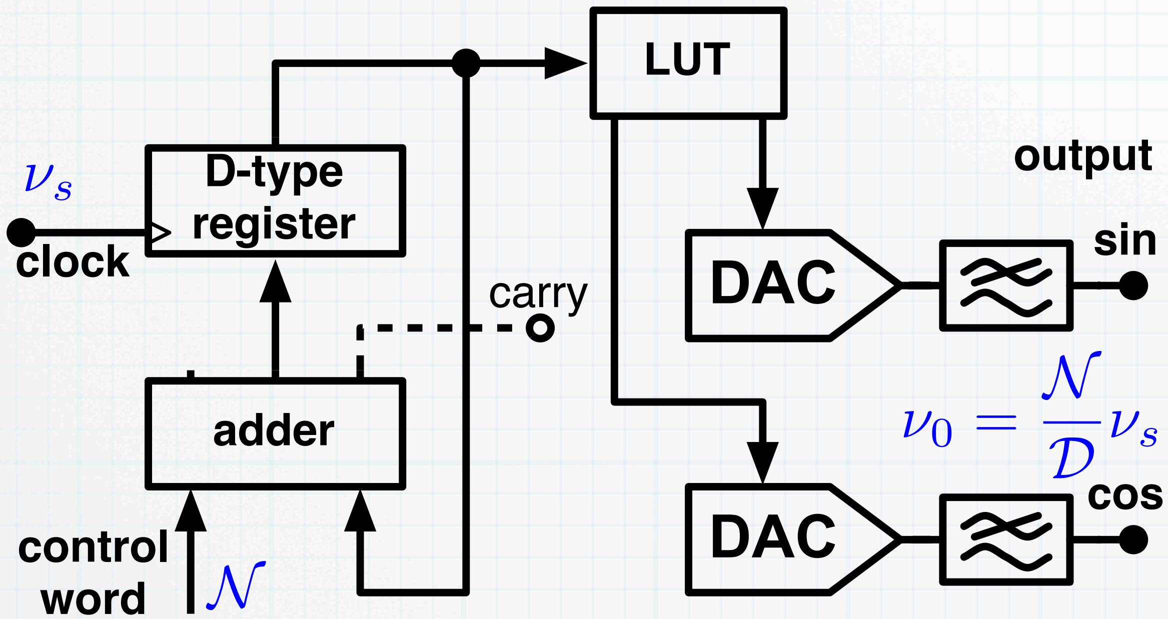
home page http://rubiola.org

Basic DDS scheme

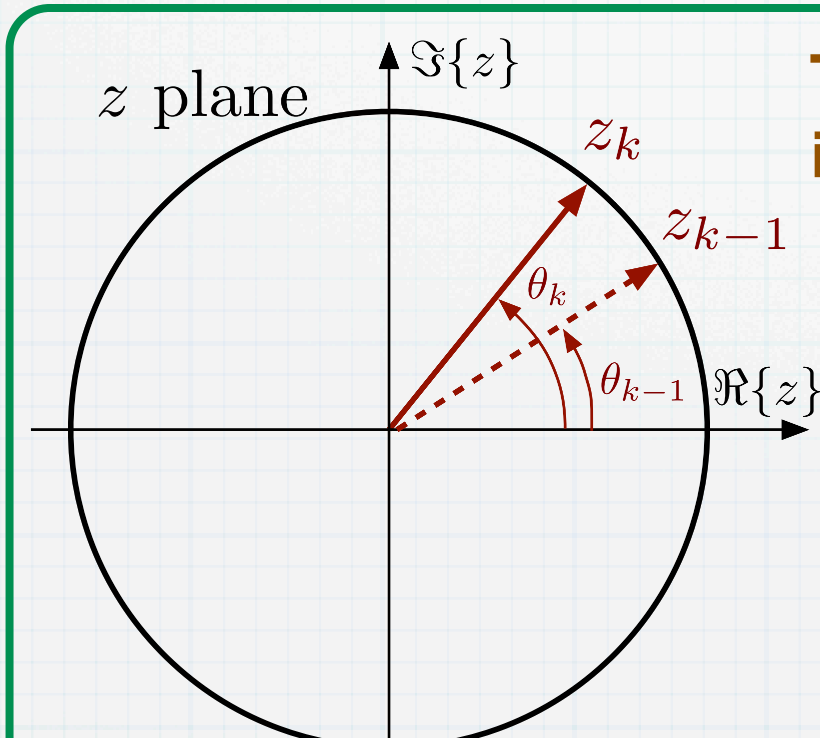
integer: $n_k = (n_{k-1} + \mathcal{N}) \bmod \mathcal{D}$

complex: $z_k = z_{k-1} \exp(j\eta)$

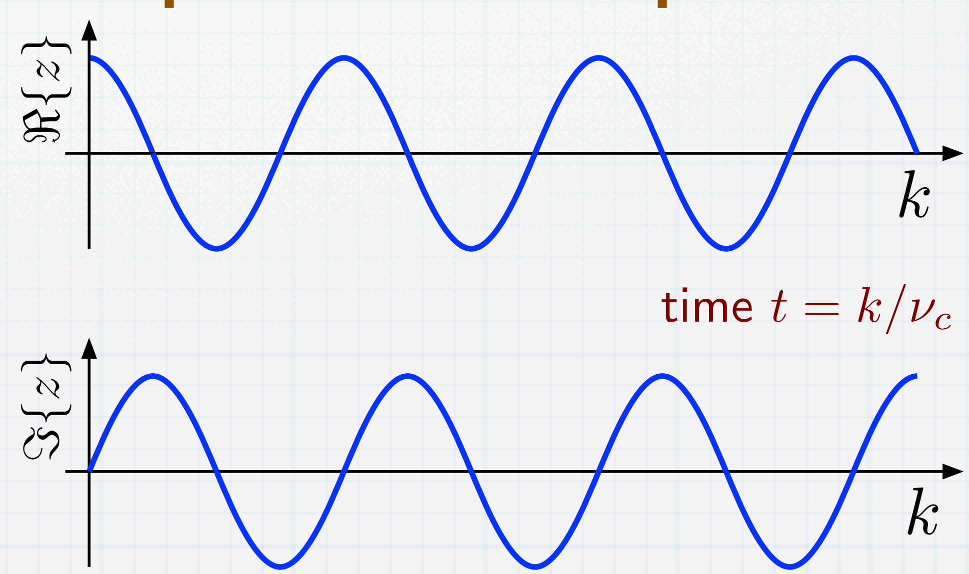
phase: $\theta_k = (\theta_{k-1} + \eta) \bmod 2\pi$



quantity	digital	analog
state variable	n	$\theta = 2\pi\frac{n}{\mathcal{D}}$
assoc. complex		$z = e^{j\theta}$
modulo	$\mathcal{D} = 2^m$	2π
increment	$\mathcal{N}$	$\eta = 2\pi\frac{\mathcal{N}}{\mathcal{D}}$
time	k, $0, 1, 2, \ldots$	$t = k/\nu_s$
clock freq. ν_s	output freq. $\nu_0 = \frac{\mathcal{N}}{\mathcal{D}}\nu_s$	

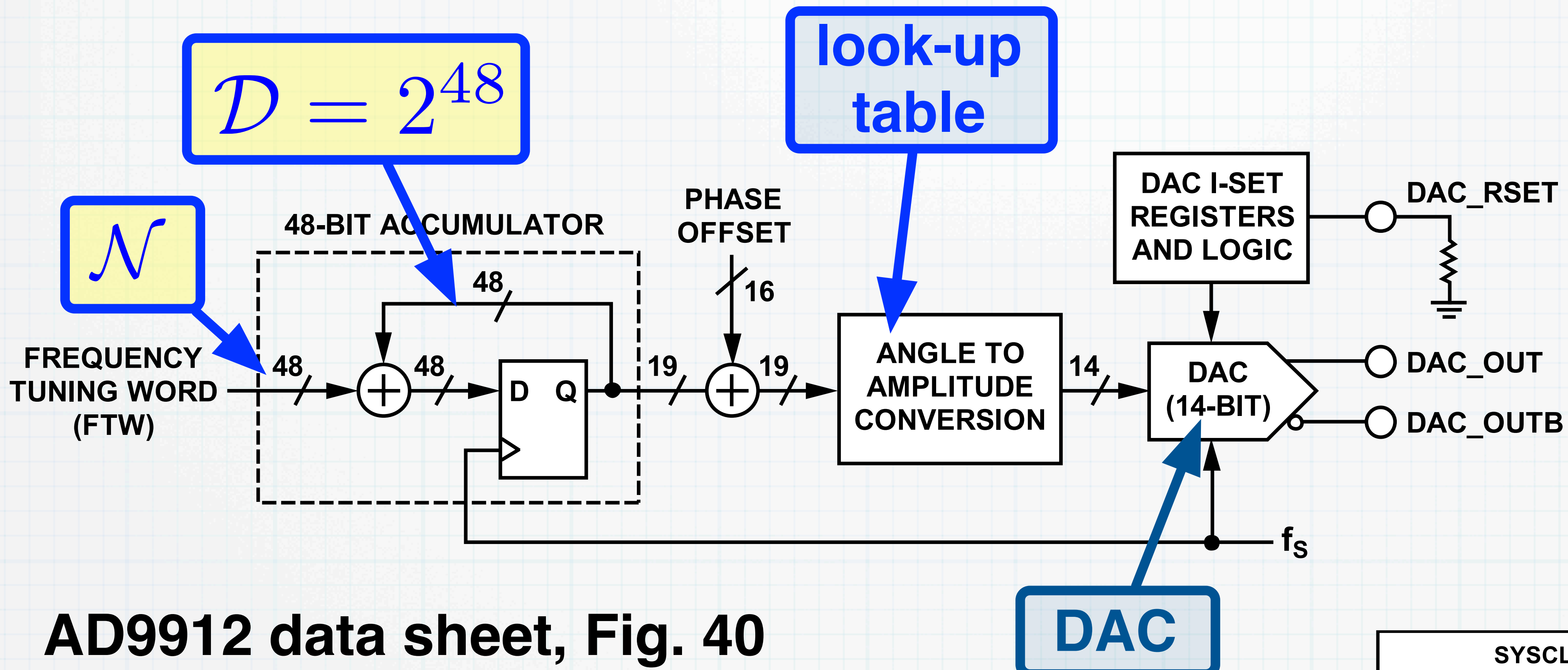


The contents *n* of the *m*-bit register is interpreted as a complex number

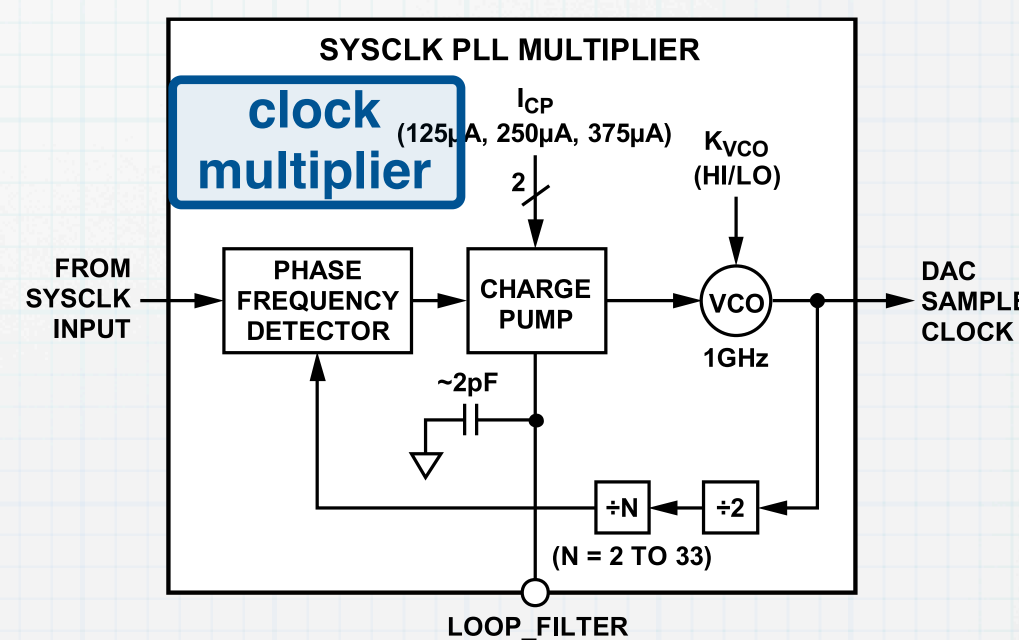


AD9912, a popular fast DDS

48 bit accumulator, 14 bit DAC, 1 GHz clock



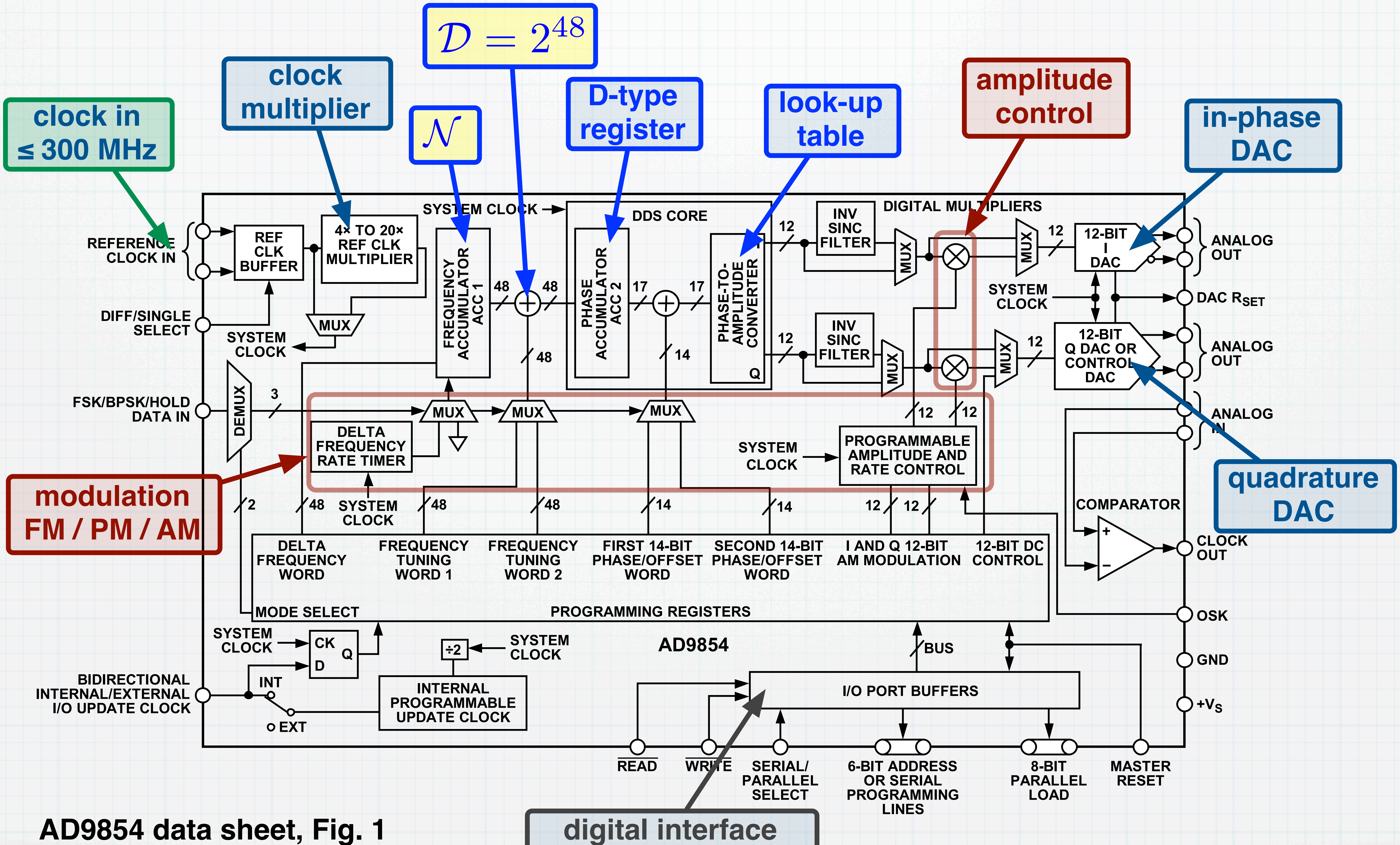
AD9912 data sheet, Fig. 40



AD9912 data sheet, Fig. 45

AD9854, a popular DDS

48 bit accumulator, 300 MHz clock, 12 bit DAC, I-Q output, AM/PM/FM capability

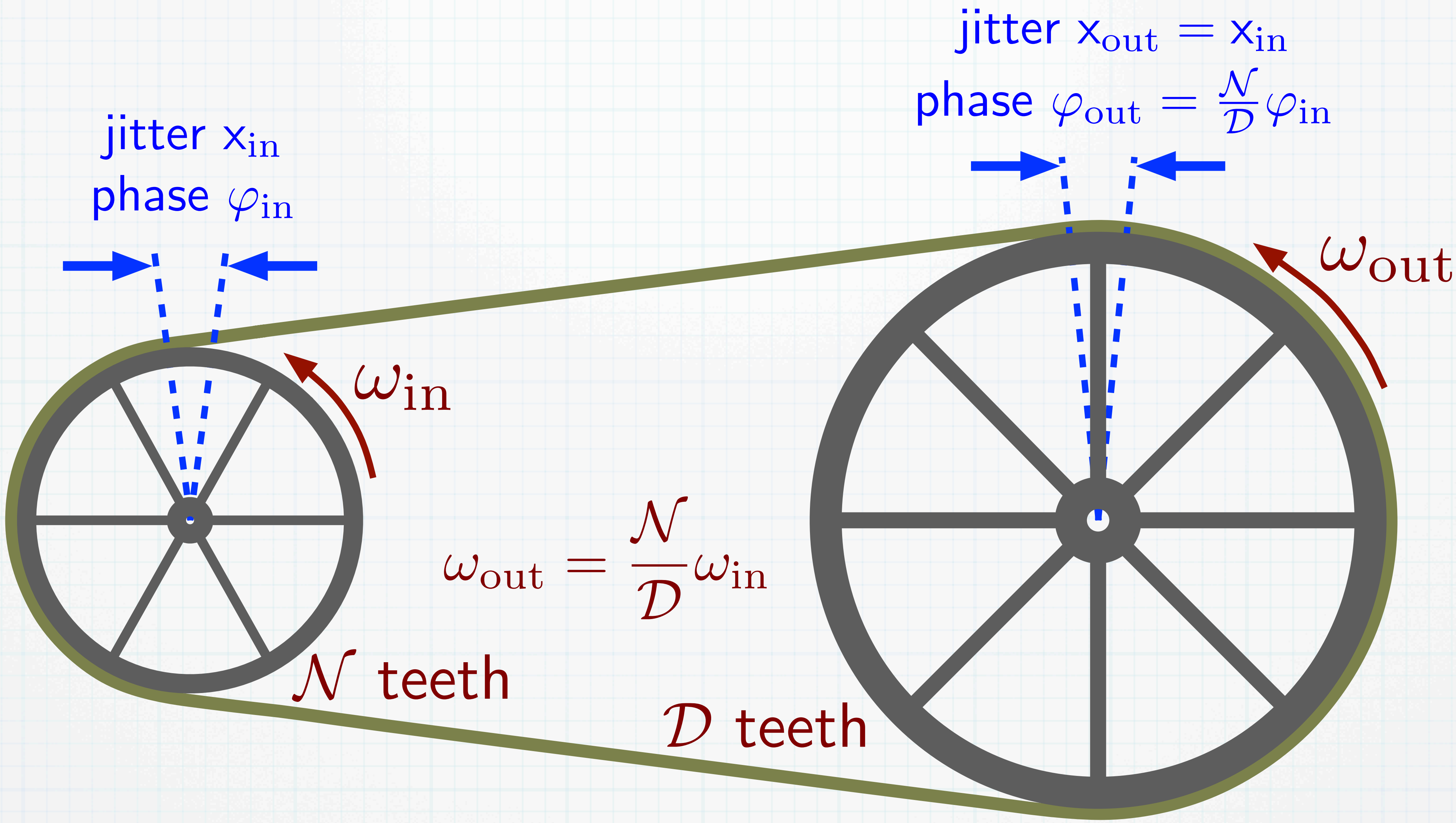


AD9854 data sheet, Fig. 1

Theory

- Simple gearbox model
- Quantization noise
- Sampling theorem
- Spurs
- [PLL clock multiplier]

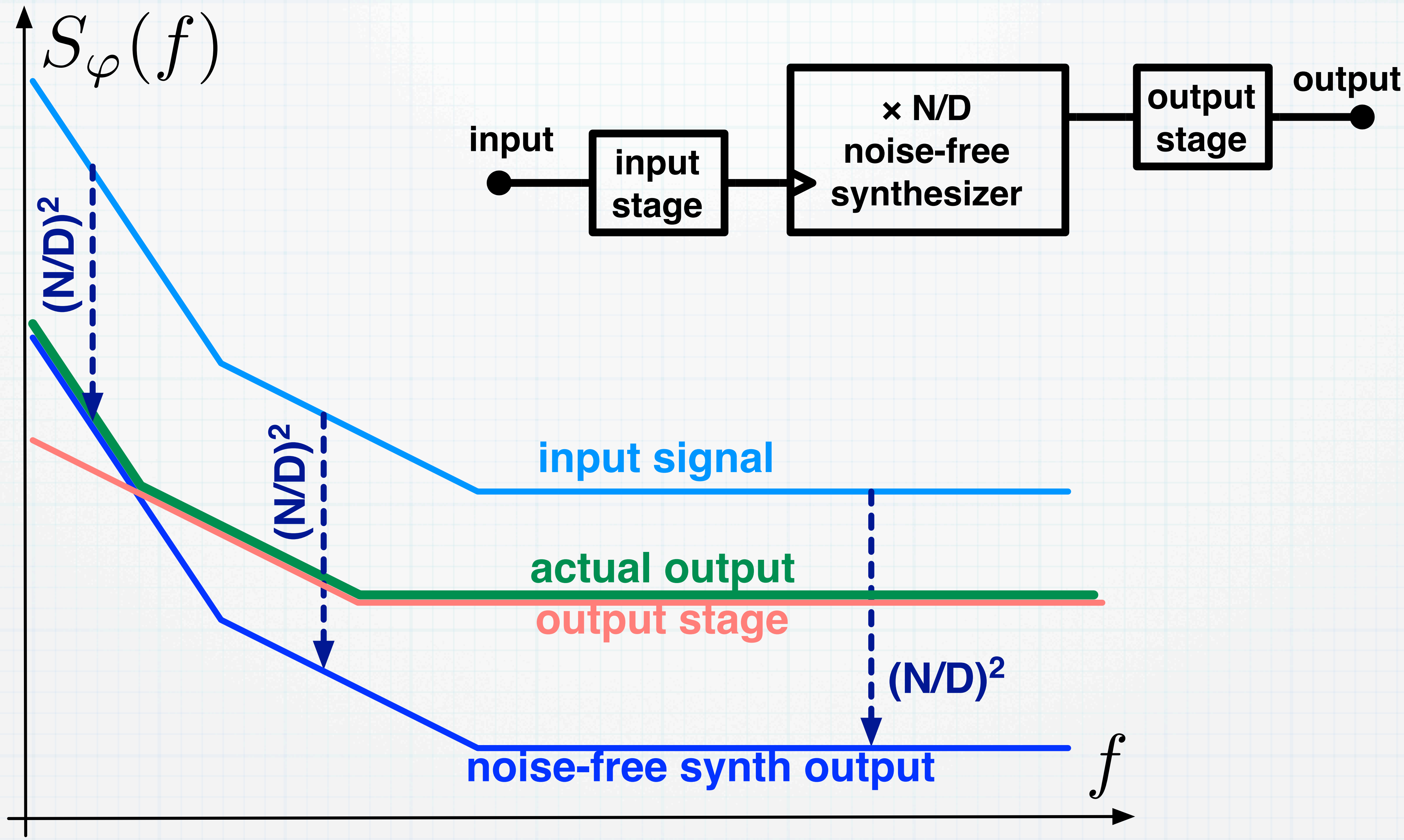
The noise-free synthesizer



- **The noise-free synthesizer propagates the jitter x (phase time)**
  - **So, it scales the phase φ as *N/D*,**
  - **and the phase spectrum S_φ as $(N/D)^2$**
- **Notice the absence of sampling**

The Egan model

for phase noise in frequency dividers

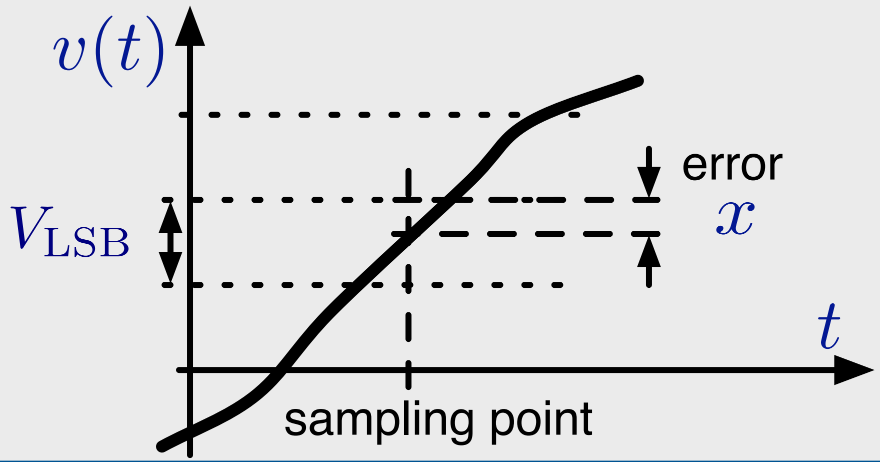


For N/D <<1, the scaled-down noise hits the output-stage limit

W.F. Egan, Modeling phase noise in frequency dividers, TUFFC 37(4), July 1990

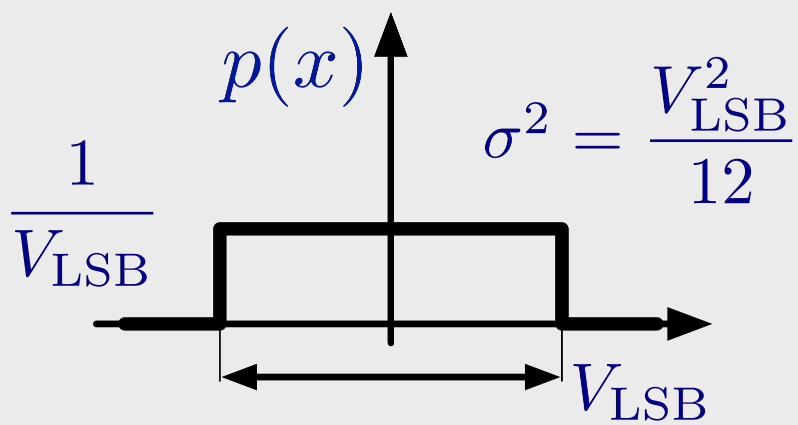
Quantization noise

W. R. Bennett, Spectra of quantized signals, Bell System Tech J. 27(4), July 1948



Analog-to-digital conversion introduces a **quantization error** x $[-V_{LSB}/2 \leq x \leq +V_{LSB}/2]$

n-bit conversion: $V_{\rm LSB} = \dfrac{V_{\rm FSR}}{2^n}$



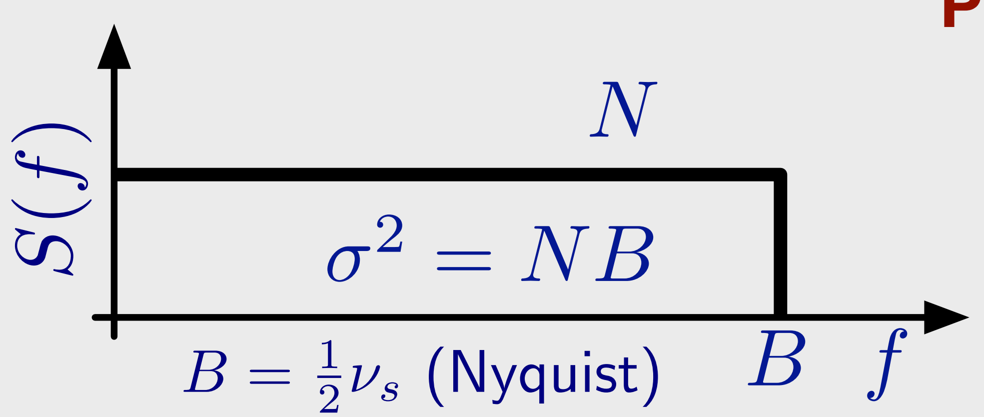
Wiener–Khintchine theorem: **in ergodic systems, interchange time / ensemble**

The noise can be calculated with statistics

$$\sigma^2 = \frac{V_{\rm FSR}^2}{12 \times 2^{2n}} \qquad \mathrm{V}^2$$

1/12 –> –10.8 dB

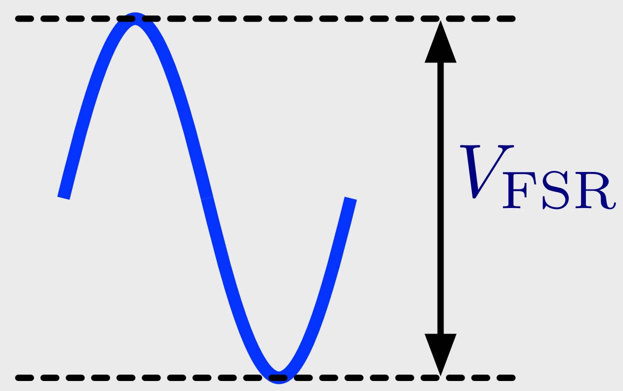
2^{2n} –> 6 dB/bit



Parseval theorem: Energy (power) calculated in time and in frequency is the same

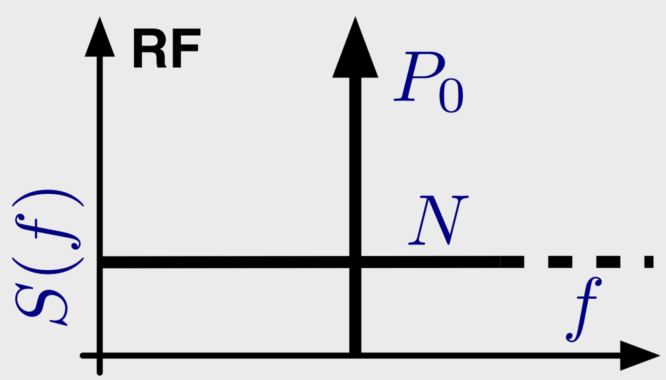
$$N = \frac{V_{\rm FSR}^2}{6 \times 2^{2n}\,\nu_s} \qquad \mathrm{V}^2/\mathrm{Hz}$$

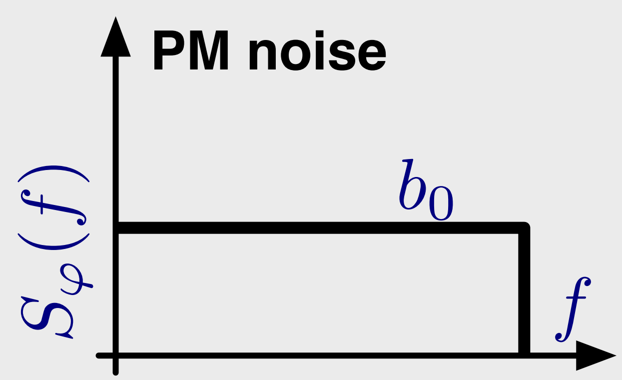
Quantization and PM noise



The **maximum power** is

$$P_0 = \frac{1}{8} V_{\text{FSR}}^2 \qquad \text{V}^2$$





In the presence of white noise *N*, the **PM noise** is

$$b_0 = \frac{N}{P_0} \qquad \text{rad}^2/\text{Hz}$$

Recall the quantization noise

$$N = \frac{V_{\text{FSR}}^2}{6 \times 2^{2n}\, \nu_s}$$

The white PM noise is

$$b_0 = \frac{4}{3}\,\frac{1}{2^{2n}\,\nu_s} \qquad \text{rad}^2/\text{Hz}$$

Example:
14 bit, 1 GHz –> –173 dB
14 bit , 400 MHz –> –169 dB
12 bit, 300 MHz –> –156 dB

Is b_0 (white PM) affected by ν_0?

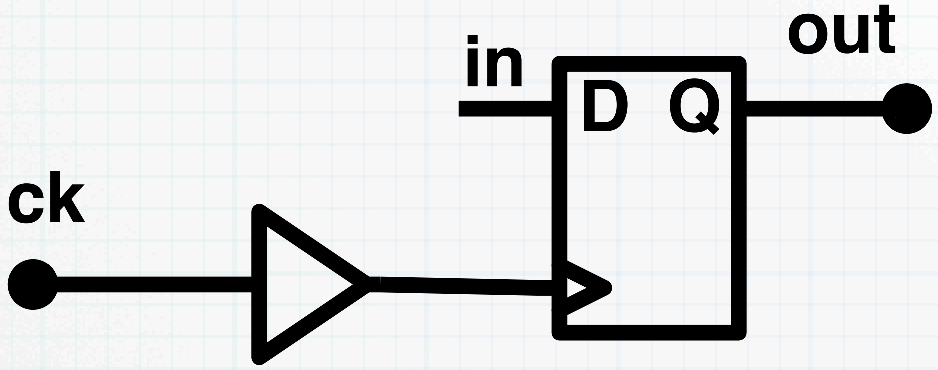
- Consider two synthesized signals, $\nu_0 < \nu_1$ (i.e., $\nu_1 = n\,\nu_0$)
- Same sampling frequency $\nu_s >> \nu_1$

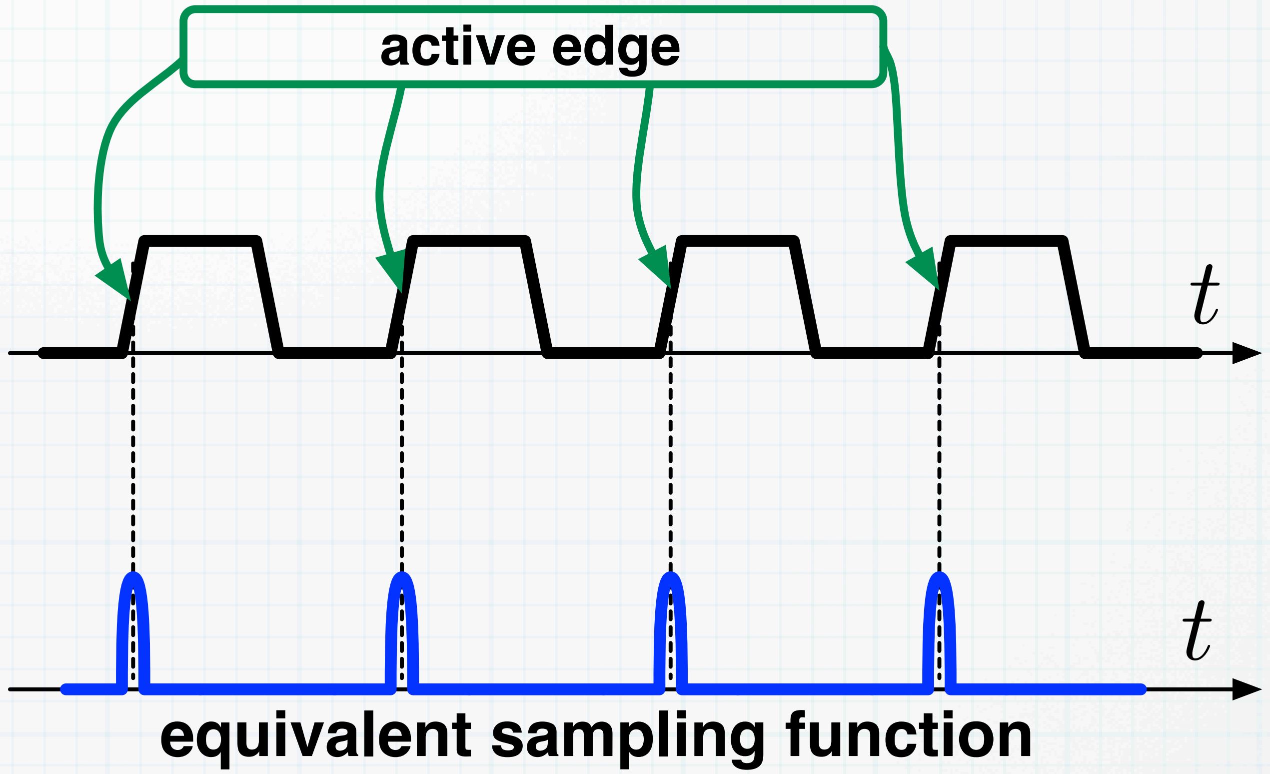
- ν_0 has factor-n more samples-per-period than ν_1
- Does ν_0 have lower PM noise than ν_1 ?

- The answer is NO!

- Analyzing at the Fourier frequency f with a resolution bandwidth B, the measurement time is ≈ $1/B$
- The degrees of freedom are ν_s/B, regardless of ν_{out}
- Accordingly, b_0 (white PM noise) at ν_0 and ν_1 is the same

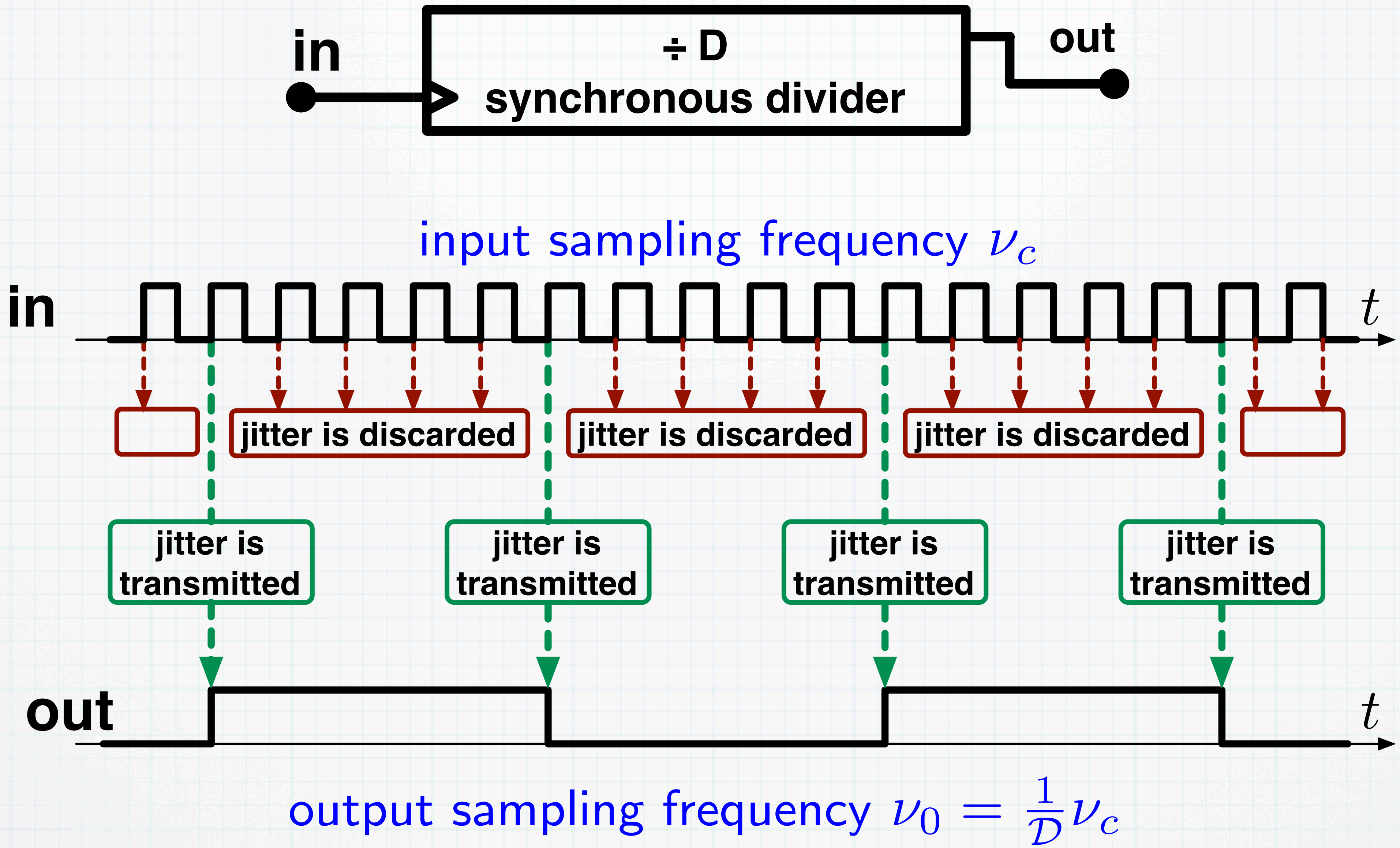
Phase noise sampling





- The input noise is sensed only during the rising edges
- This is equivalent to sampling at the at the clock frequency
- The phase noise in the full input bandwidth is “aliased” to half the clock frequency

Phase noise sampling in dividers



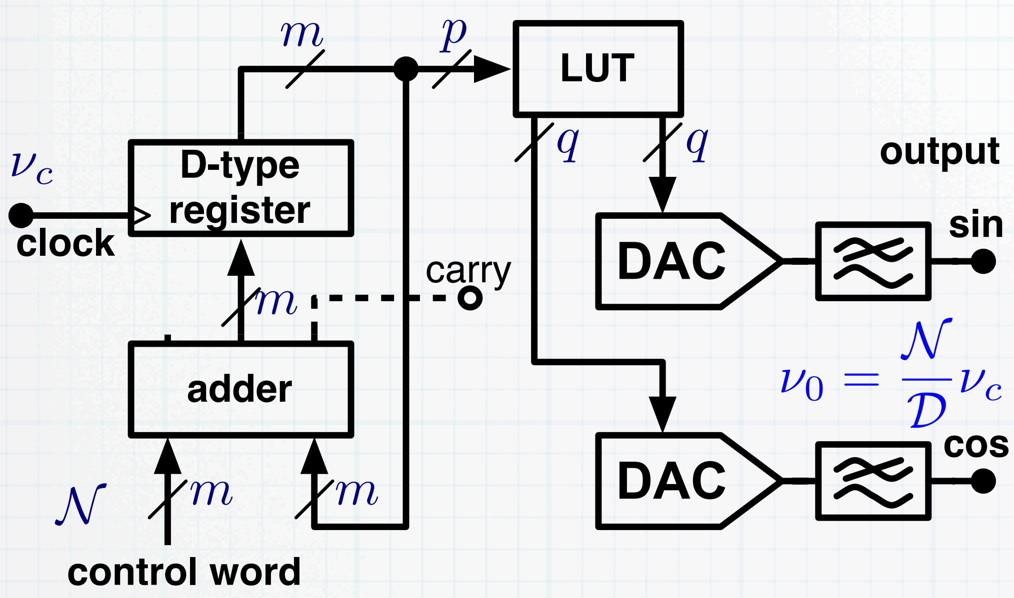
- **The output jitter results from sampling the input jitter at the frequency $\nu_0 = \nu_c / D$**
- **Aliasing increases the white part of S_φ by a factor of *D***

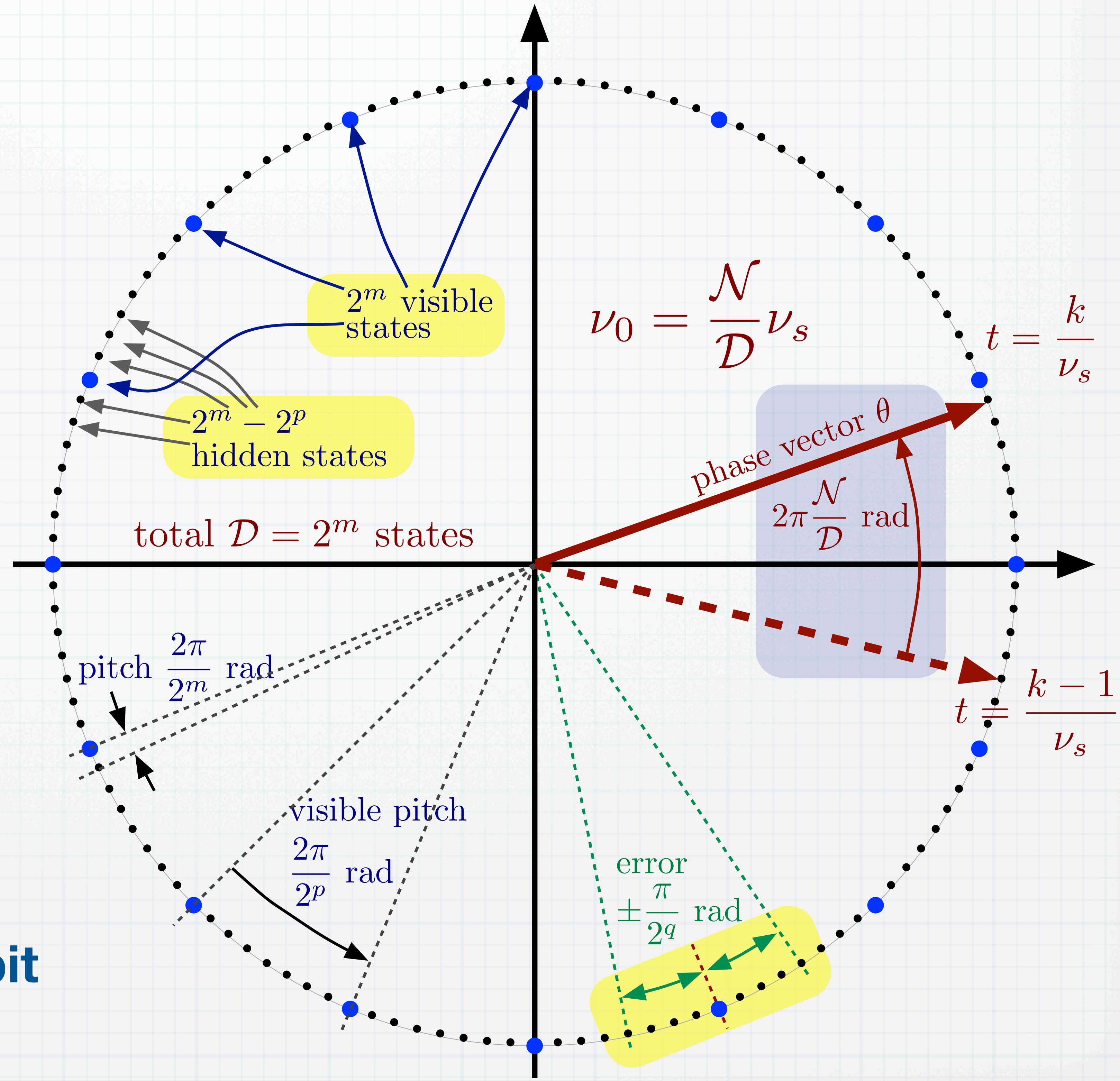
$$(S_\varphi)_{\text{out}} = \frac{1}{D}(S_\varphi)_{\text{in}}$$

- **The $1/D^2$ law still holds for autocorrelated noise (flicker, walk)**

State-variable truncation

$$n_k = (n_{k-1} + \mathcal{N}) \bmod \mathcal{D}, \quad \mathcal{D} = 2^m$$

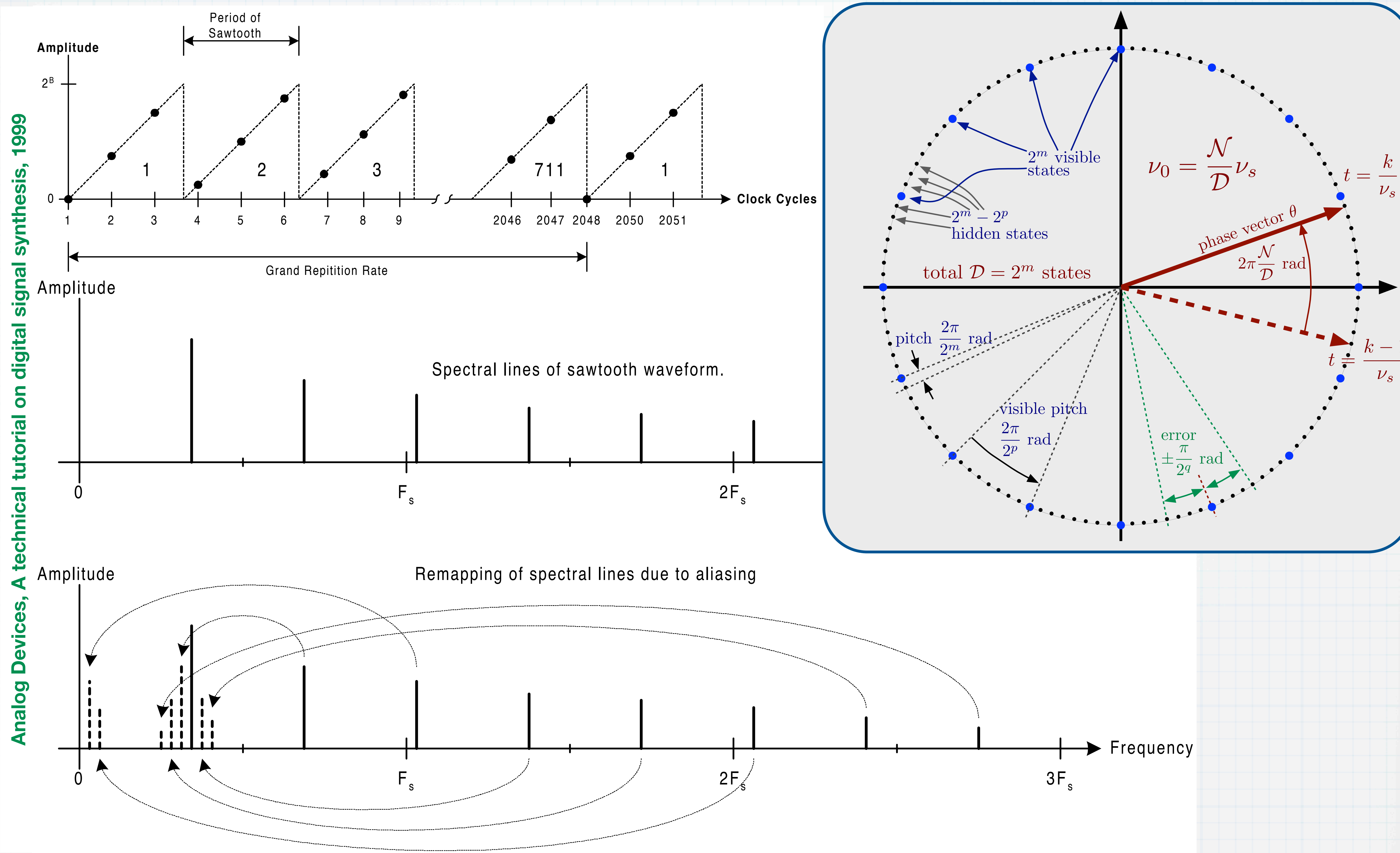




- **Only quantization shows up with full m-bit conversion**
- **Technology –> q max**
- **Why p > q**
- **Slow pseudorandom beat, 3d 6h 11m 15s @ 1 GHz, 48 bit**
- **Spurs –> next**

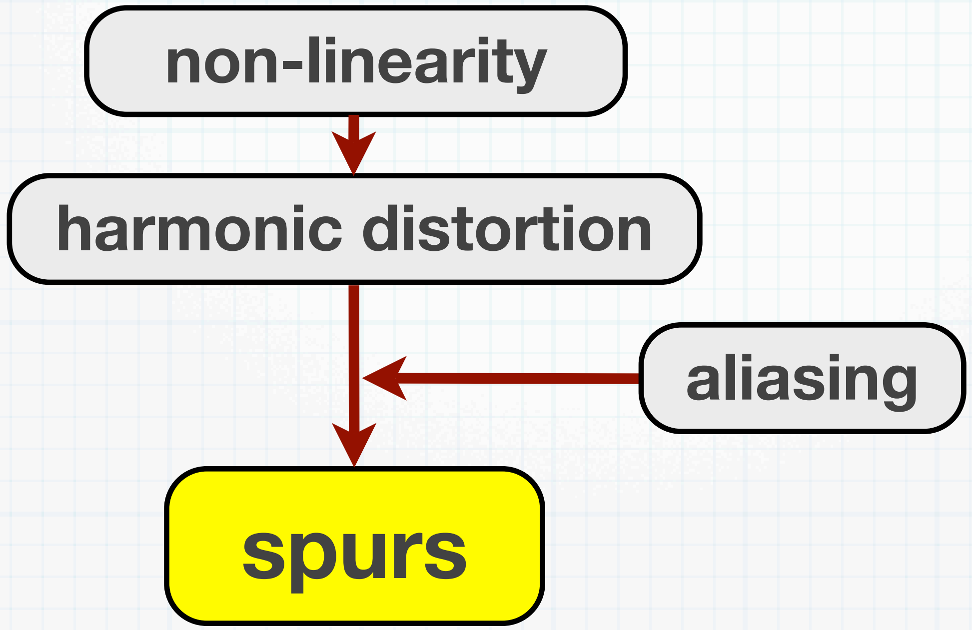
Truncation generates spurs

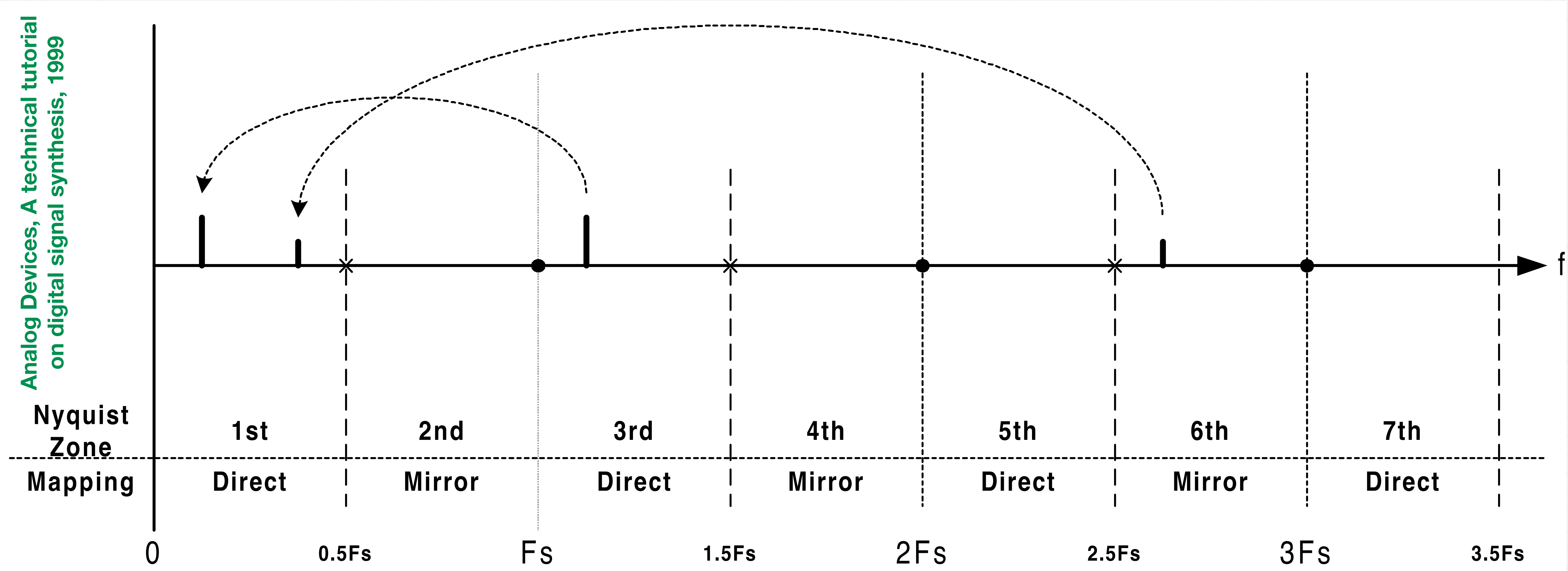
Analog Devices, A technical tutorial on digital signal synthesis, 1999



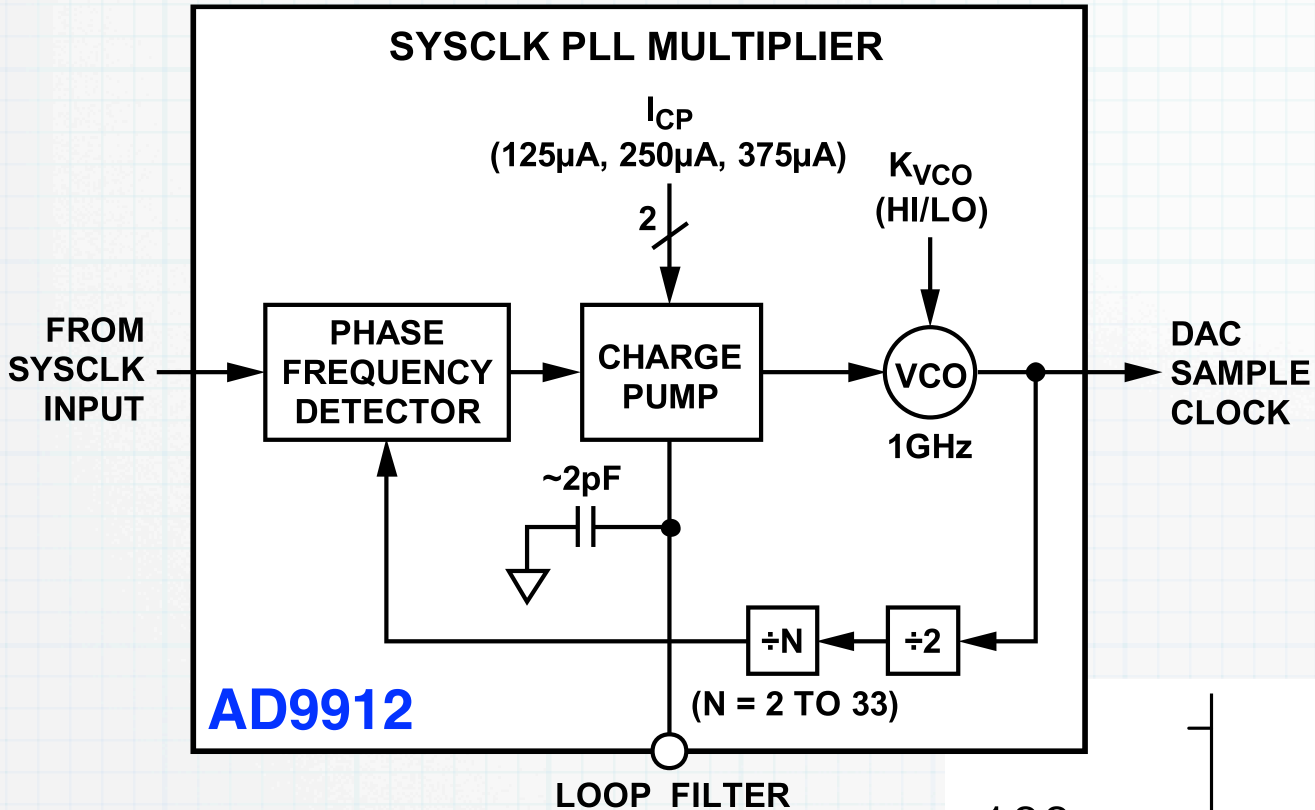
The power of spurs comes at expenses of white noise – yet not as one-to-one

Nonlinearity generates spurs



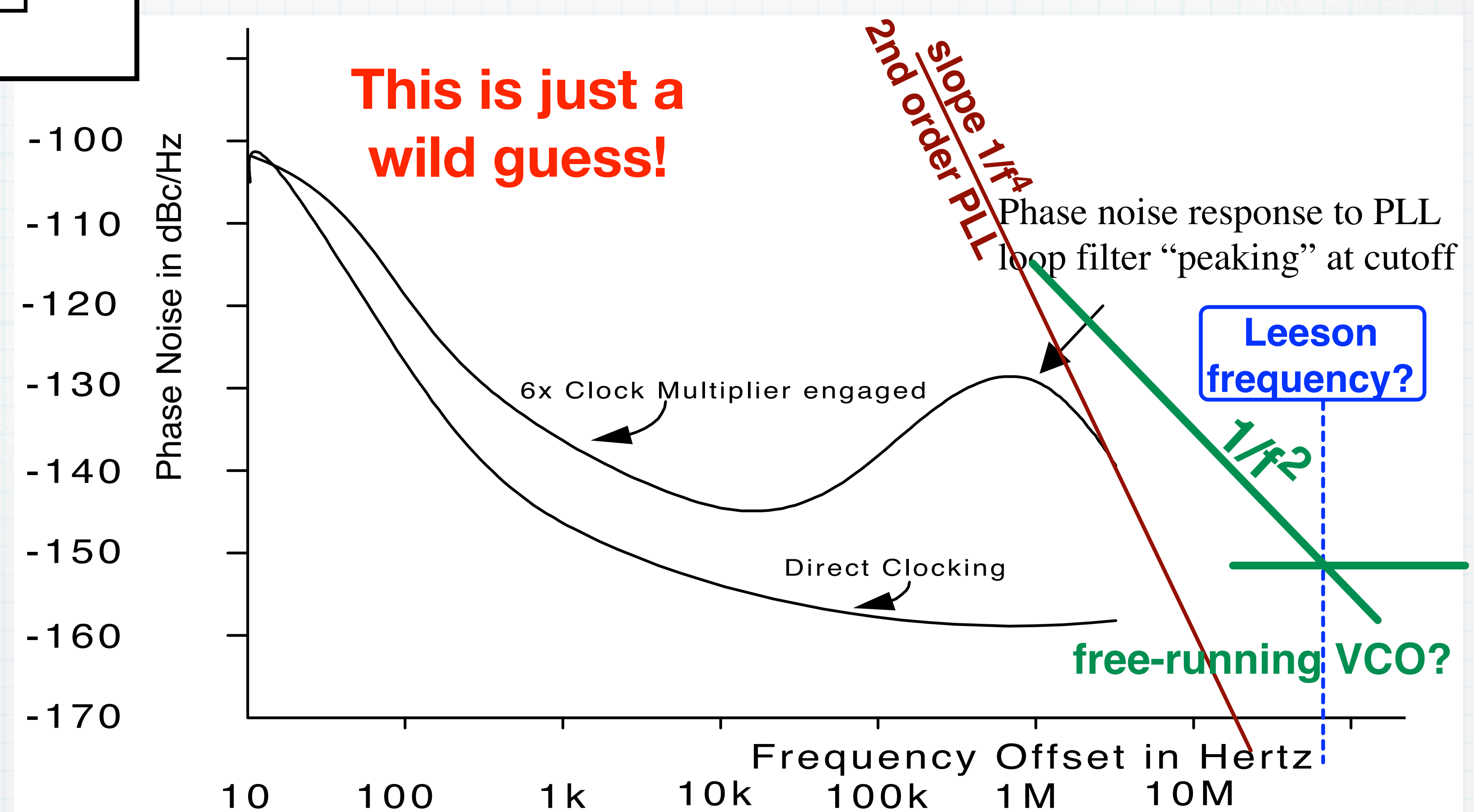


PLL clock multiplier



- On-Silicon LC oscillator
  - (also used in other AD devices)
- Literature suggests Q ≈ 5…10
  - Leeson f_L = 50–100 MHz
- Tight PLL is needed
- Divider noise
- No data from the manufacturer

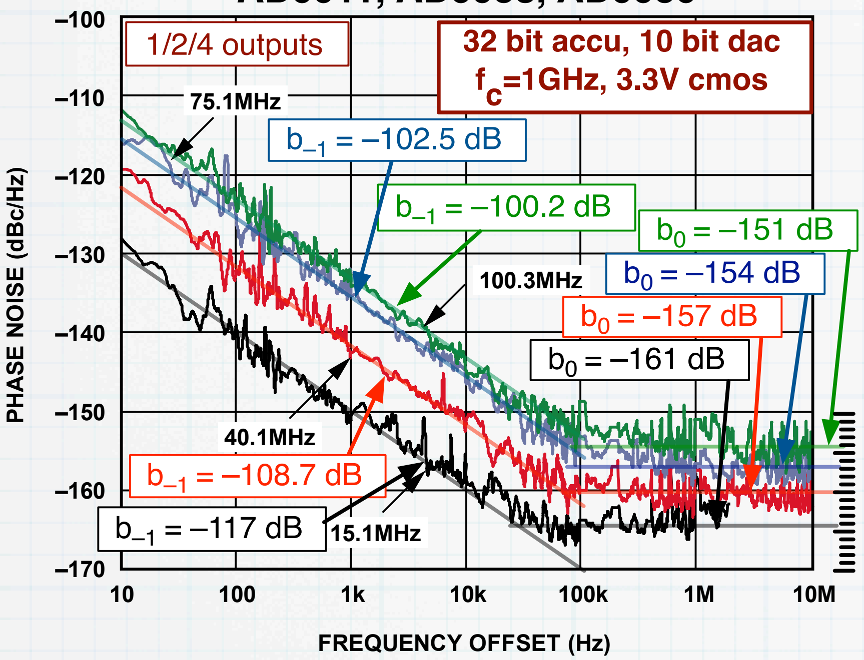
The AD 9854 is likely similar, yet the VCO frequency is 300 MHz



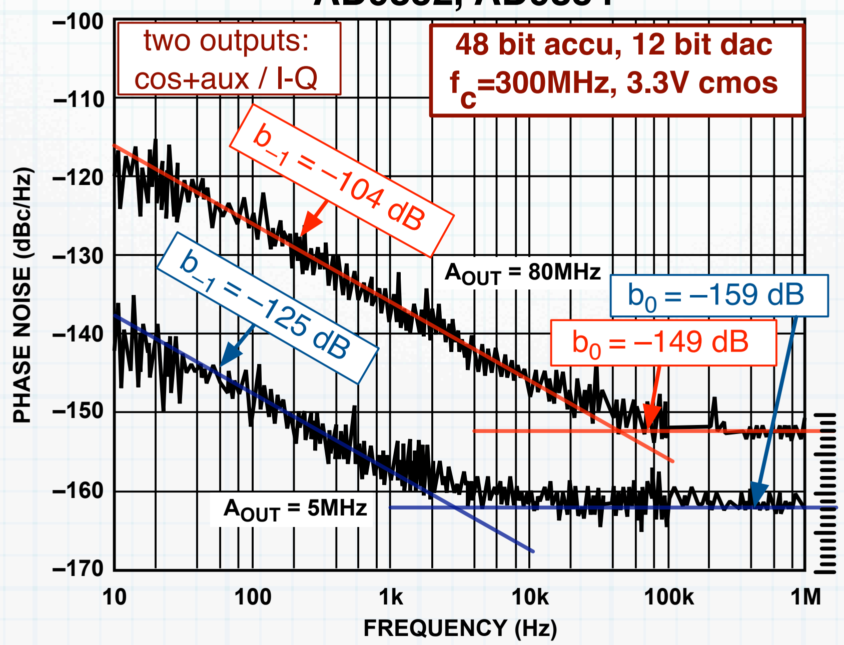
3.3 V: lower PM noise than 1.8 V

Probably related to the cell size and to the dynamic range

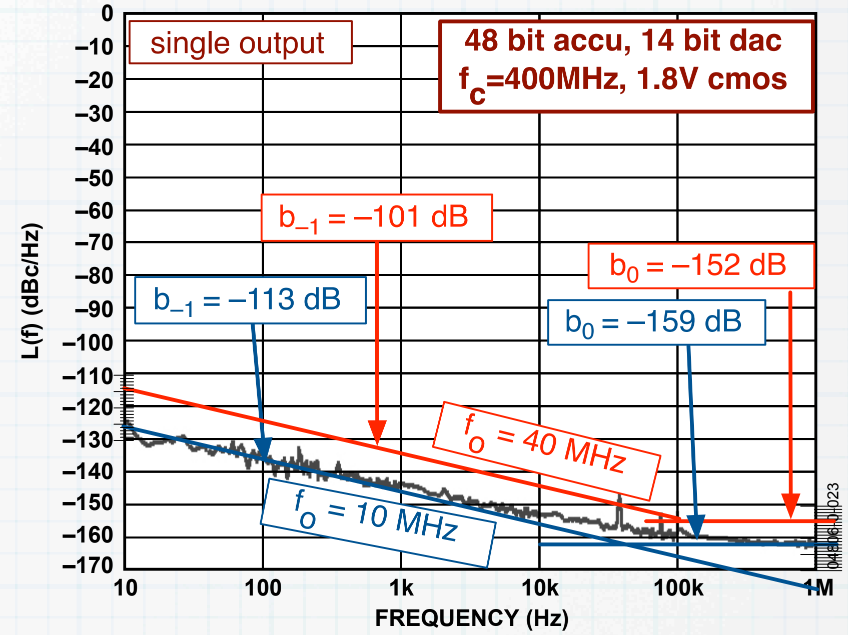
AD9911, AD9958, AD9959



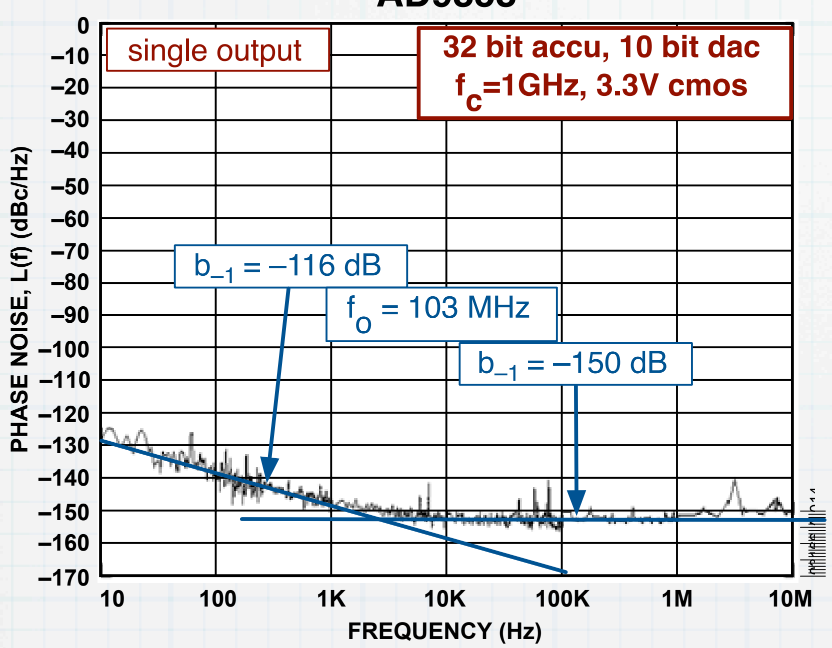
AD9852, AD9854



AD9956



AD9858



AD9912

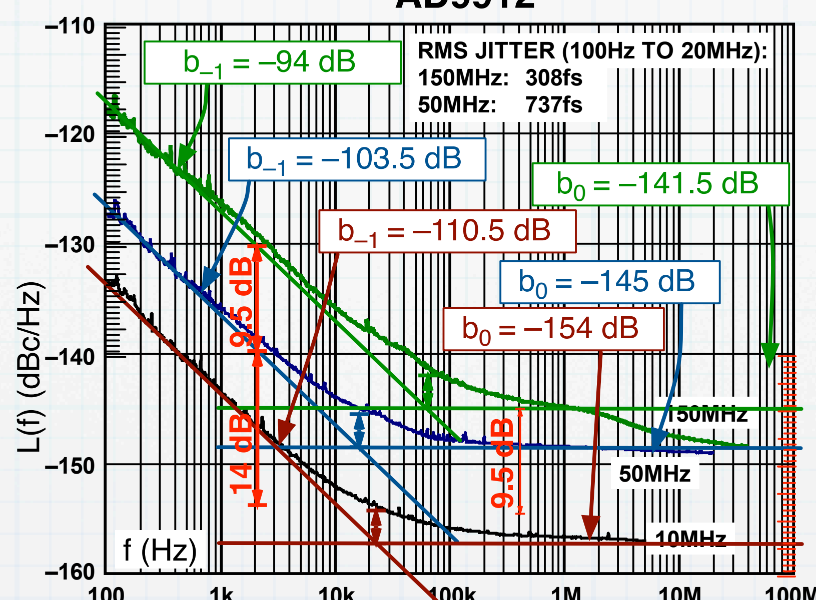
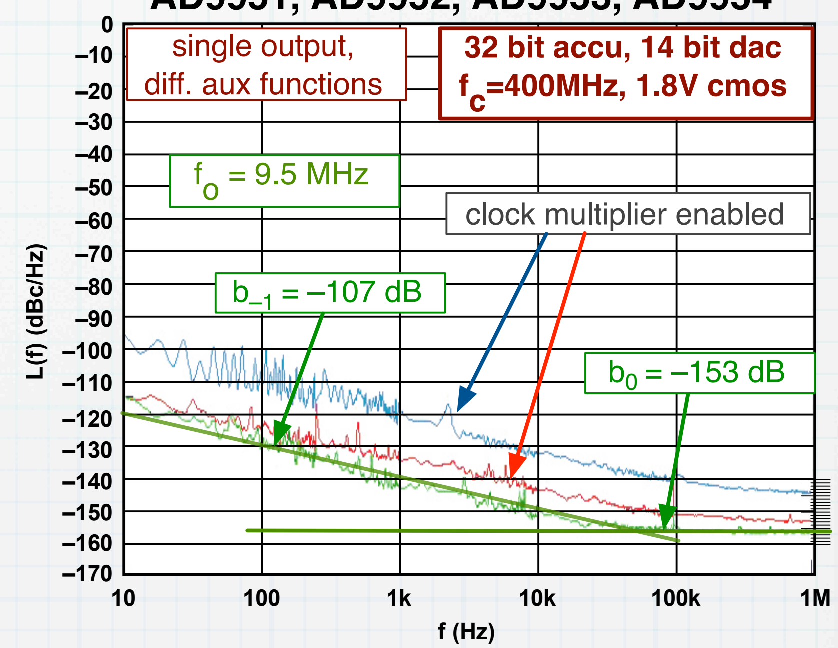


Figure 16. Absolute Phase Noise Using CMOS Driver at 3.3 V, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed) DDS Run at 200 MSPS for 10 MHz

AD9951, AD9952, AD9953, AD9954



E. Rubiola, Mar 2007 (adapted from the Analog Devices data sheets)

Plots originally used to extract the noise parameters

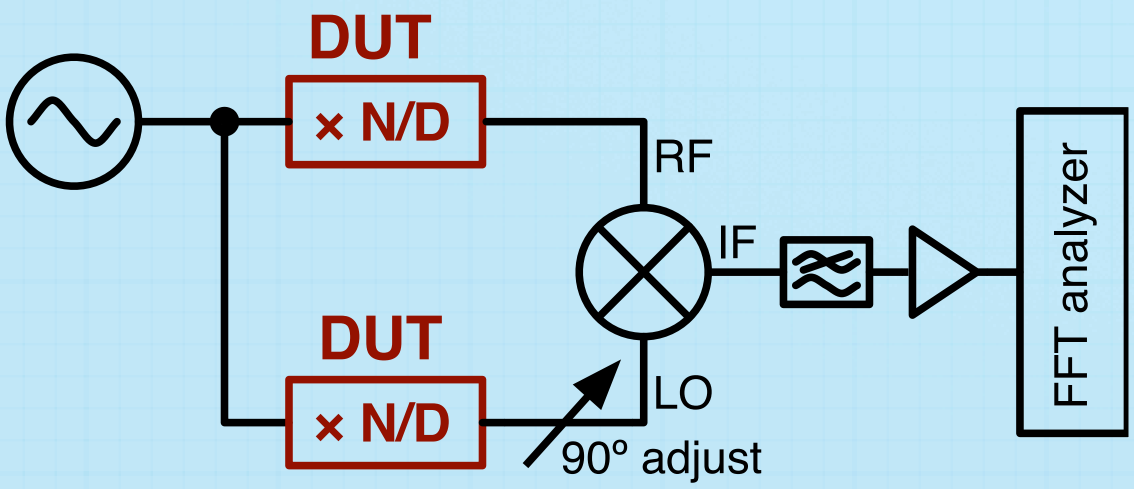
Experiments

- AD9912 demo board
- AD9854 (9914) demo board
- Claudio's AD9854 board
  - V1 – Current feedback OPA output stage
    - 25Ω input impedance, 8 nV/√Hz noise, kHz coupled
  - V2 – Balun and MAV-11 RF output amplifier
    - F = 3.6 dB, AC coupled (≥1–2) MHz
      - Specified above 50 MHz, yet works well below

Experimental method (PM noise)

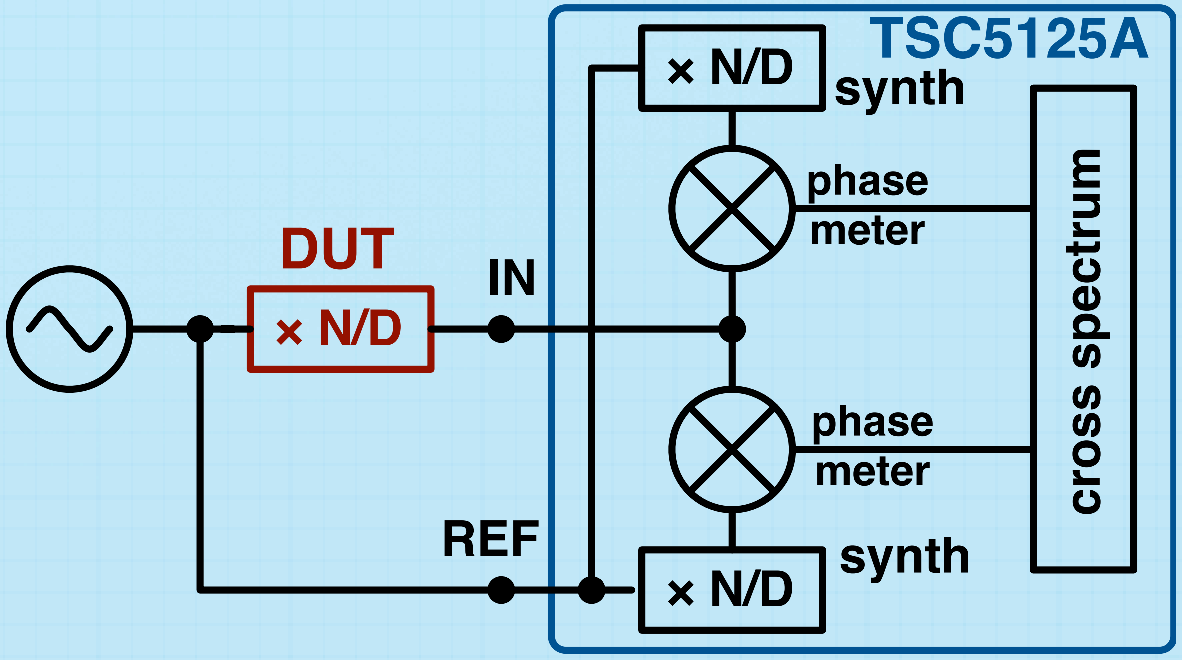
- Pseudorandom noise, slow beat (days)
- The probability that two accumulators are in phase is ≈ 0
- Two separate DDS driven by the same clock have a random and constant delay
- The delay de-correlates the two realizations, which makes the phase measurement possible

Single channel

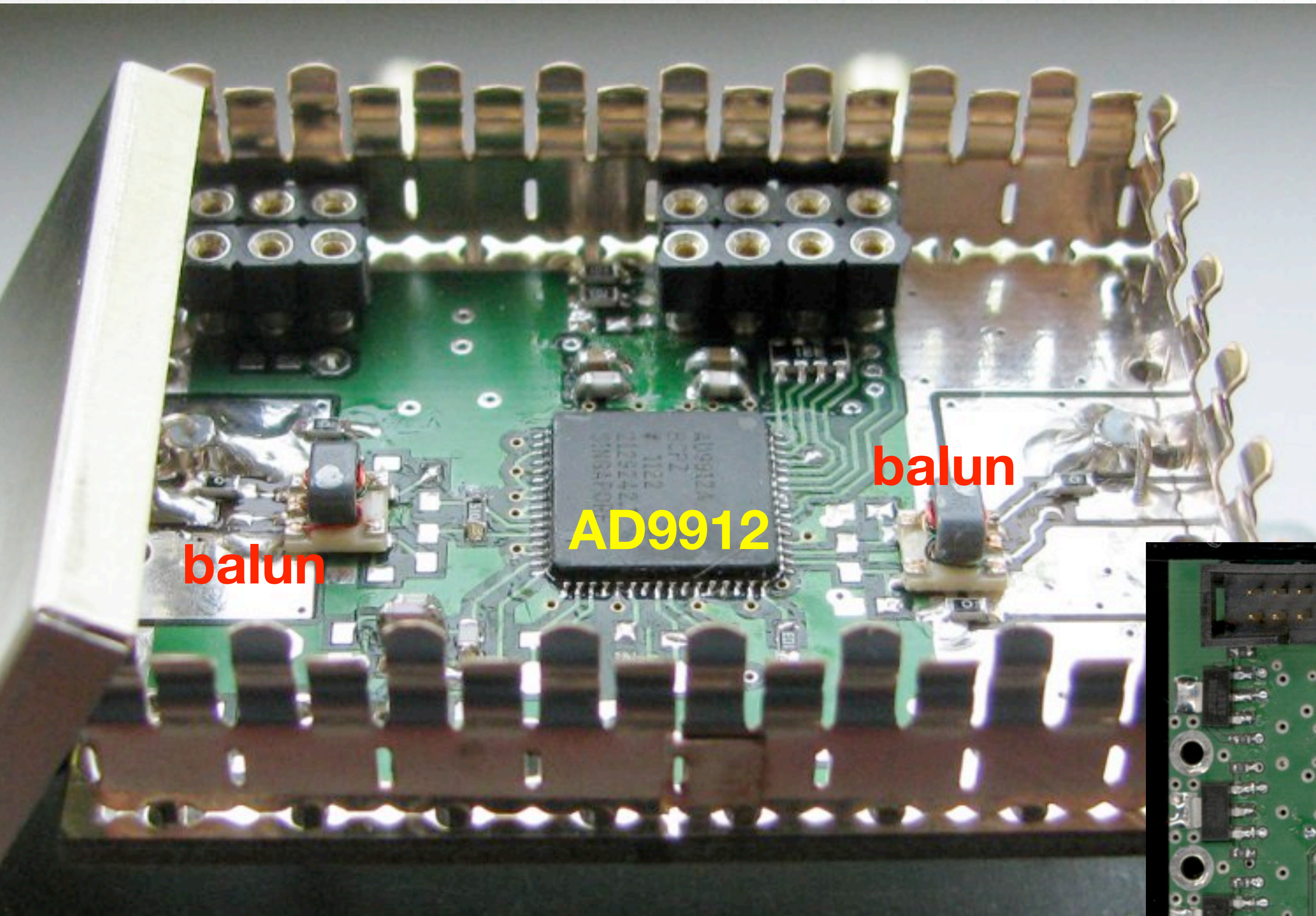


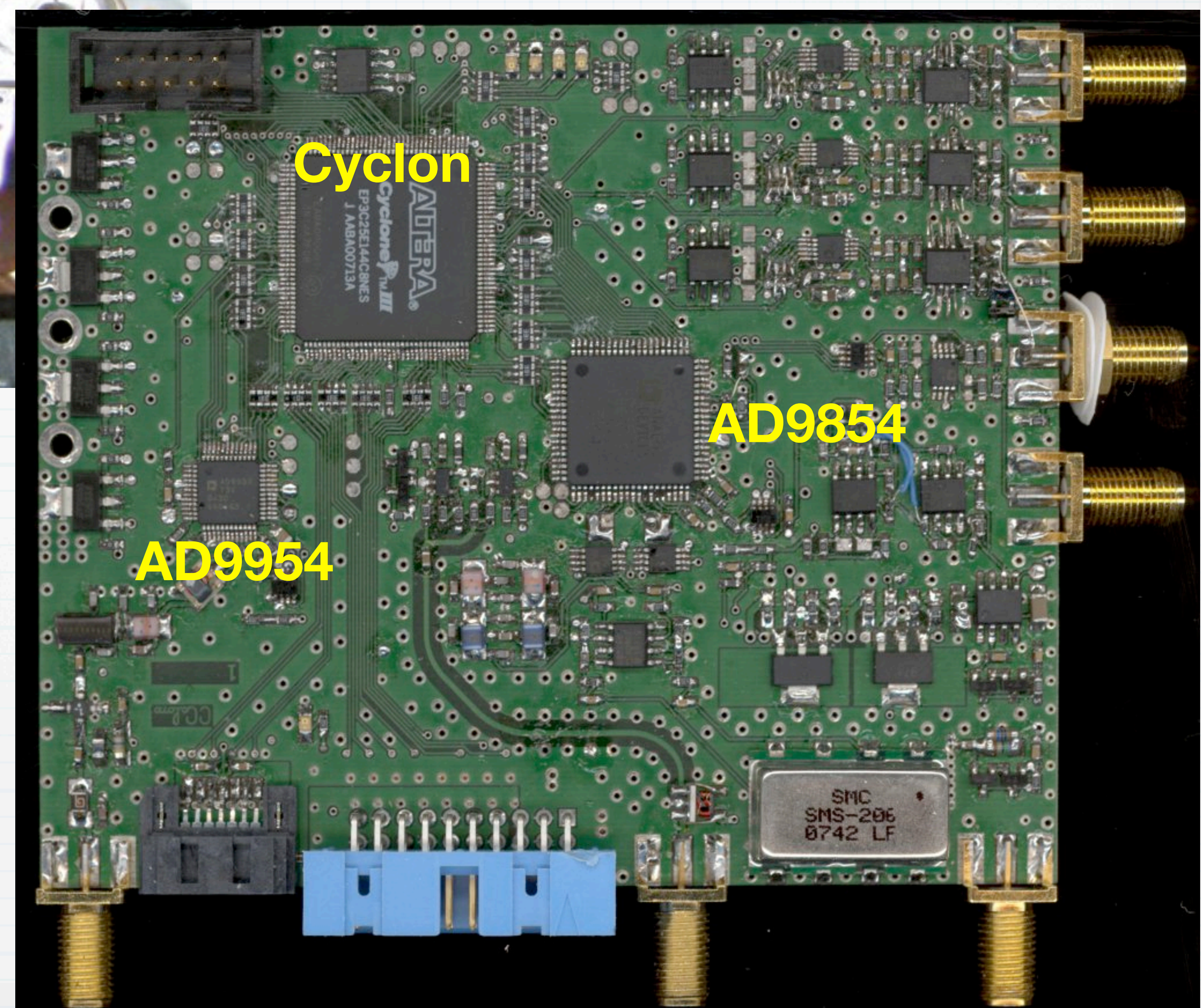
Dual channel

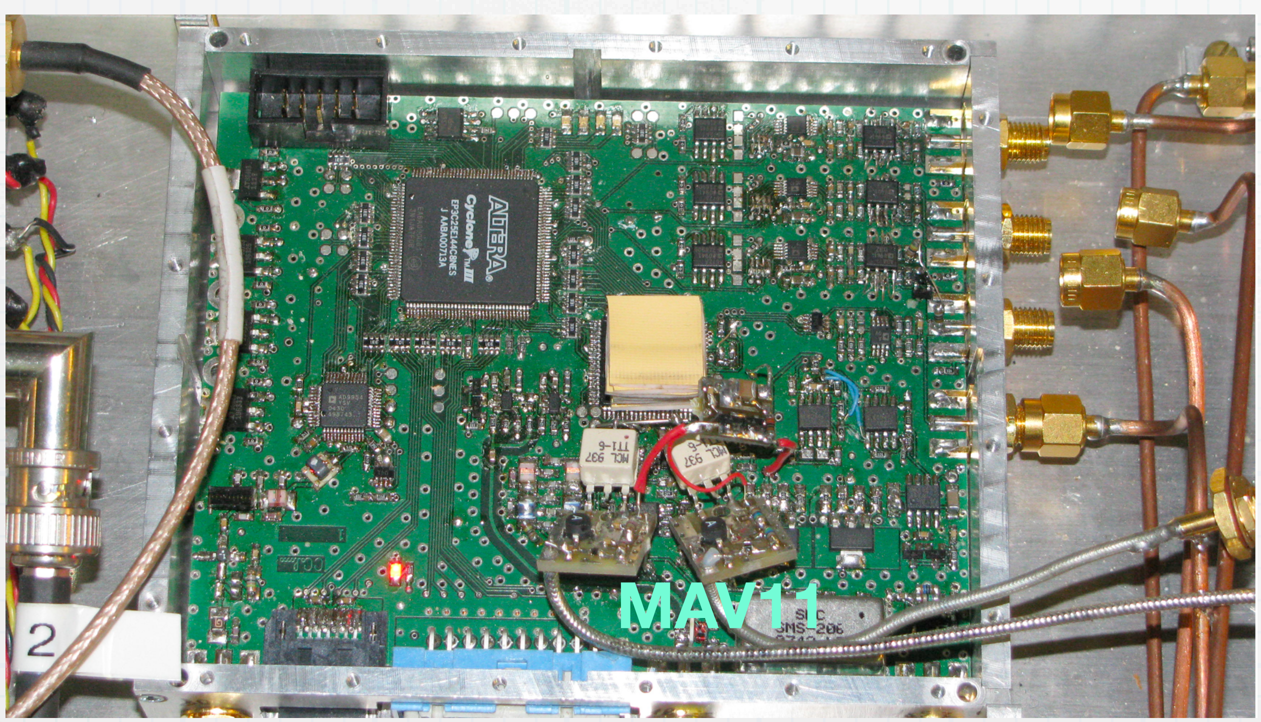
kind of virtual mixer, after (sub)sampling & direct ADC



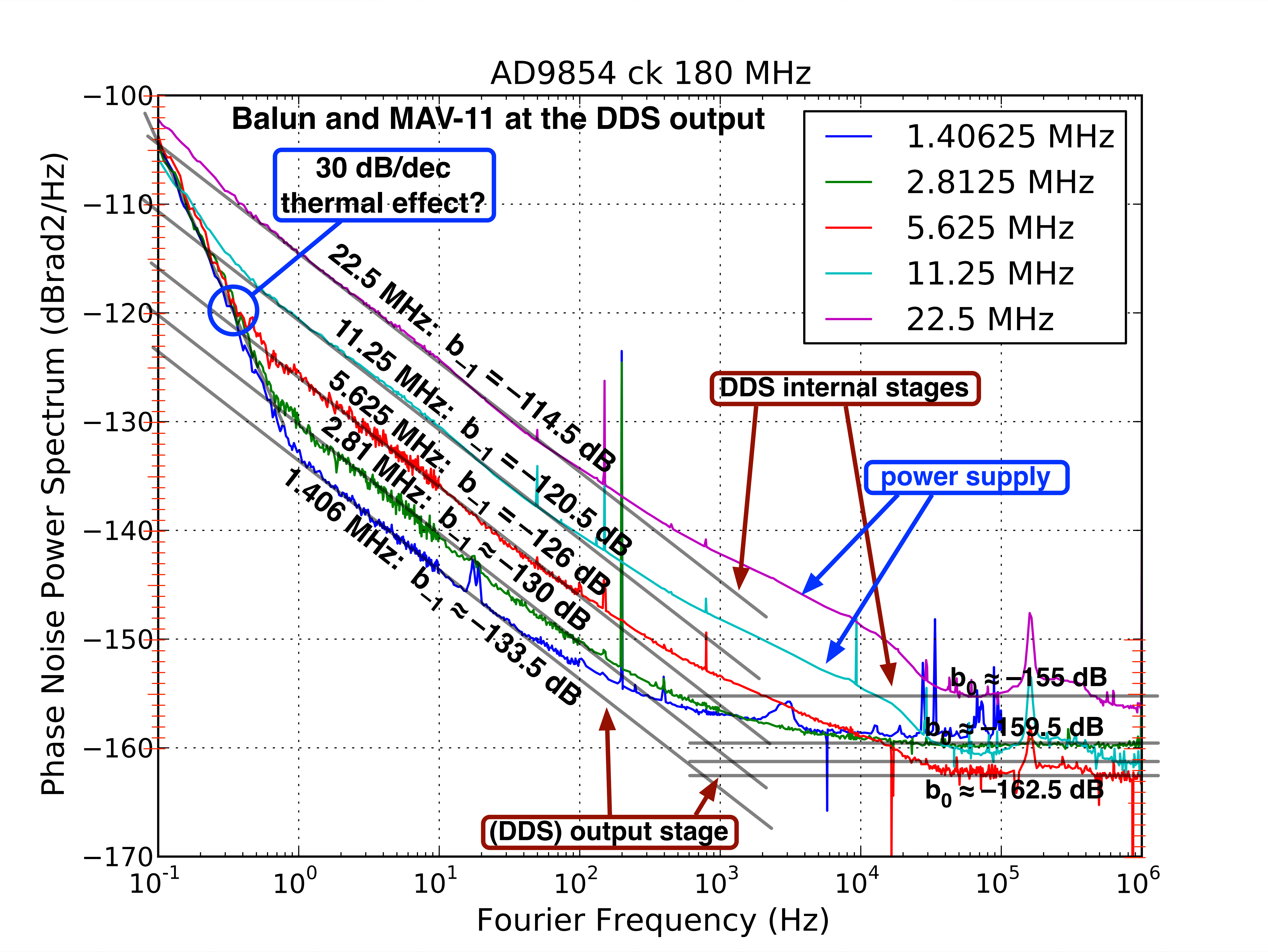
Claudio’s prototypes





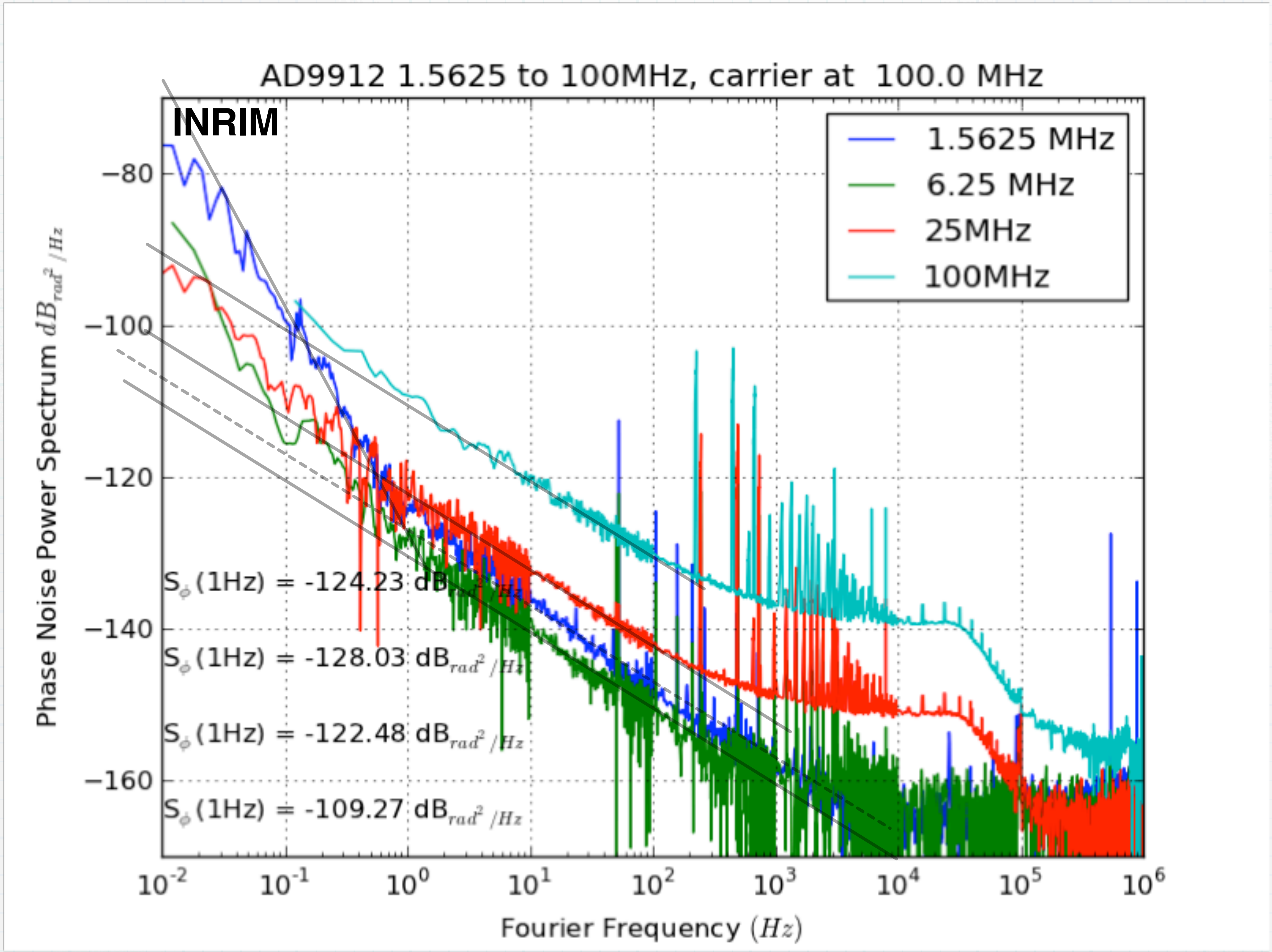


PM noise vs. output frequency

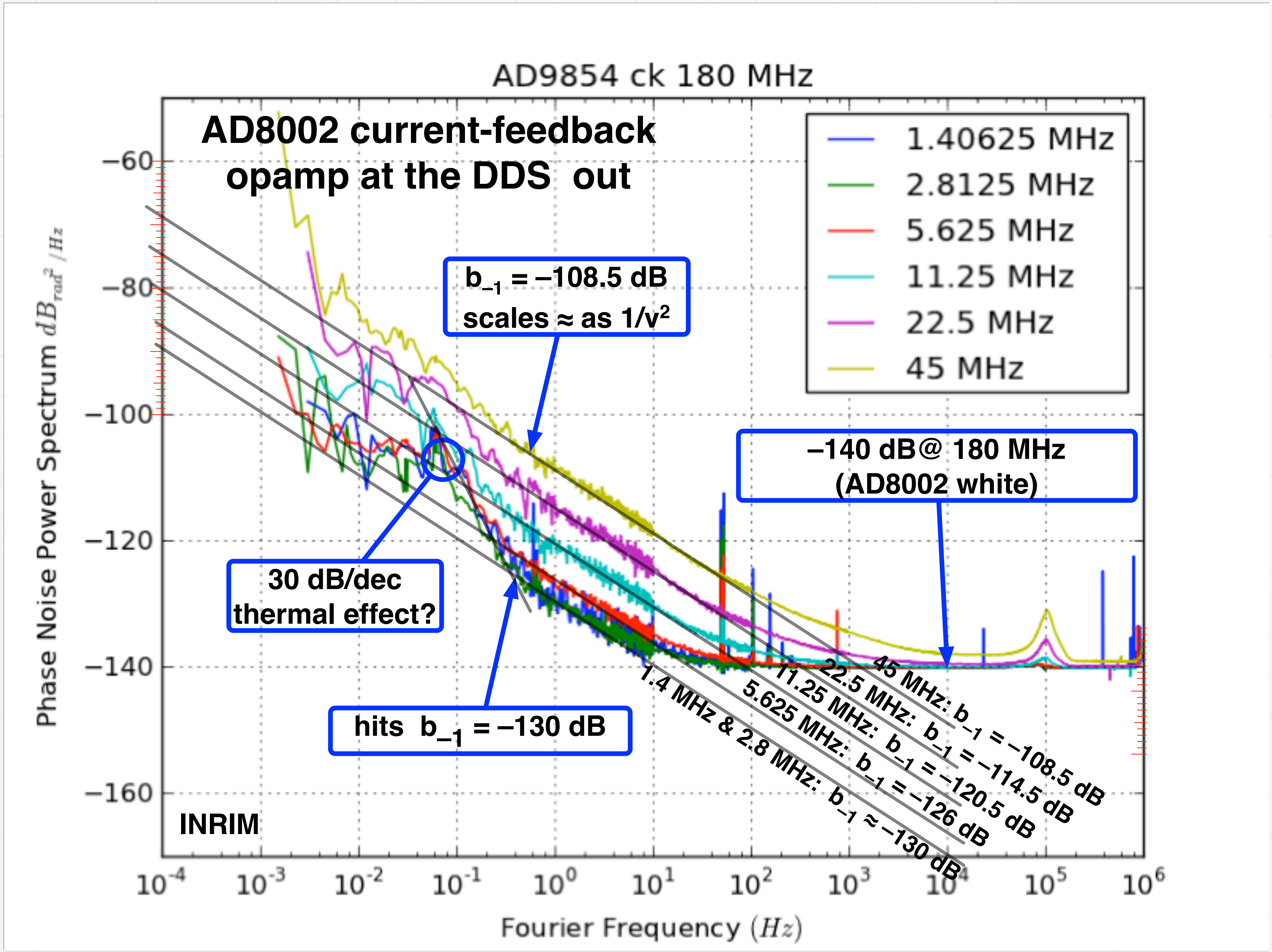


AD9912 noise vs. out frequency

– low Fourier frequencies –

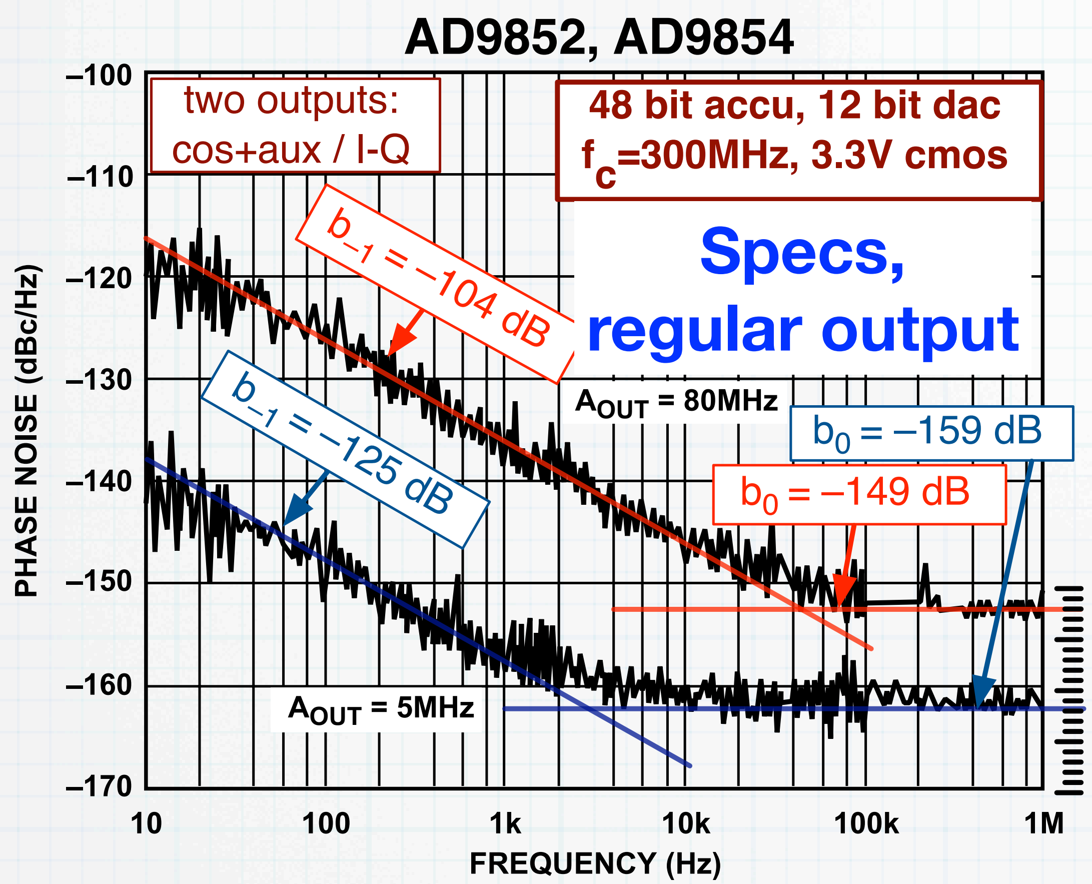


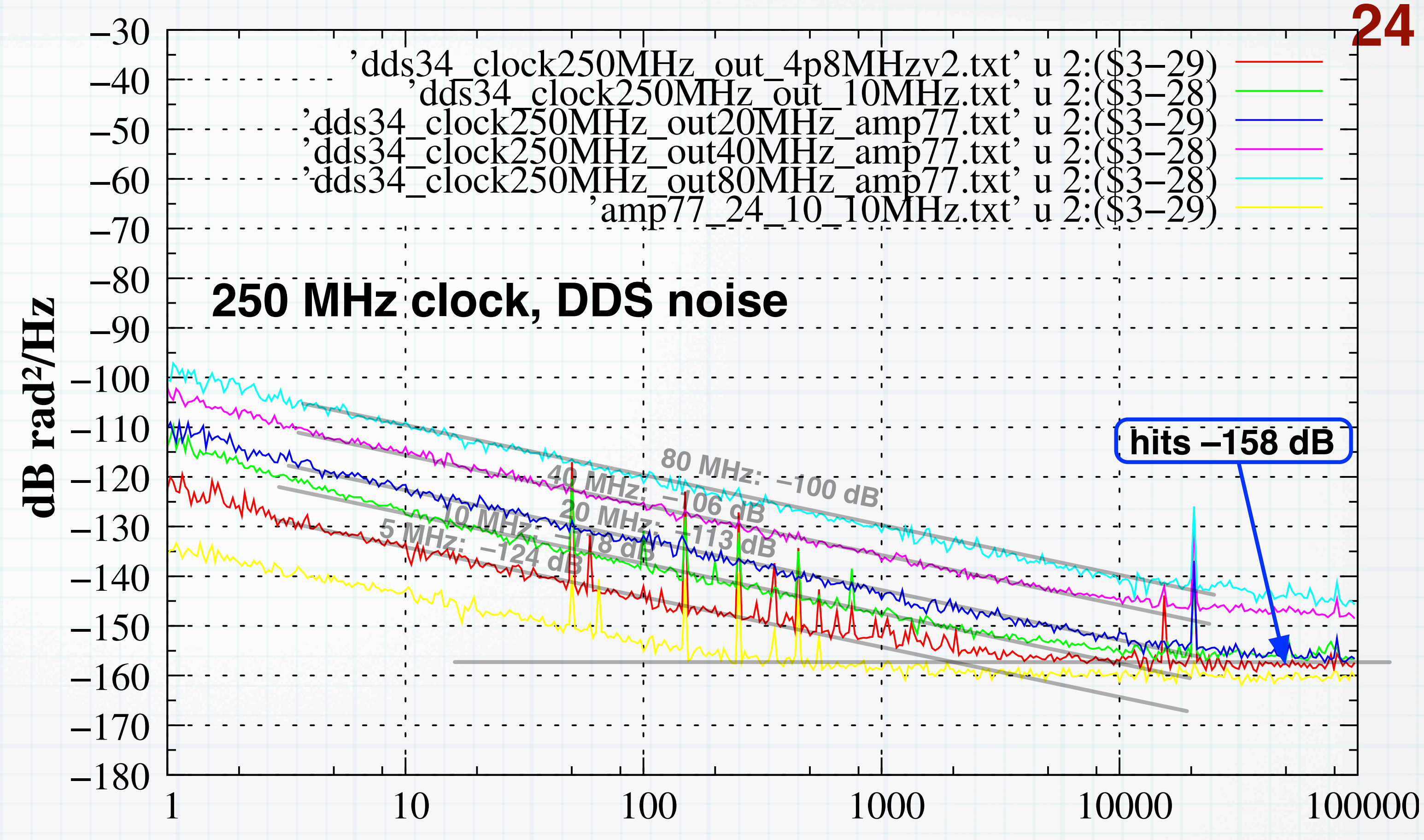
PM noise vs. output frequency



- **The –140 dB floor is due to AD8002 at the DDS output**
- **The flicker is unchanged (comes from the DDS)**

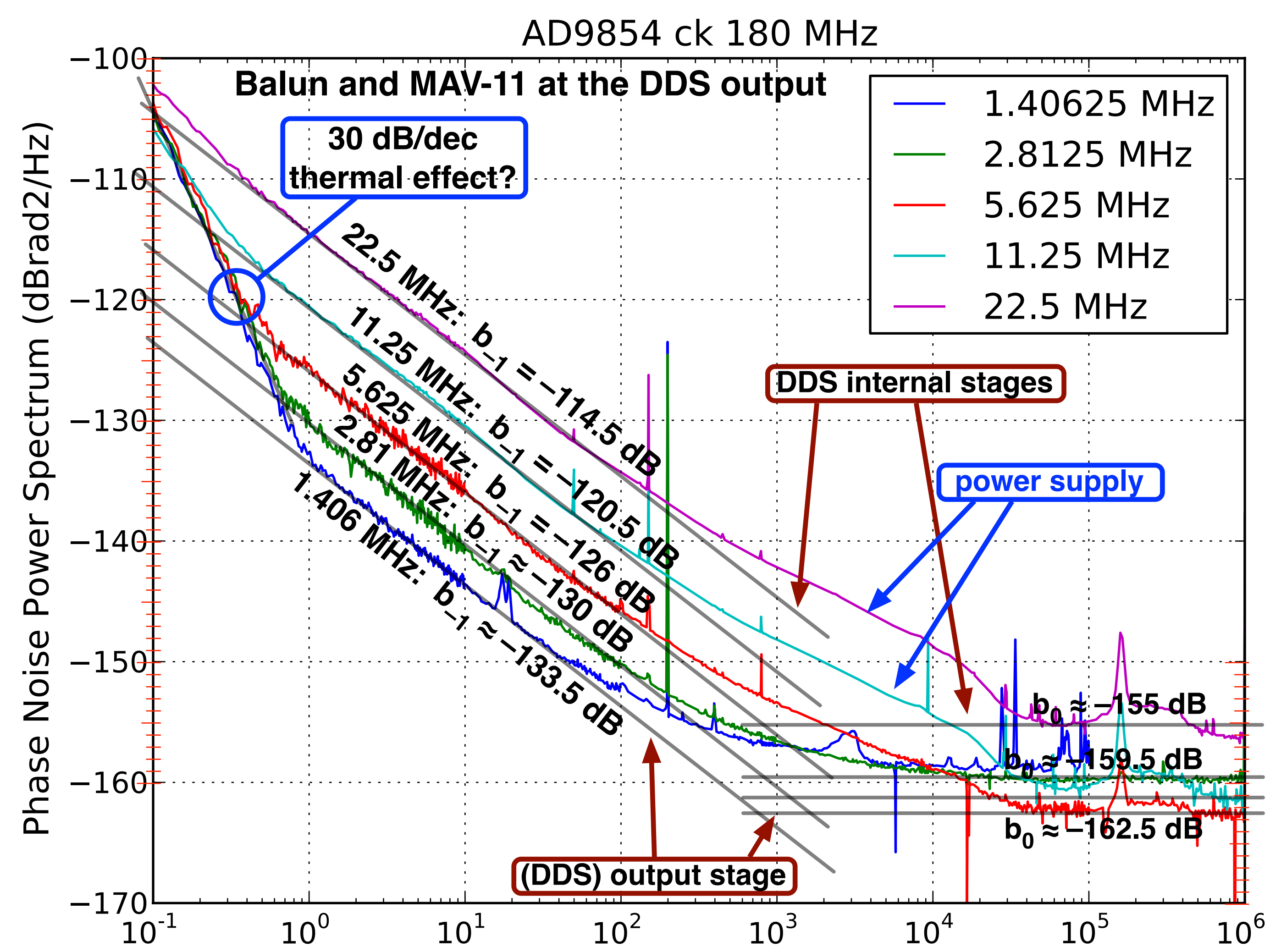
AD9854 noise





Flicker is in fair agreement

White is made low by spurs



Basic formula for white noise

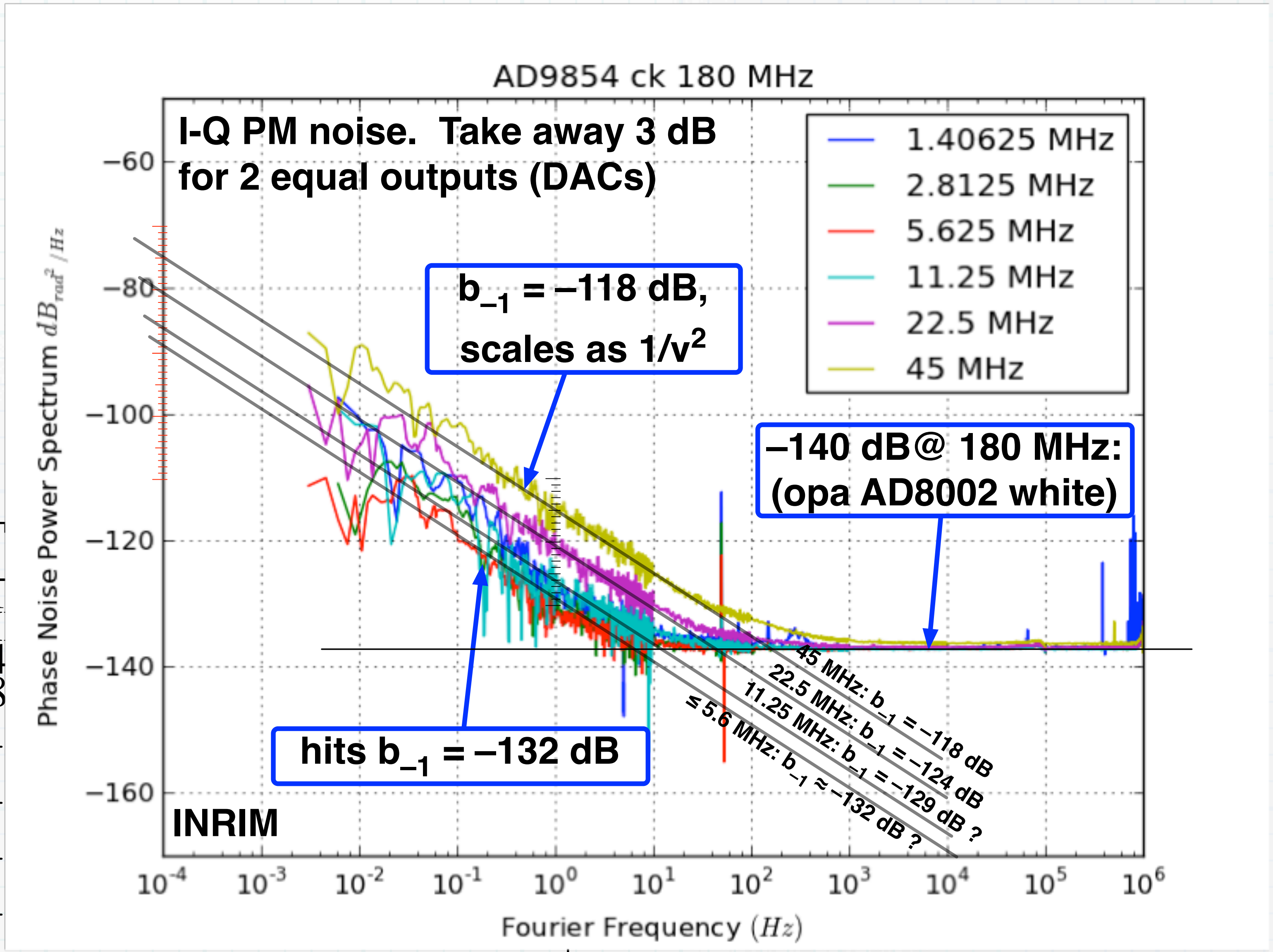
$$b_0 = \frac{4}{3}\,\frac{1}{2^{2n}\,\nu_s} \quad \mathrm{rad}^2/\mathrm{Hz}$$

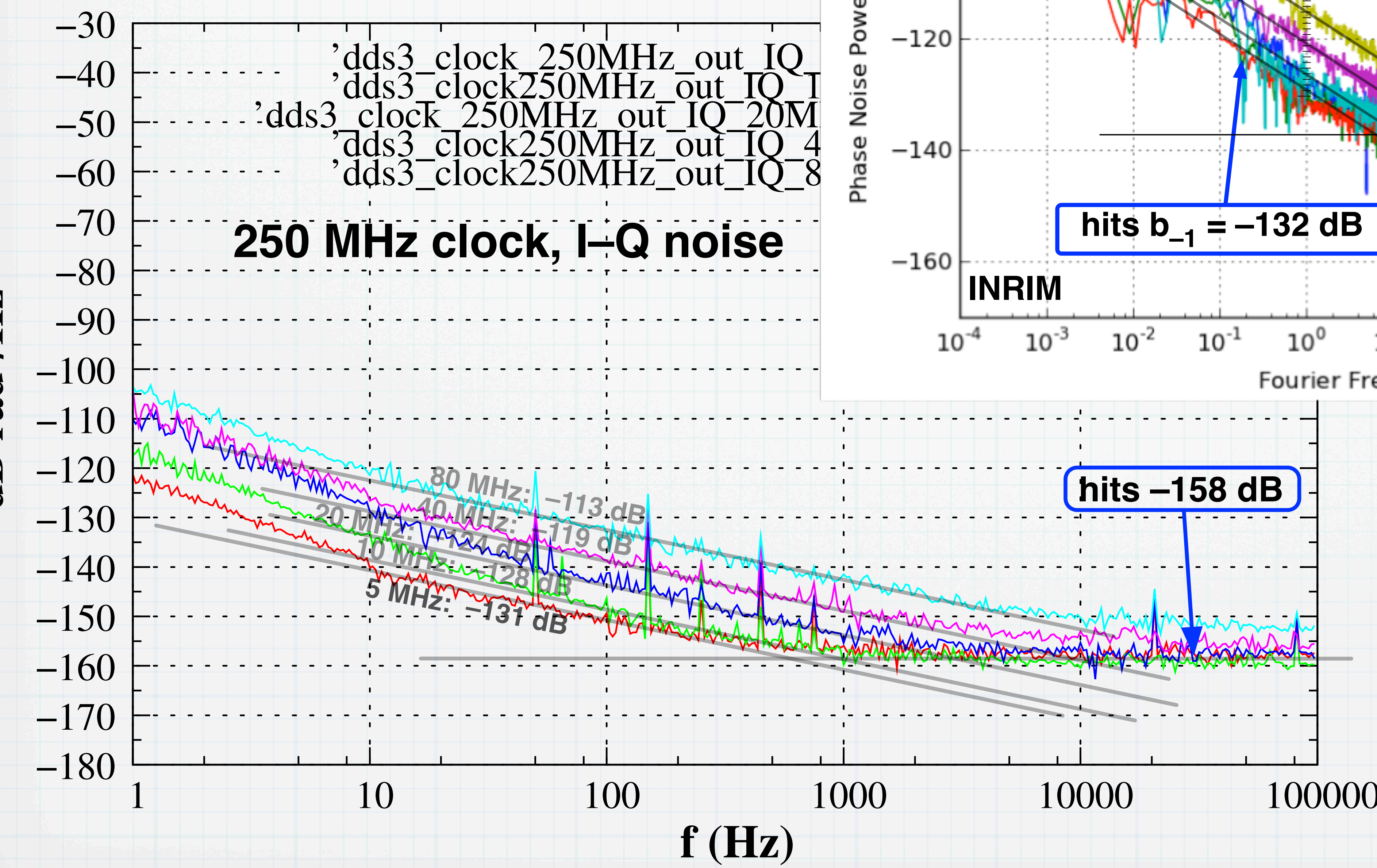
who	meas, dB	math, dB	clock, MHz
specs	–159	–155.8	300
YG	–158	–155.0	250
CC	–162.5	–153.6	180

AD9854 I–Q noise

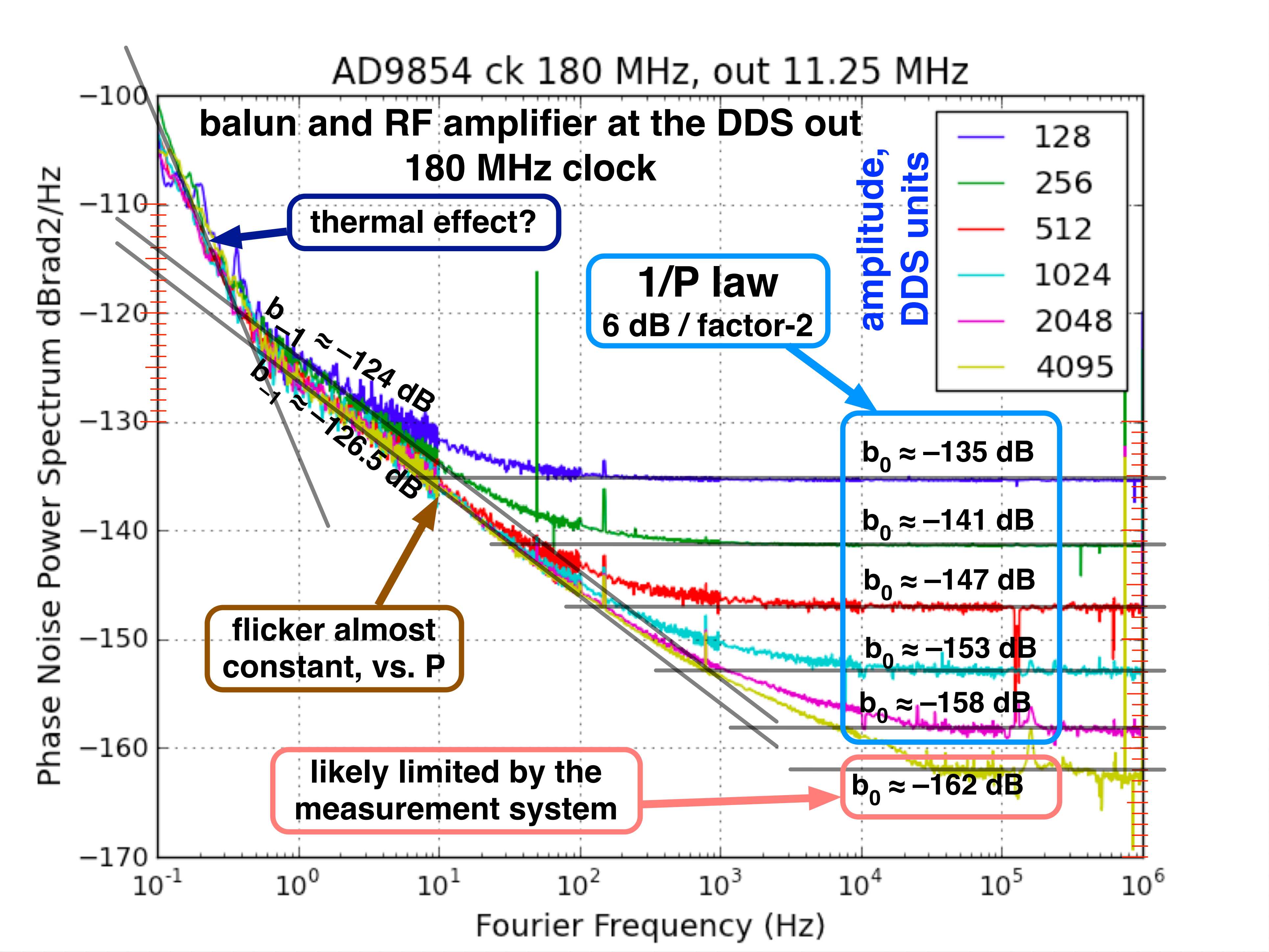
Flicker is in quite a good agreement between YG and CC

I–Q spectra cannot be compared to specs



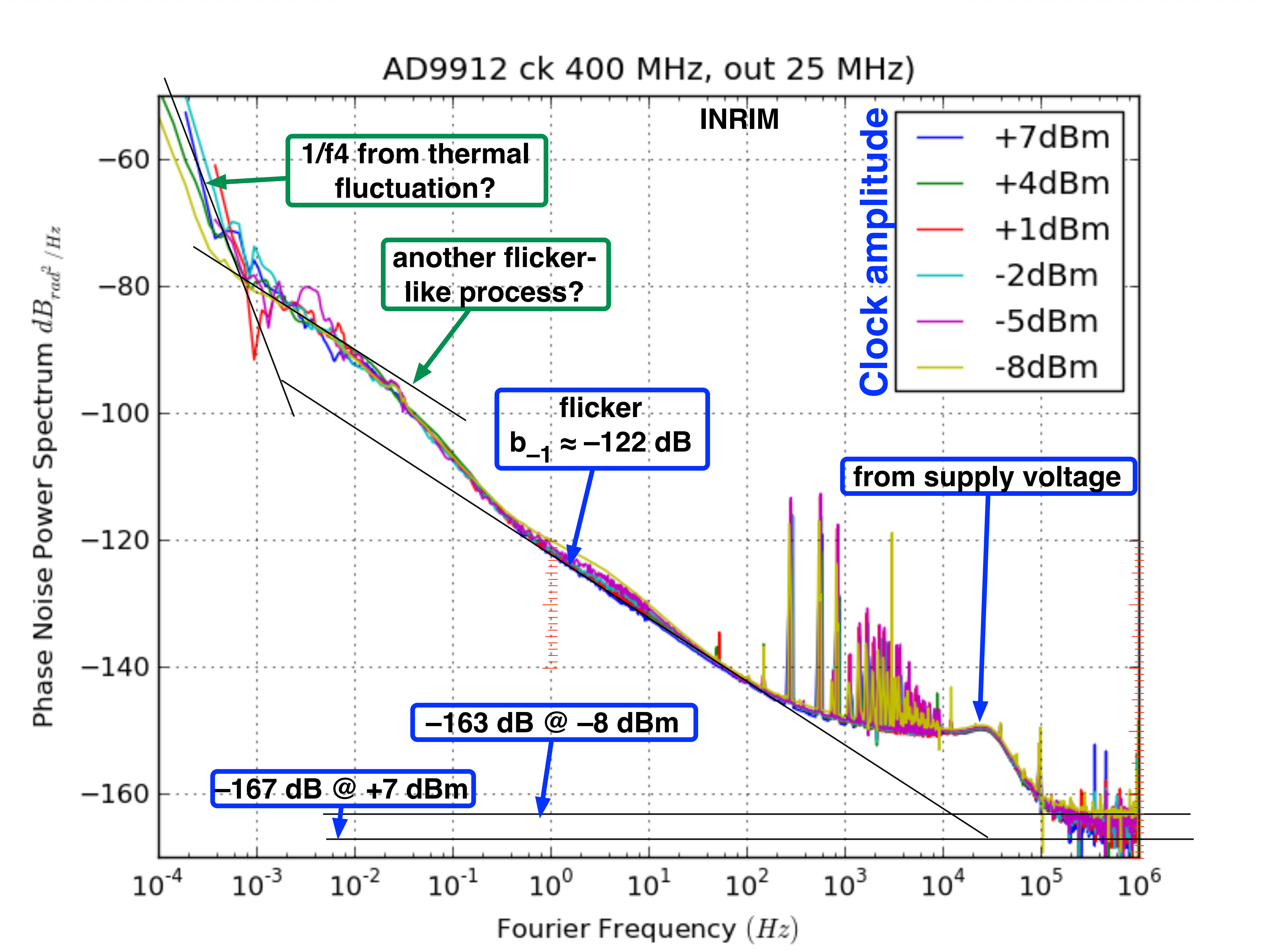


PM noise vs. output amplitude

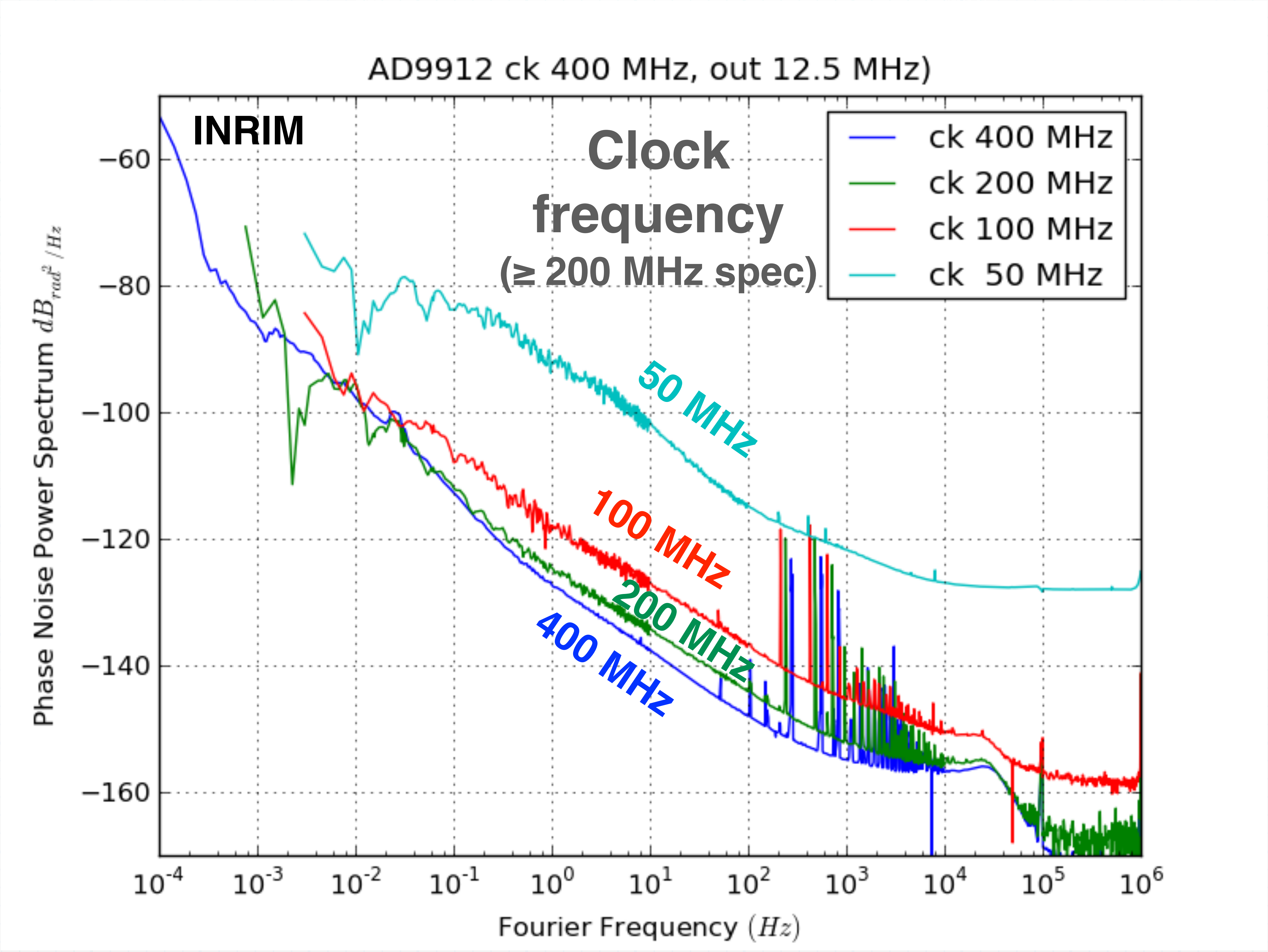


- PM noise scales 6 dB per factor-of-two output amplitude
- Signature of digital multiplication: lower amplitude is obtained by reducing the integer number at the DAC input

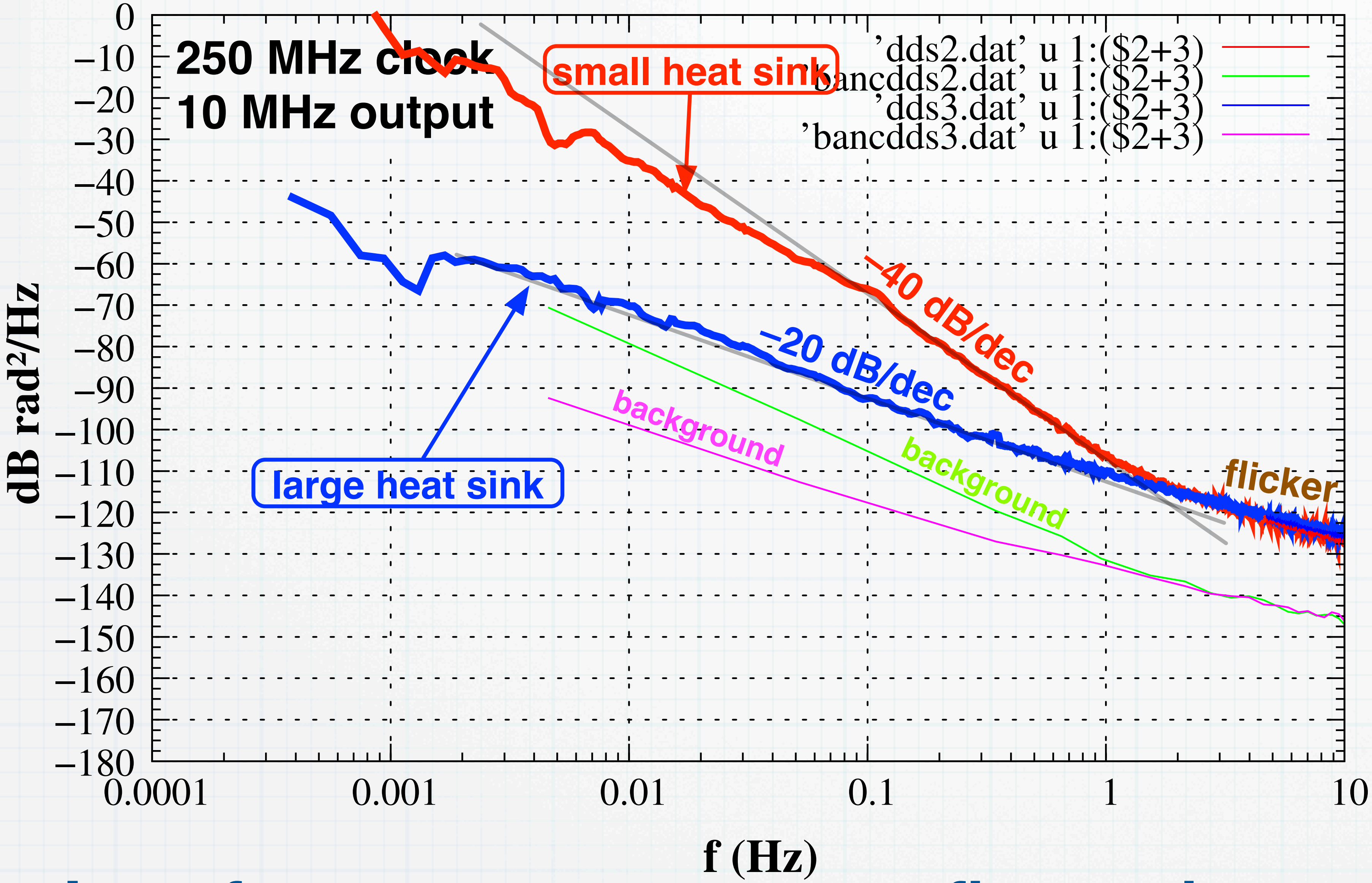
PM noise vs. clock amplitude

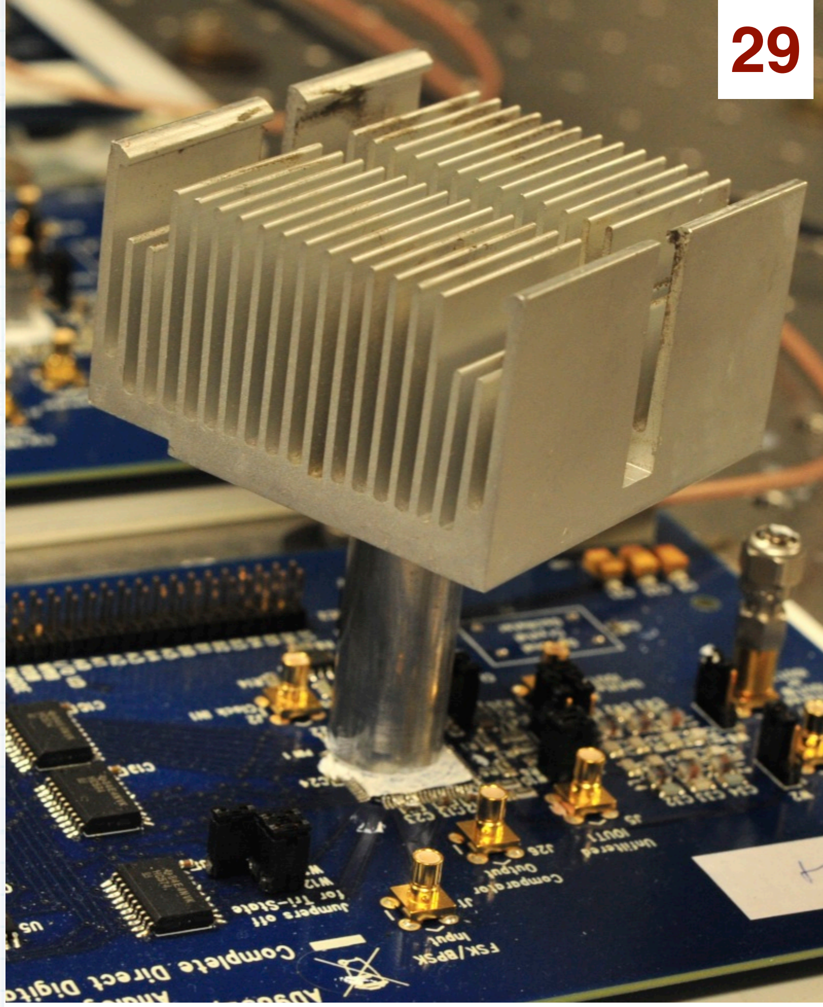


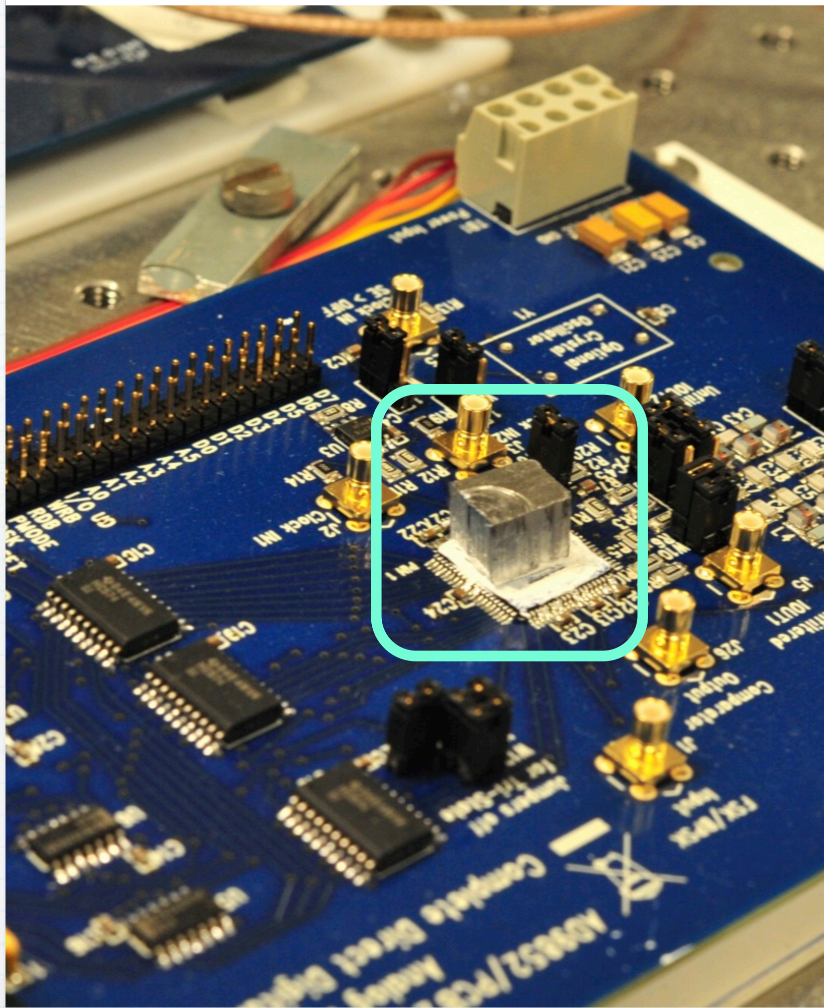
The effect of the clock frequency



Thermal effects

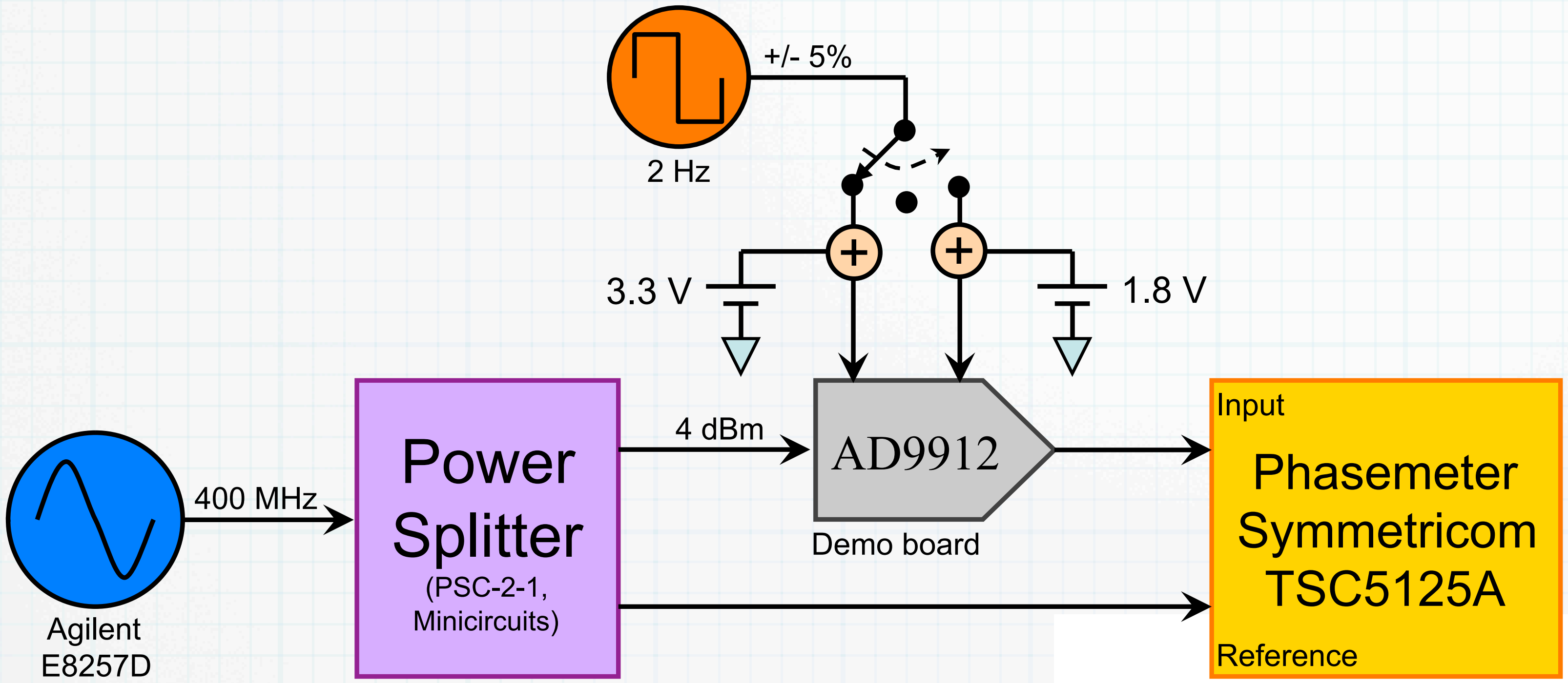


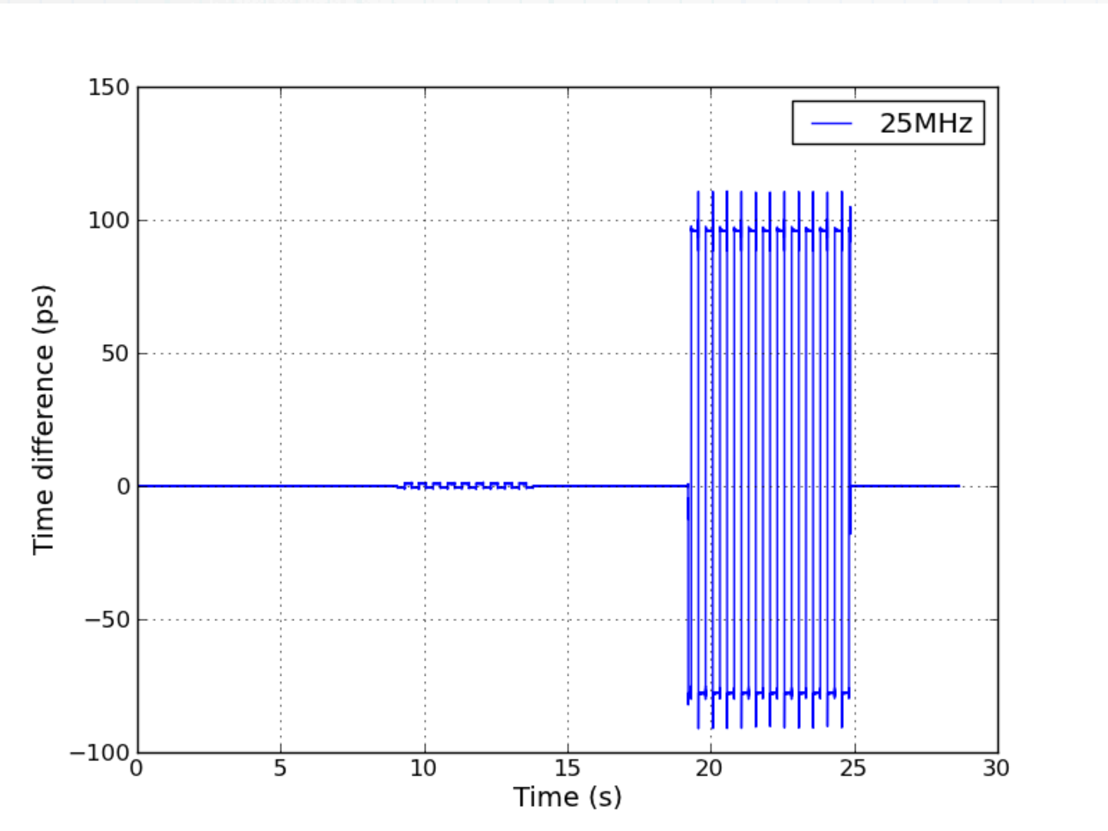


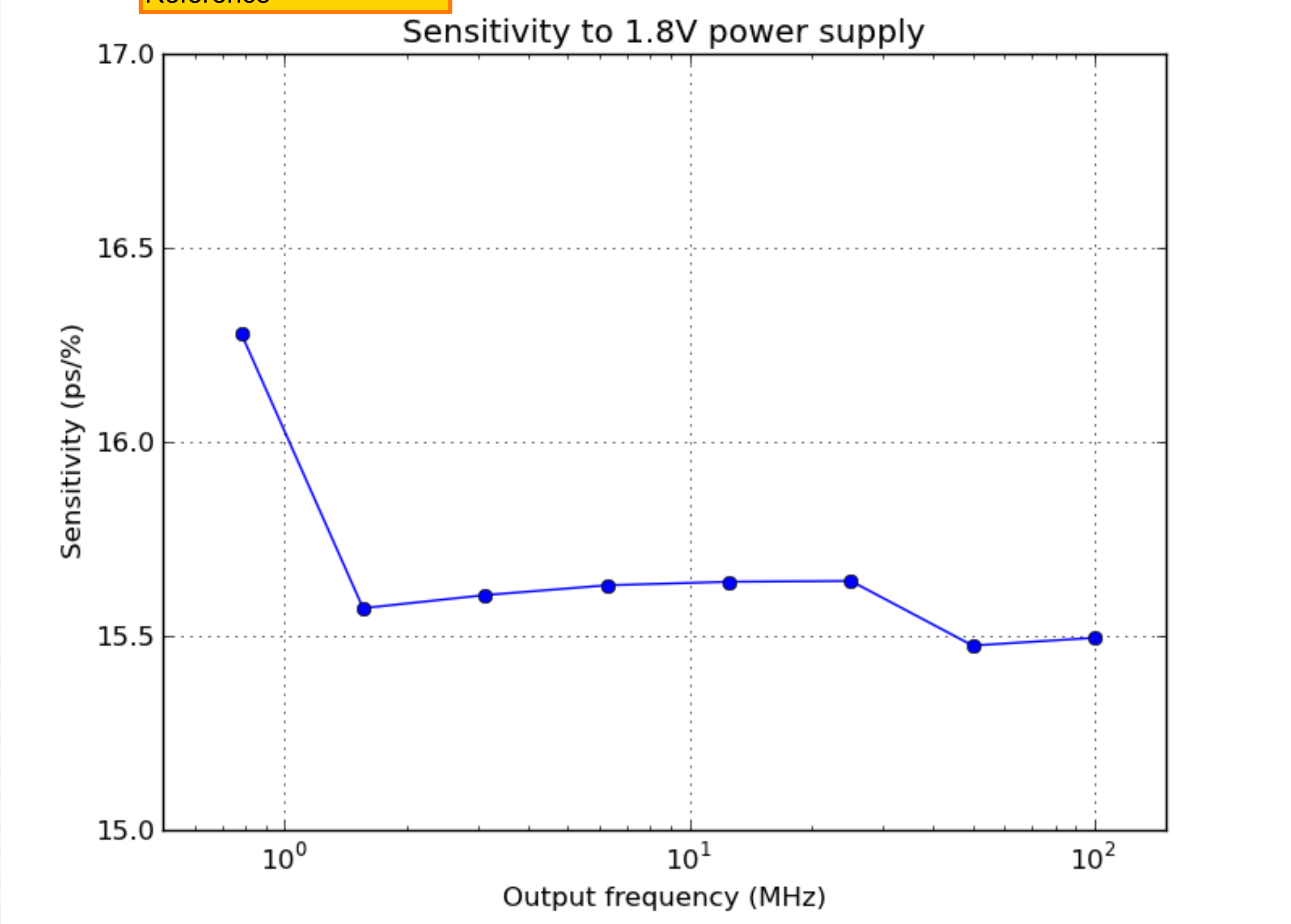


- Low-frequency temperature fluctuations induce phase noise
- A large thermal mass helps

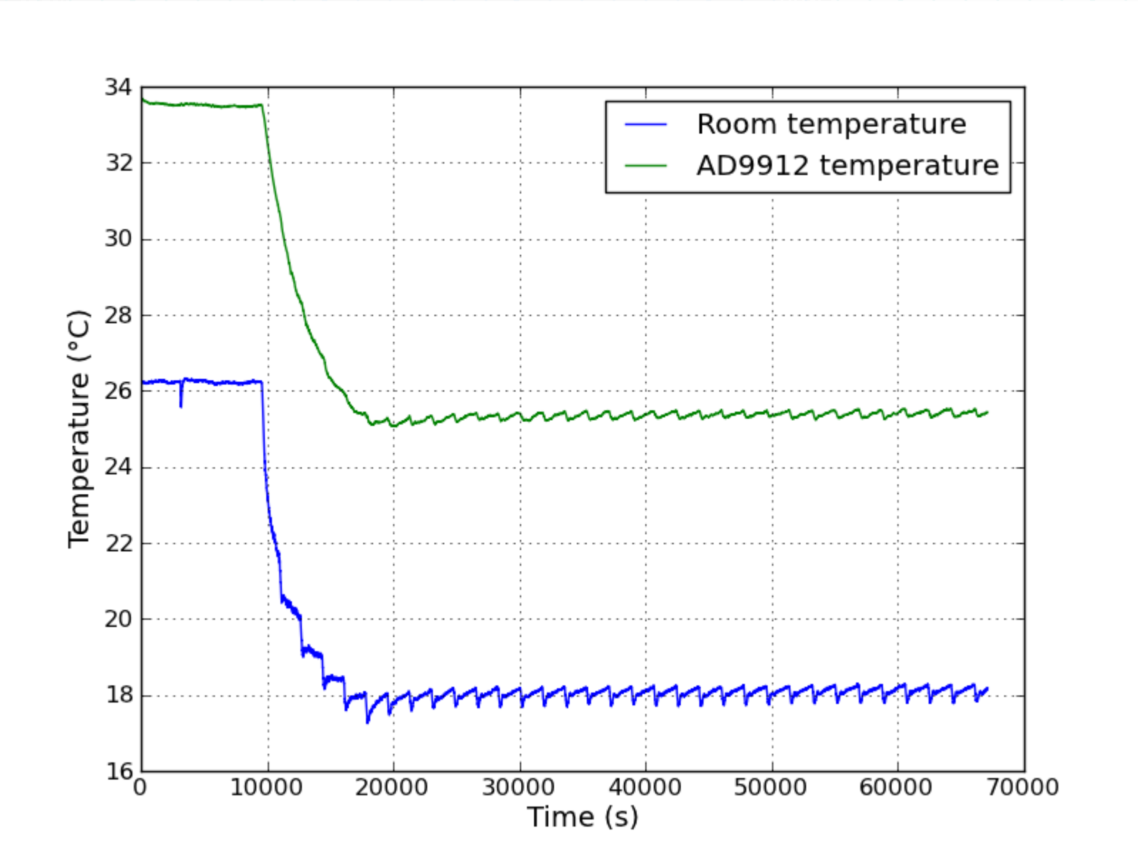
AD9912 Voltage sensitivity

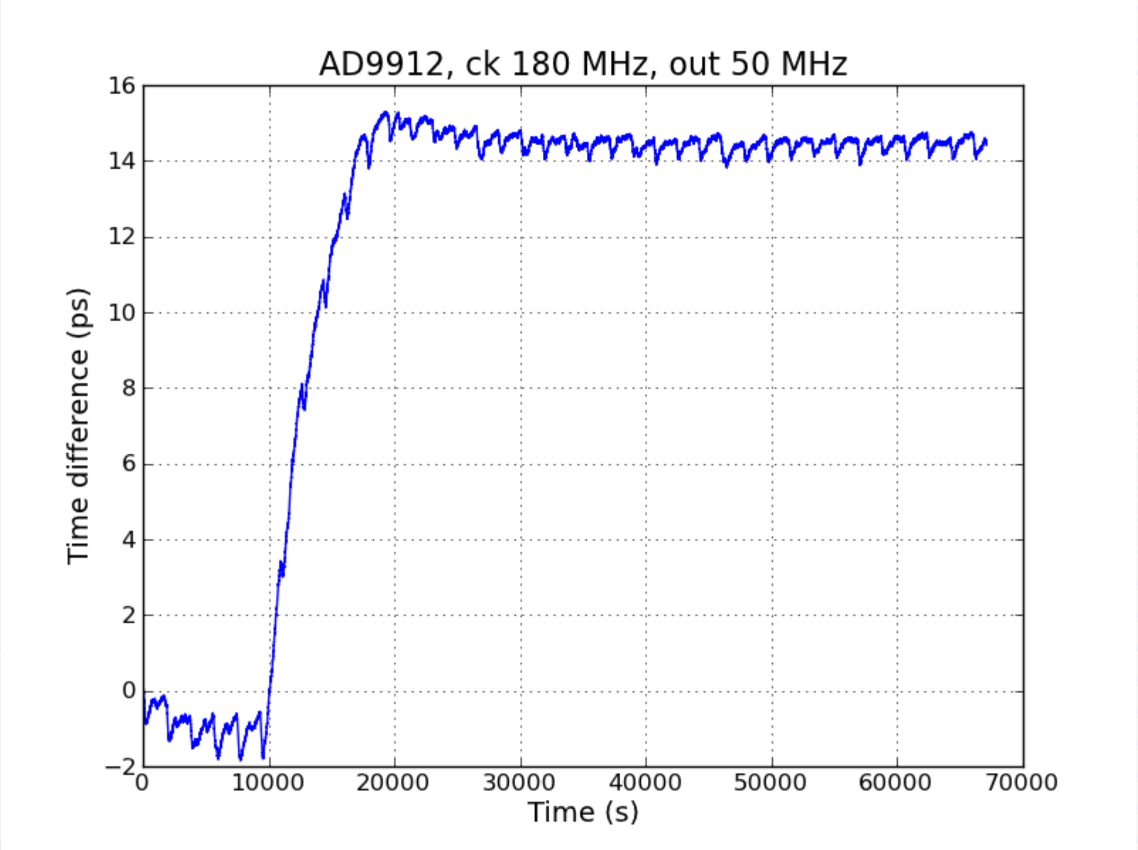






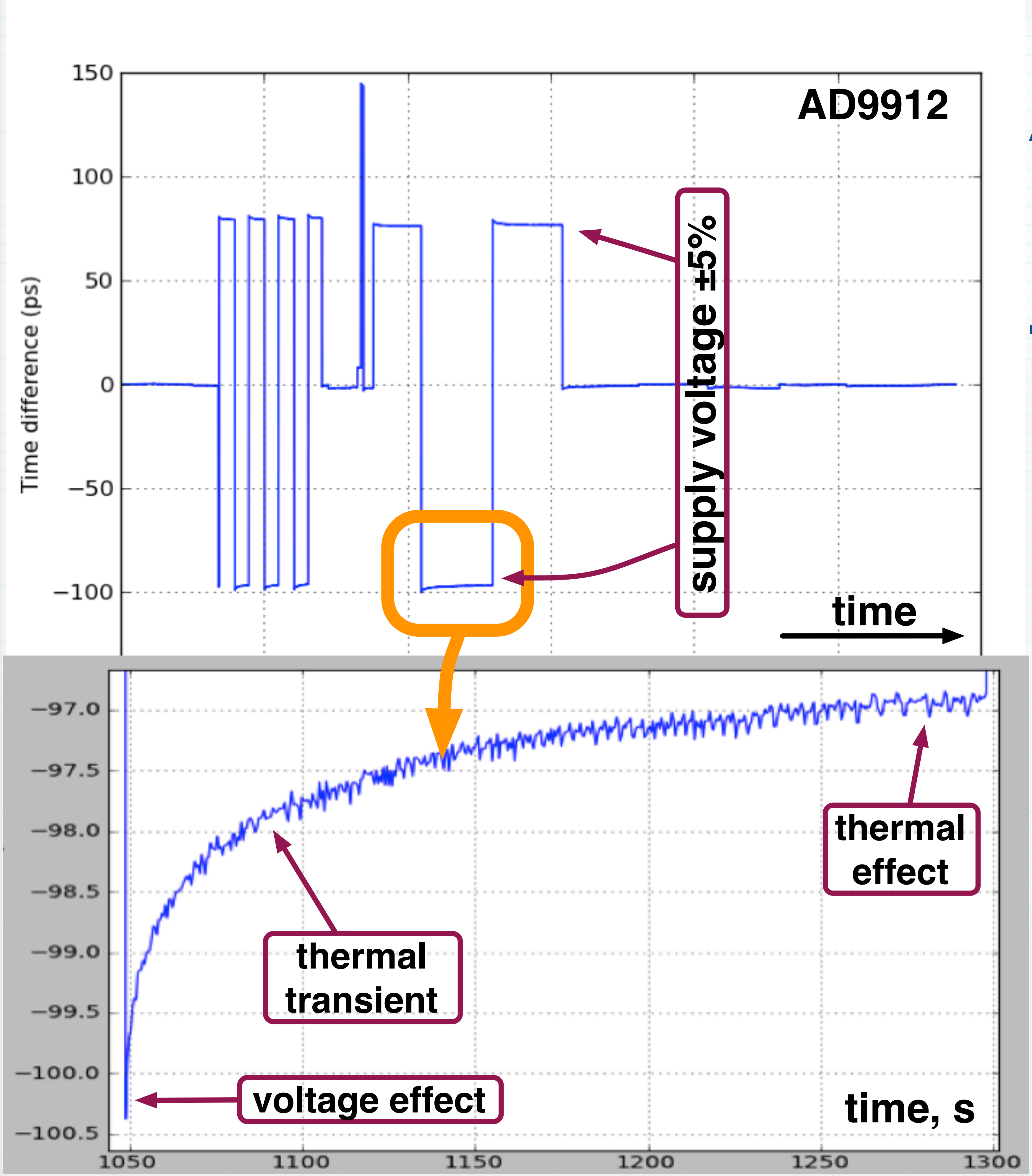
AD9912 temperature sensitivity



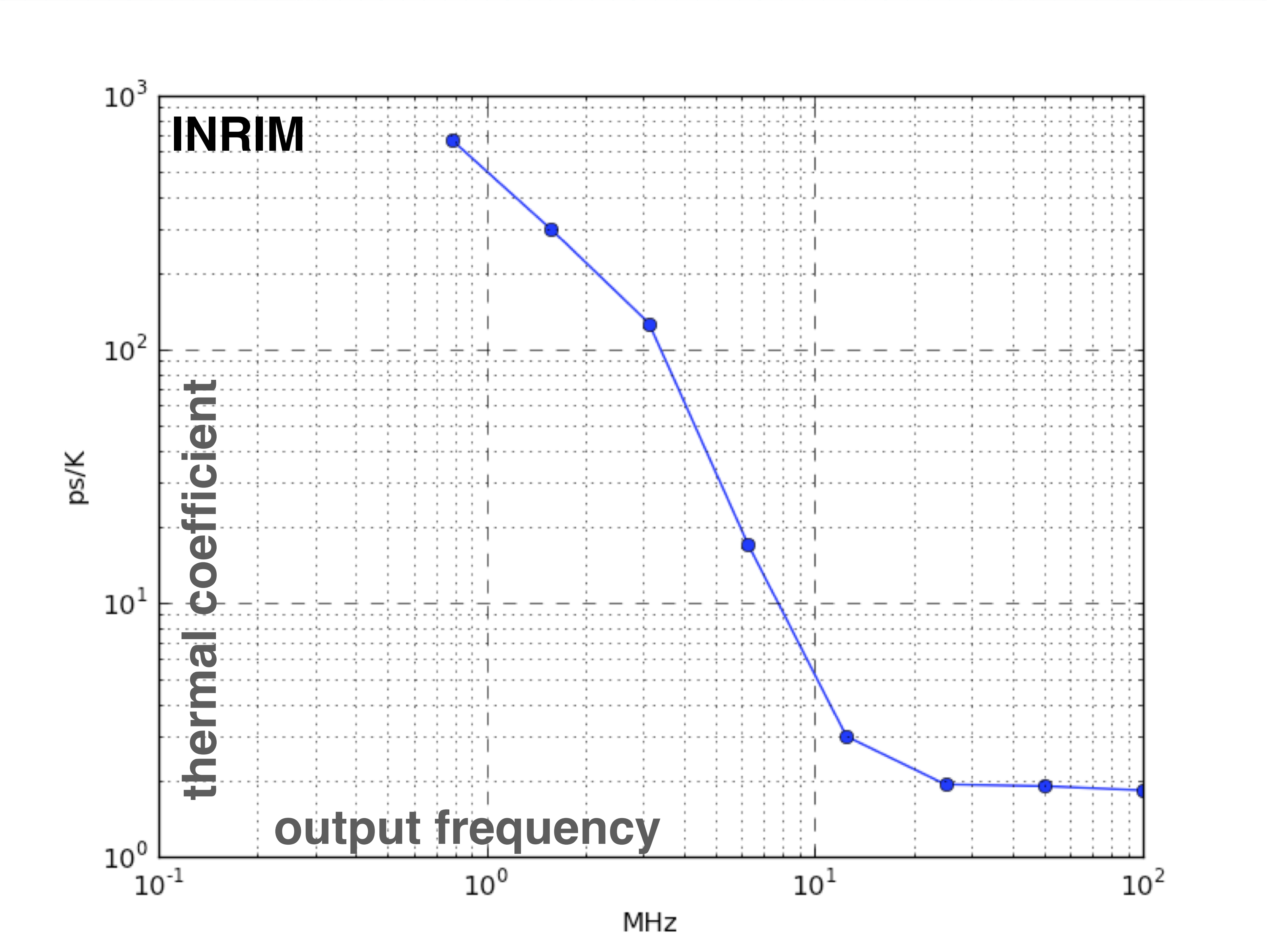


- **Temperature control (chamber)**
- **Measured: –2 ps/K**
- **Includes cables, baluns etc**

AD9912 sensitivity to temperature (alternate)



AD9912 temperature sensitivity



- **High frequency: –2 ps/K, constant**
- **Low frequency: $1/\nu^3$ law**

PM noise of the AD 9912

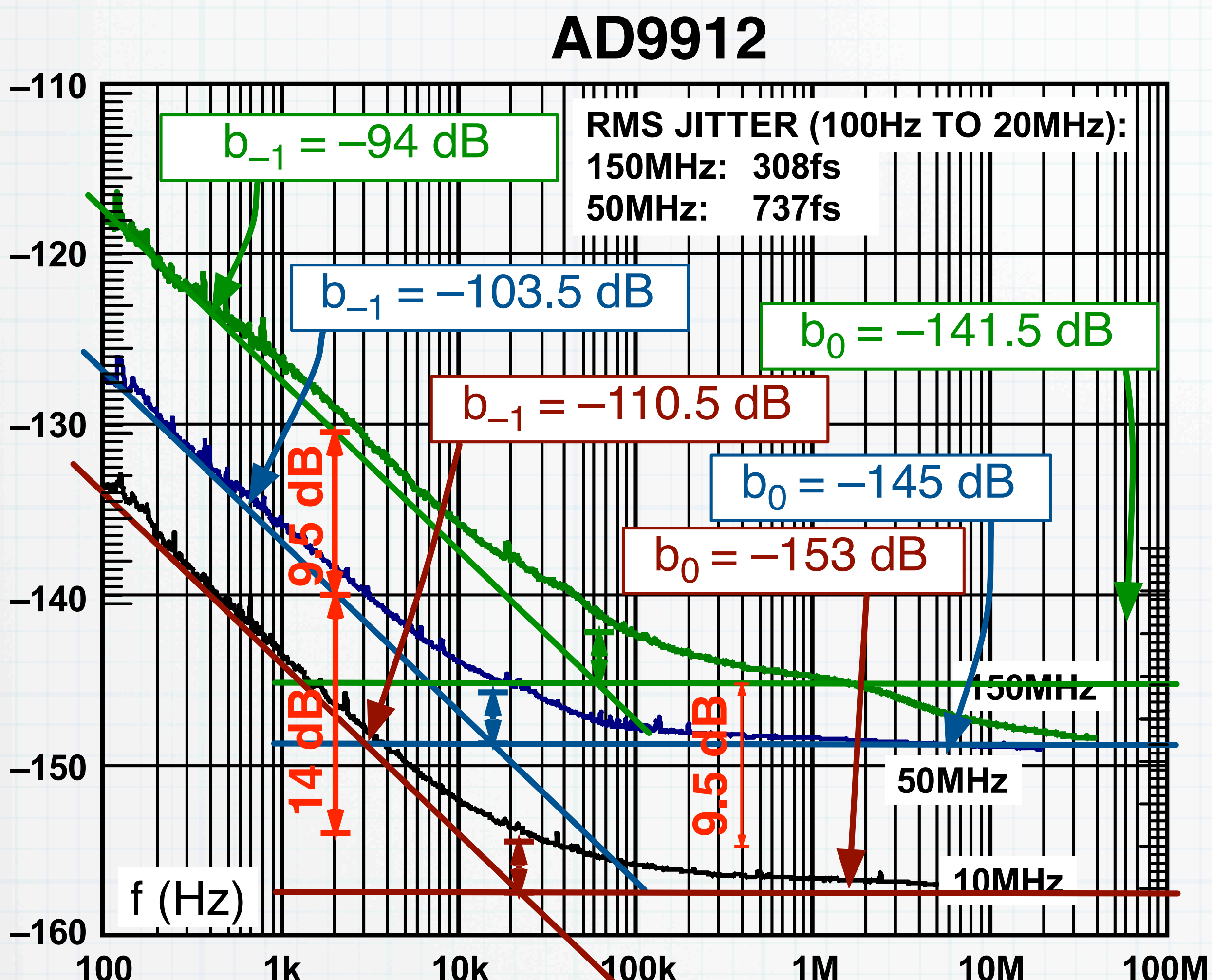
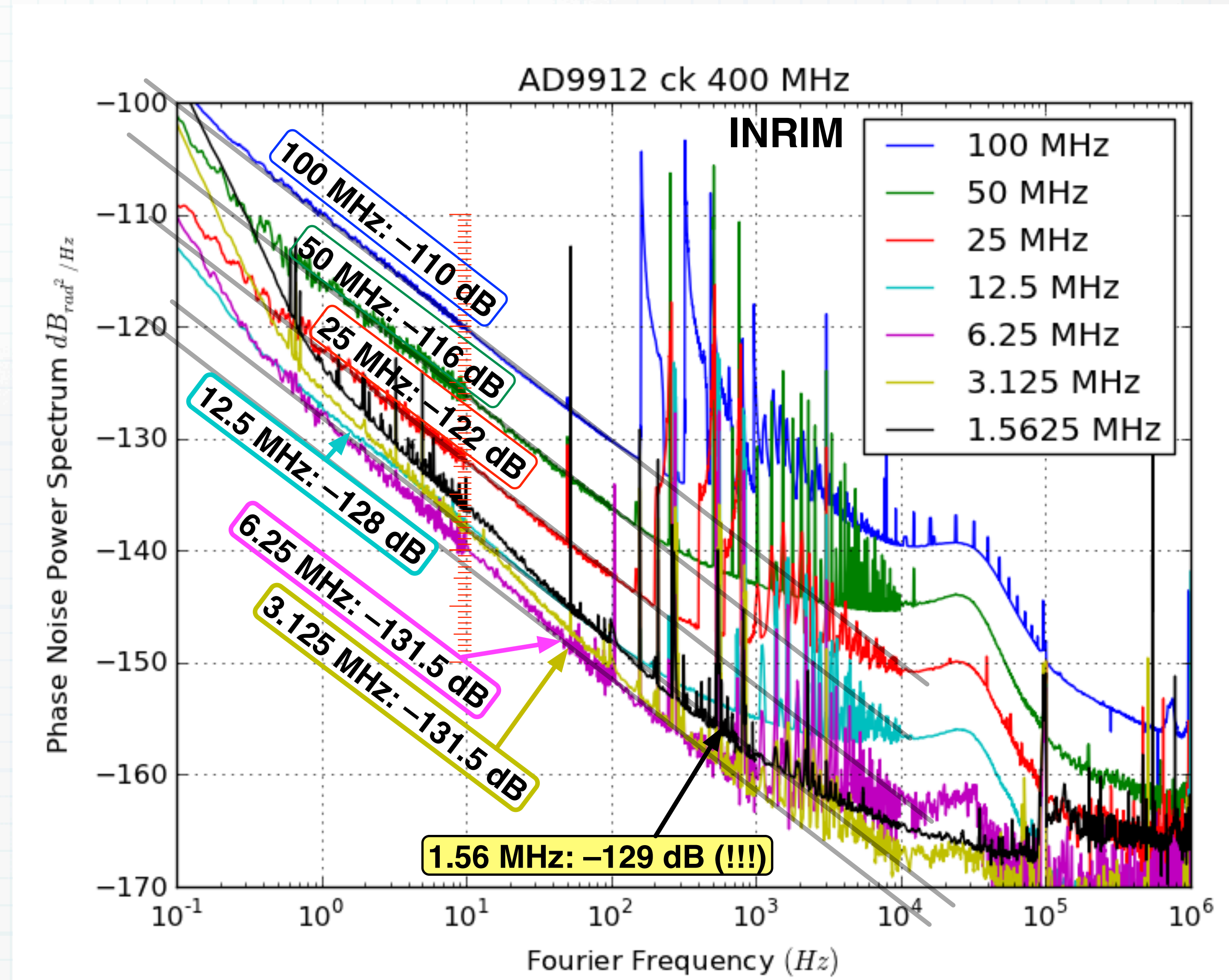
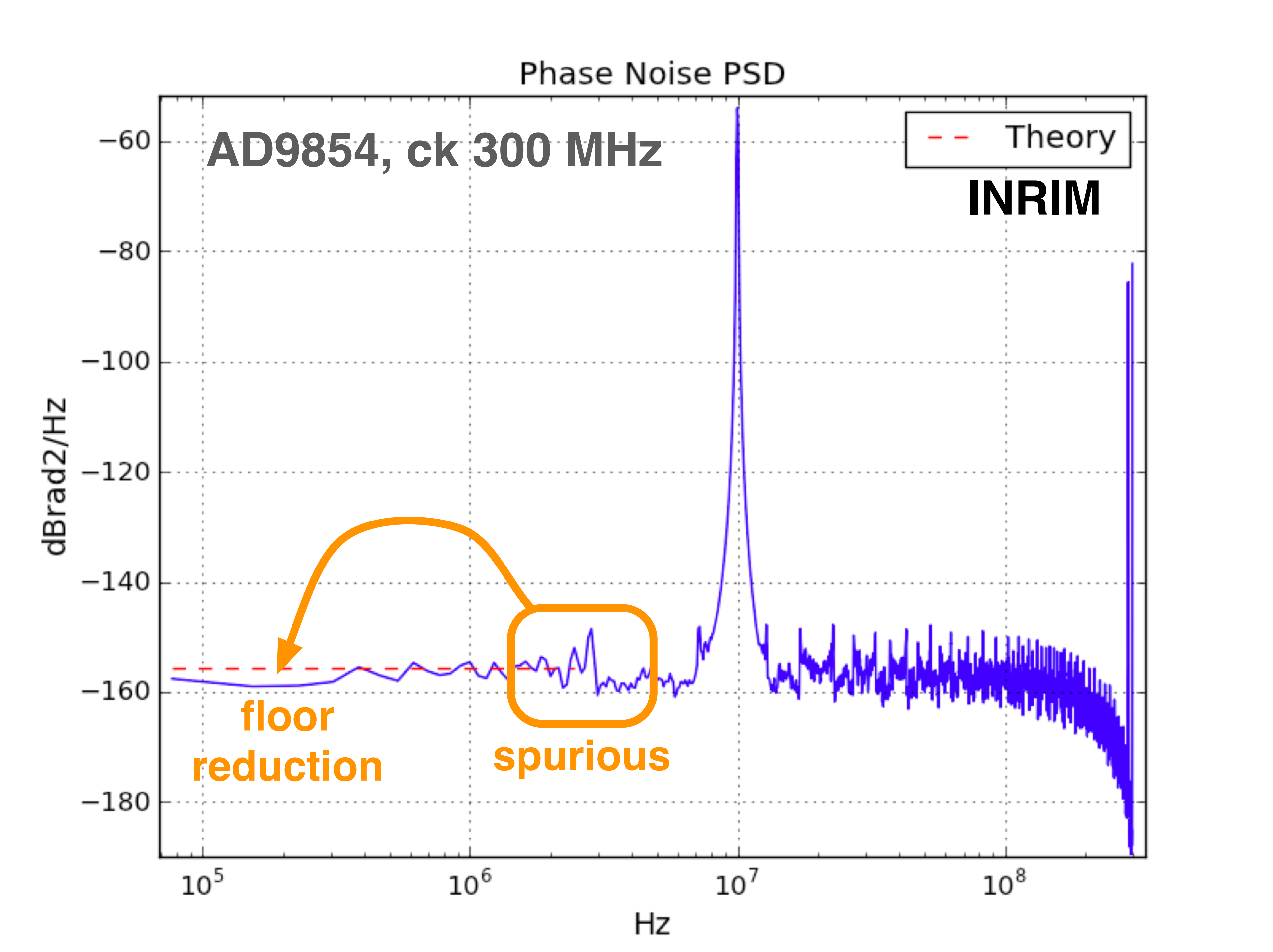


Figure 16. Absolute Phase Noise Using CMOS Driver at 3.3 V, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed) DDS Run at 200 MSPS for 10 MHz

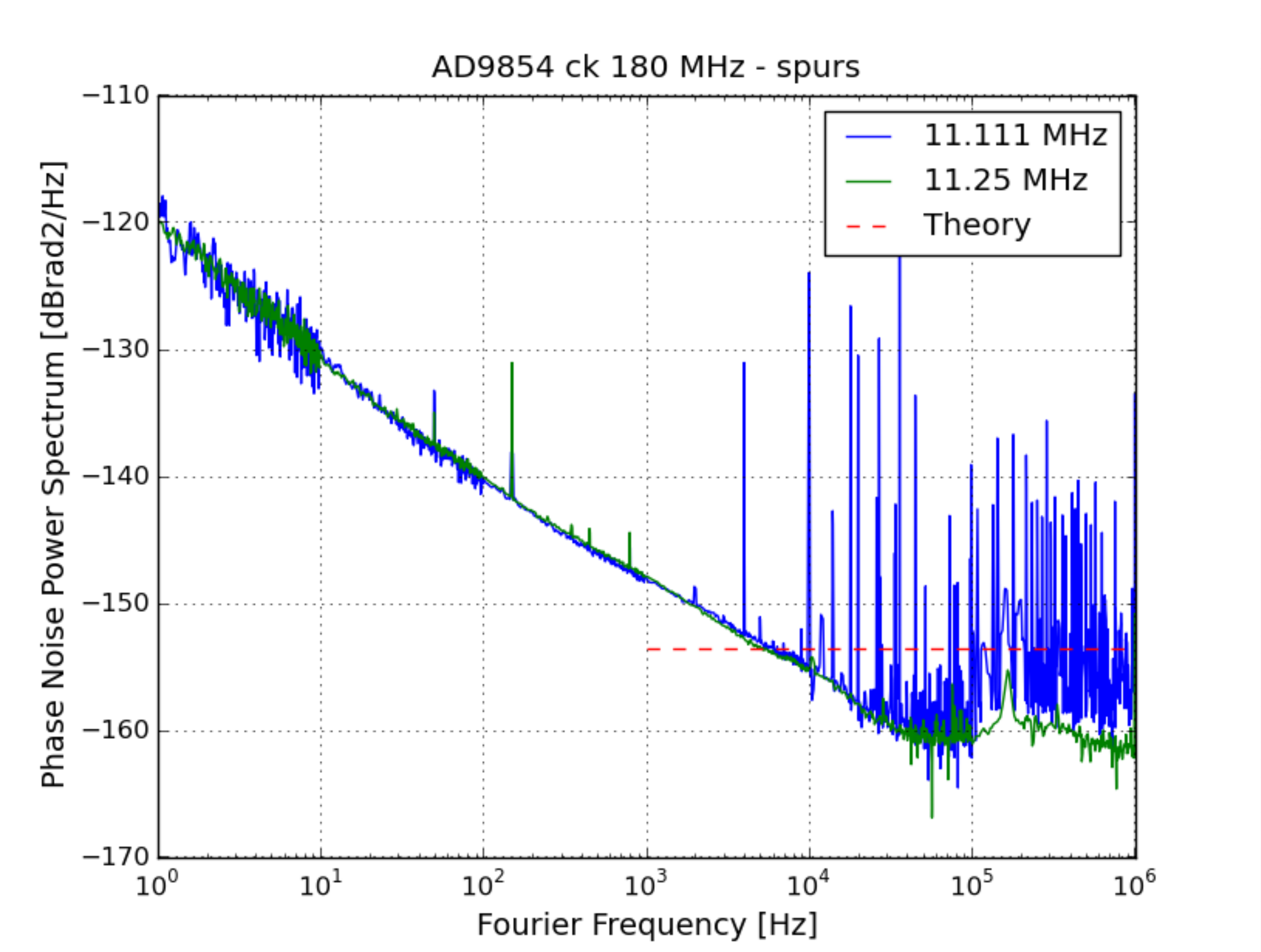


- **At 50 MHz and 10/12.5 MHz we get ≈15 dB lower flicker than the data-sheet spectrum**
- **Experimental conditions unclear in the data sheets**

Spurs reduce the white noise

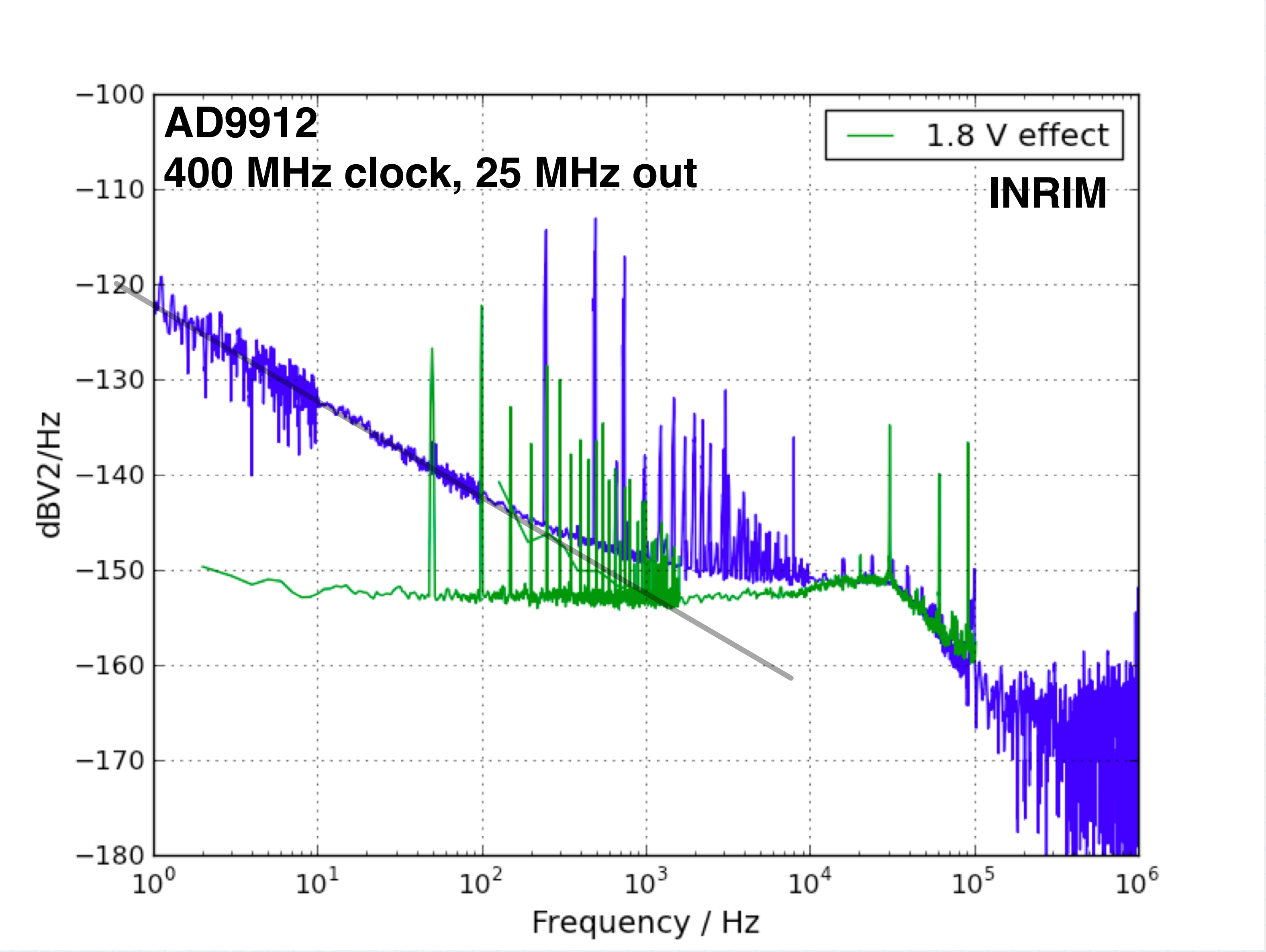


Spurs can be amazing



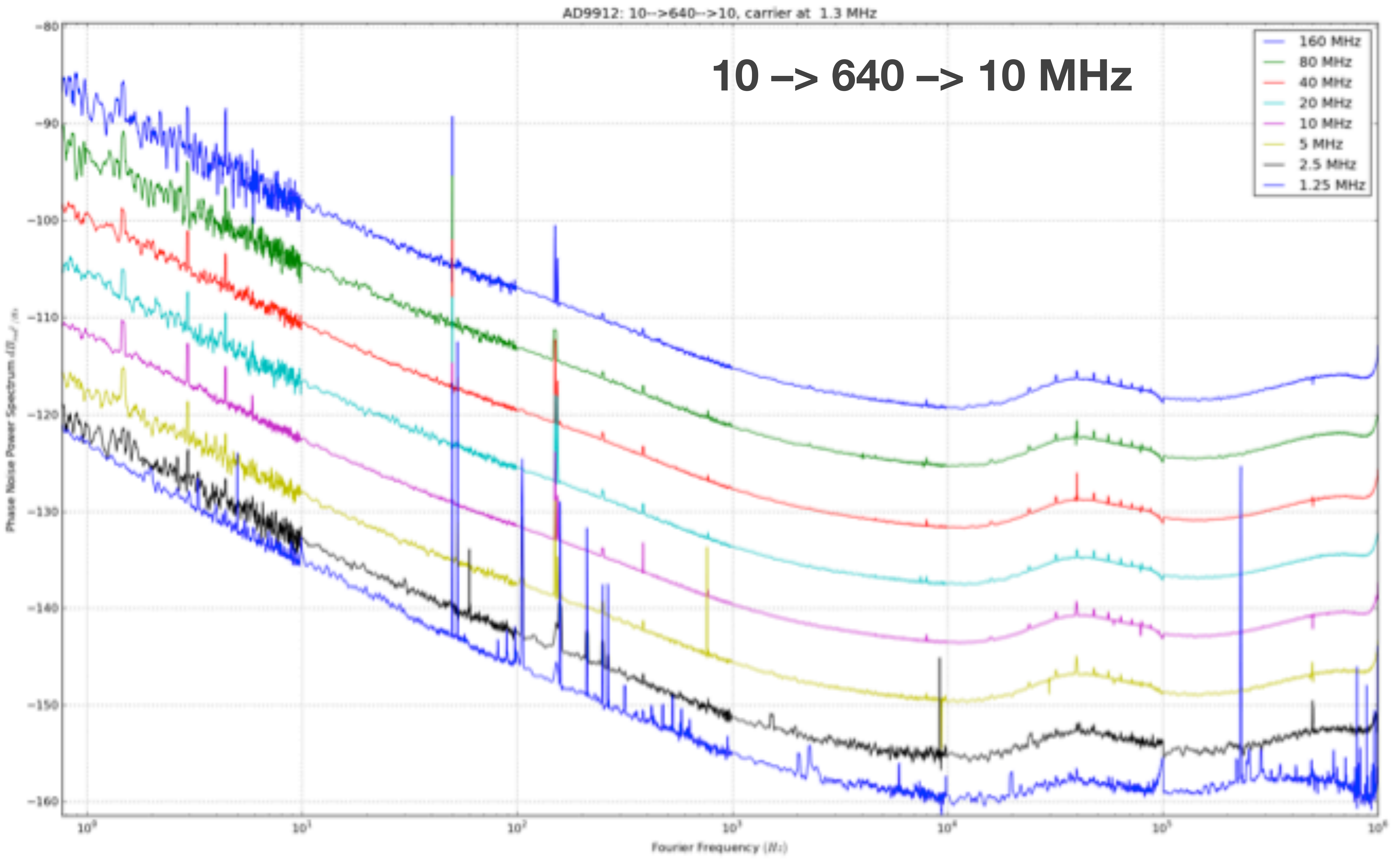
More about a PM-noise bump

- Low PSRR (power-supply rejection ratio) of PM noise
- For instance The AD9912 at 25 MHz out has 15 ps/% supply-voltage sensitivity
- No bump at 10^3–10^5 Hz is seen in the data-sheet spectra
- DC regulator may show a similar bump, alone or or with the output capacitor

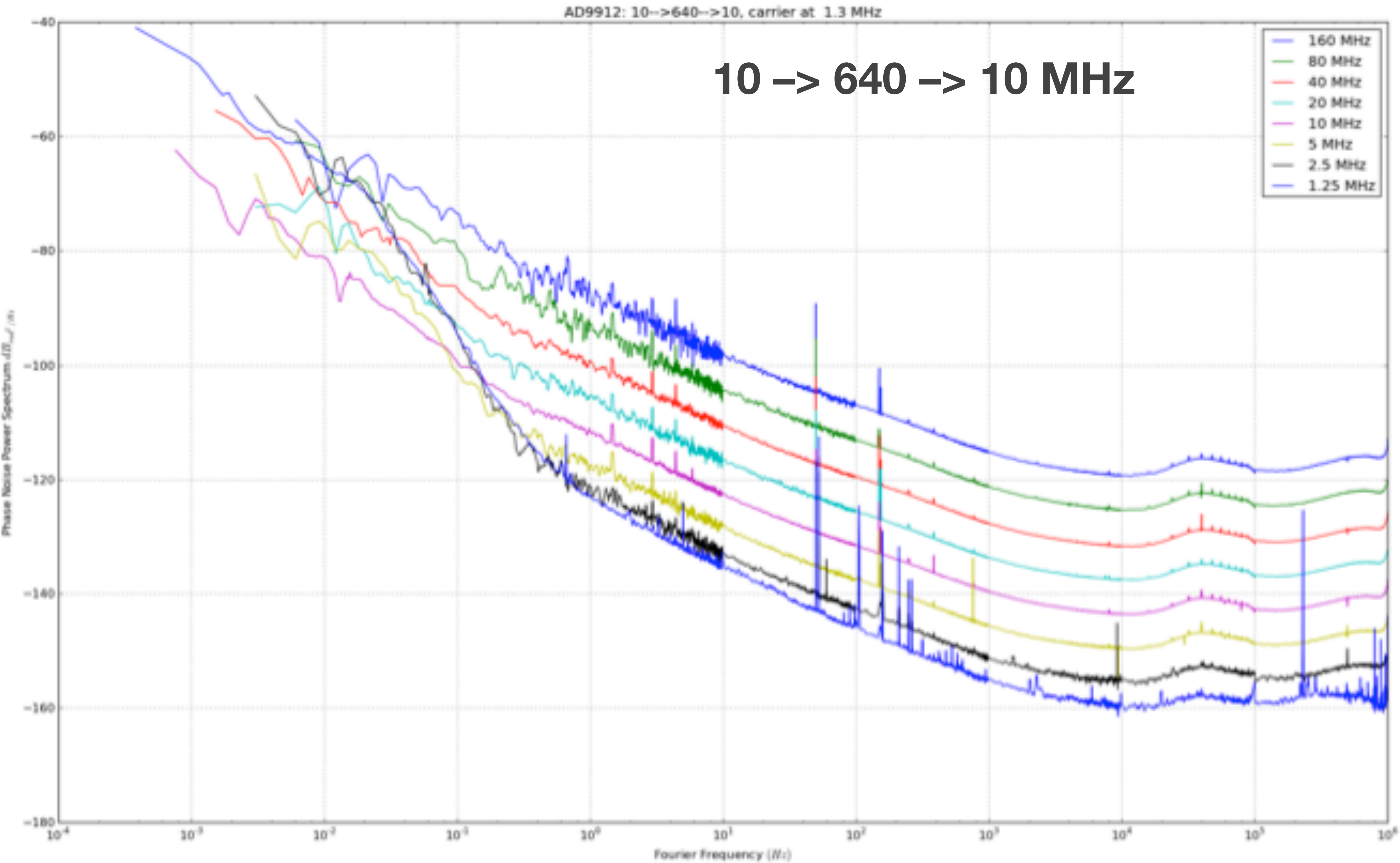


X7R SMD capacitor shows low ESR (≤5 mΩ)

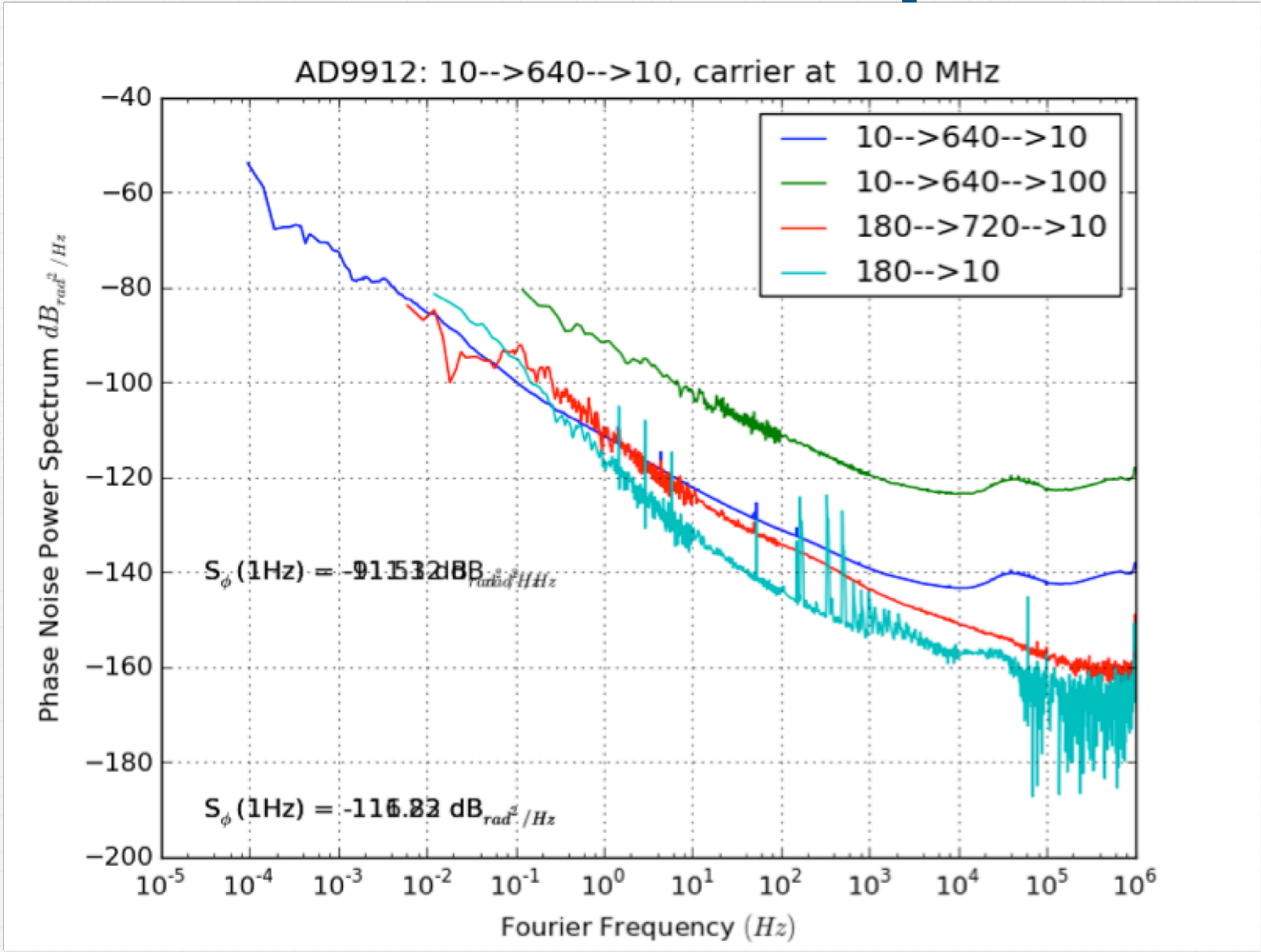
PLL clock multiplier



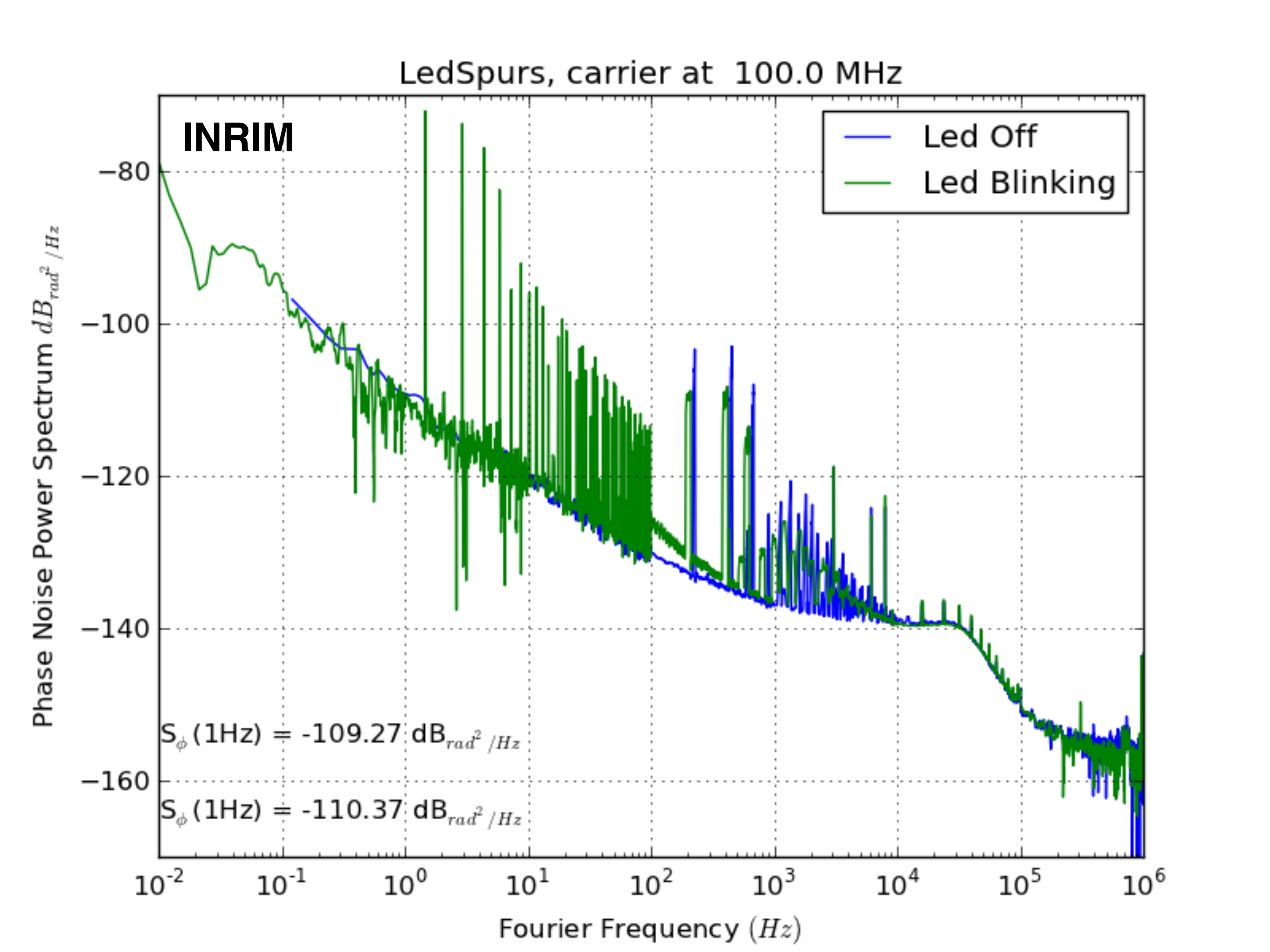
PLL clock multiplier



PLL clock multiplier

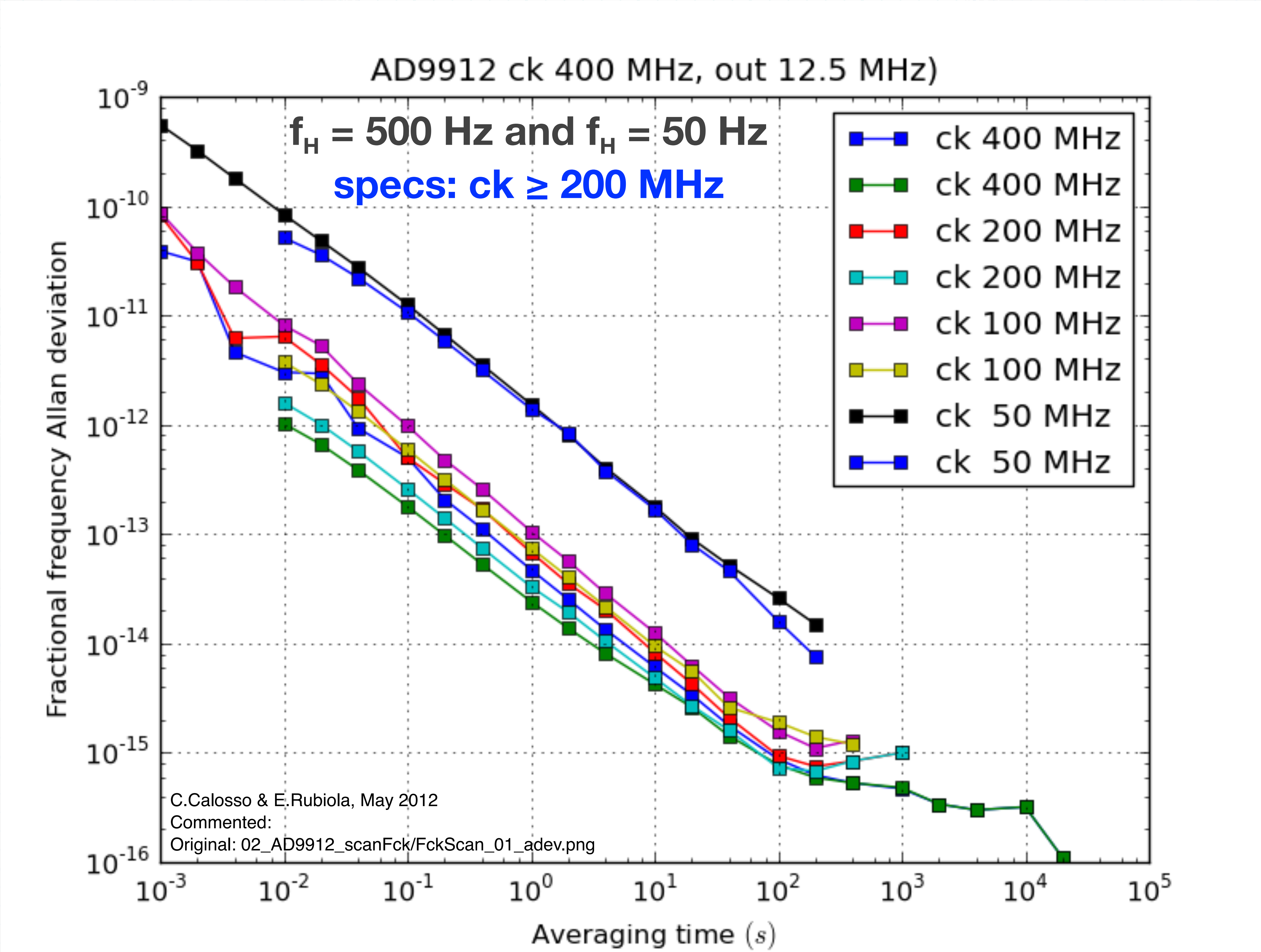


Effect of other parts on the PCB

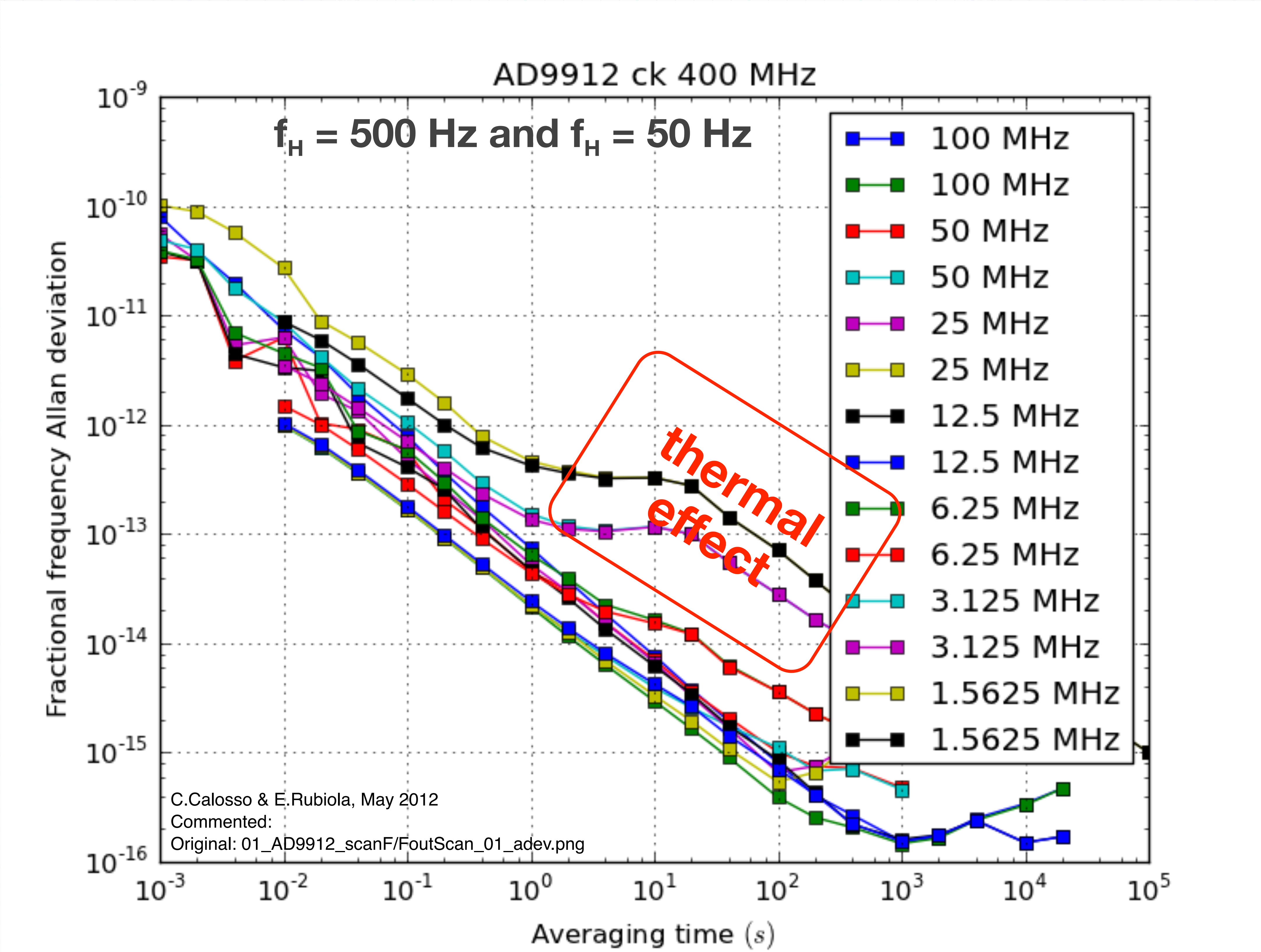


A blinking LED somewhere on the PCB spoils the output spectrum

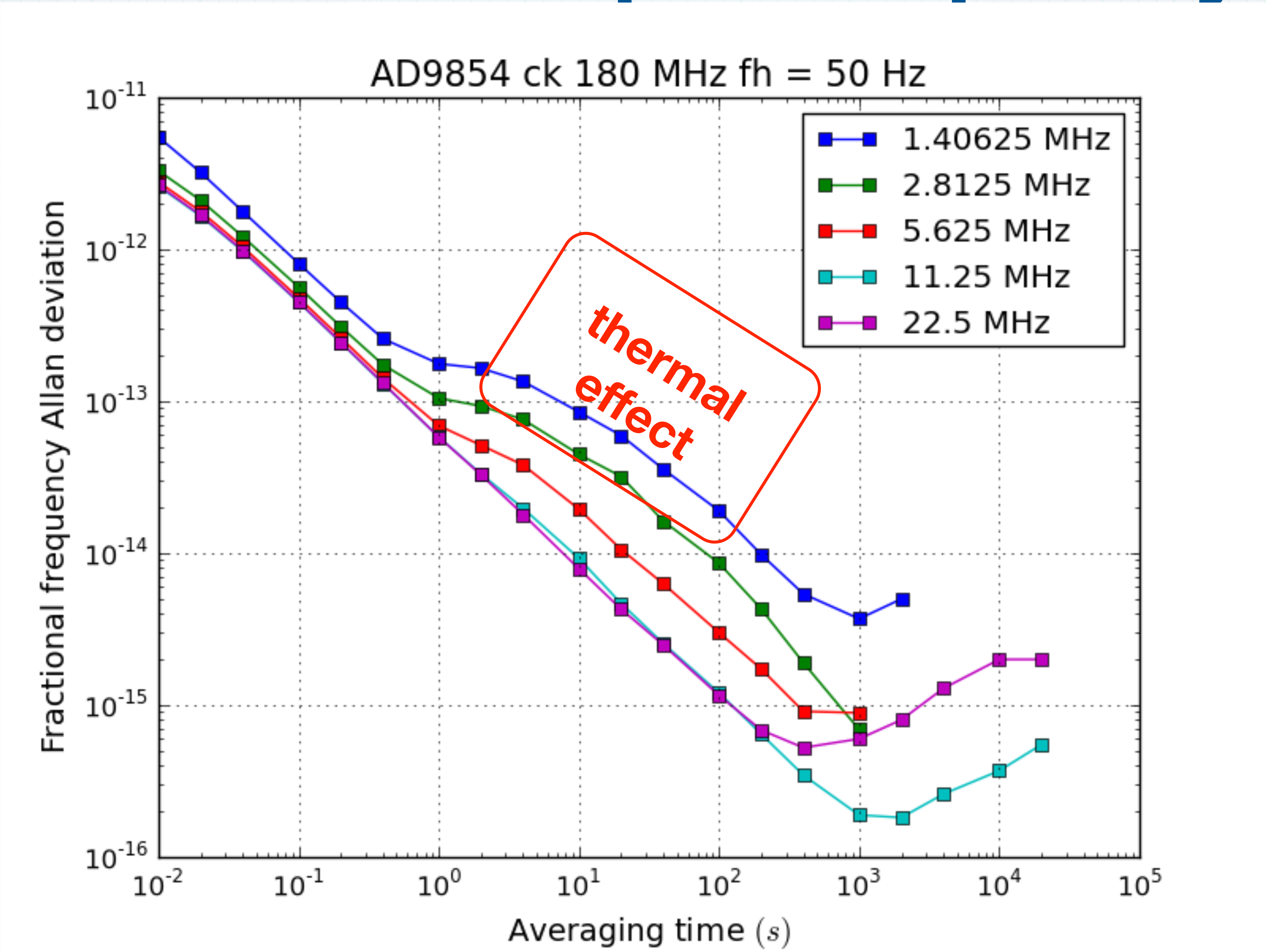
ADEV vs. clock frequency



ADEV vs. output frequency

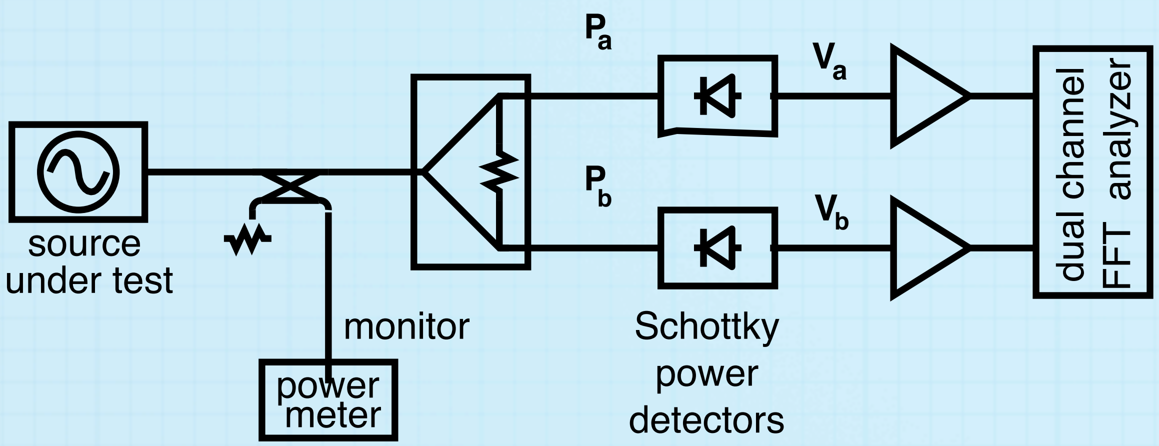


ADEV vs. output frequency



Experimental method (AM noise)

Cross-spectrum



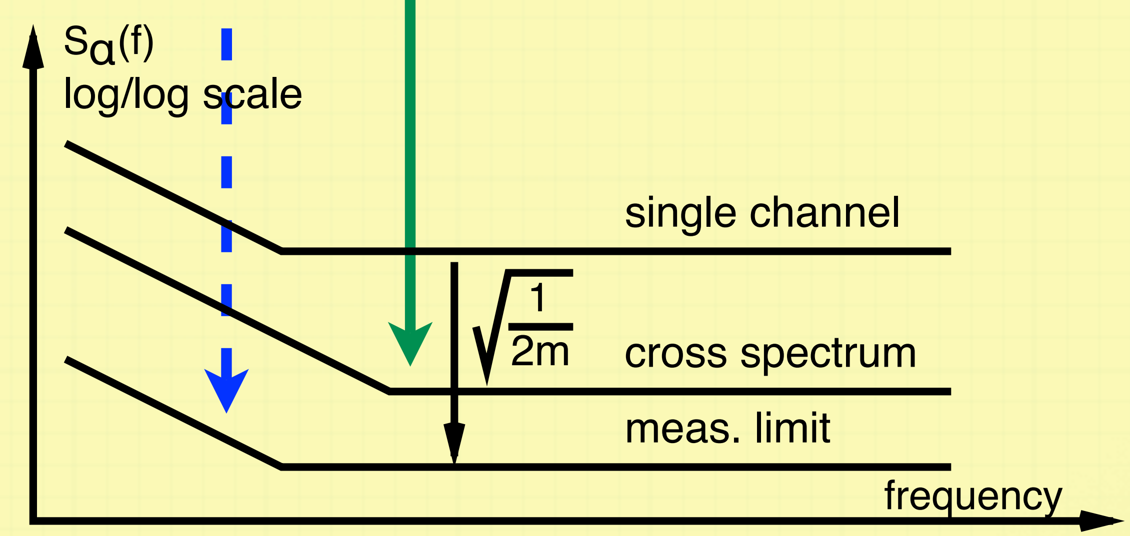
$$v_a(t) = 2k_a P_a \alpha(t) + \text{noise}$$
$$v_b(t) = 2k_a P_b \alpha(t) + \text{noise}$$

The cross spectrum $S_{ba}(f)$ rejects the single-channel noise because the two channels are independent.

$$S_{ba}(f) = \frac{1}{4k_a k_b P_a P_b} S_\alpha(f)$$

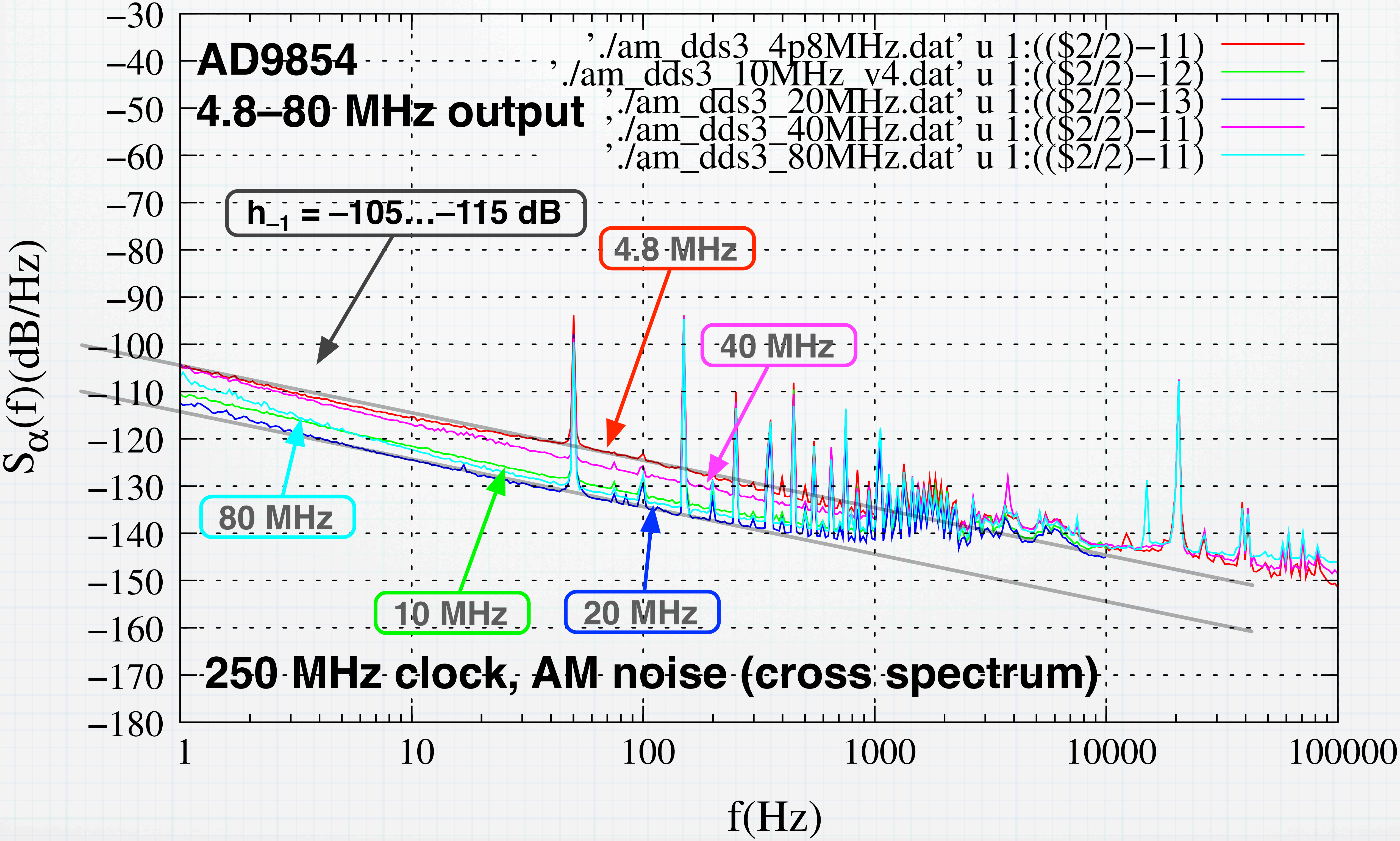
- **Averaging on m spectra, the single-channel noise is rejected by $\sqrt{1/2m}$**

- **A cross-spectrum higher than the averaging limit validates the measure**

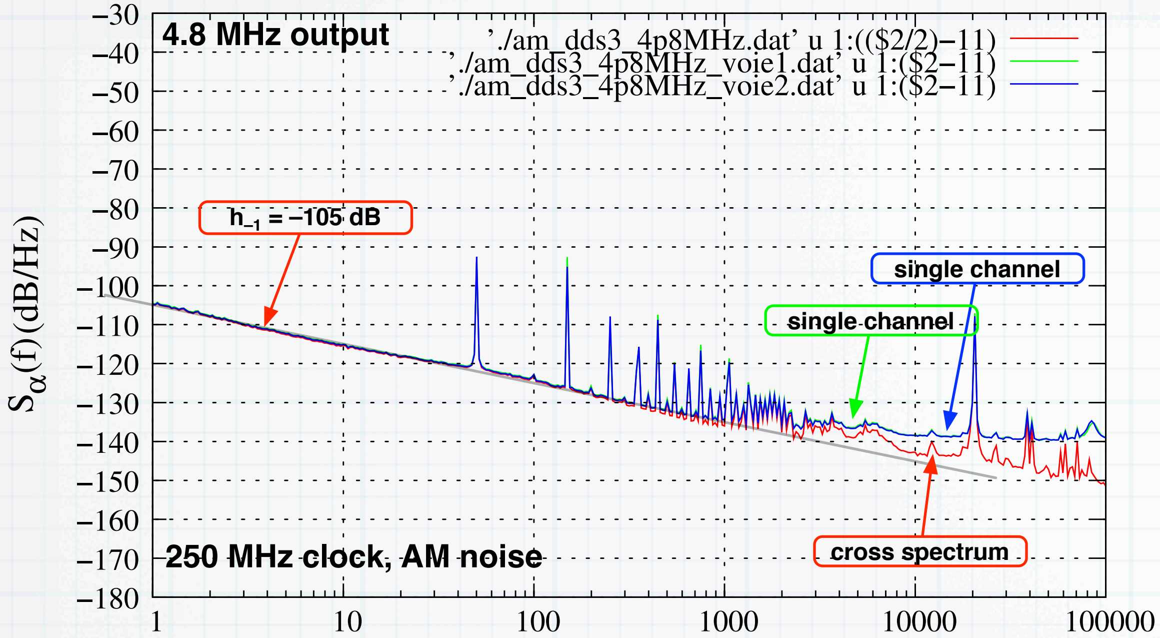


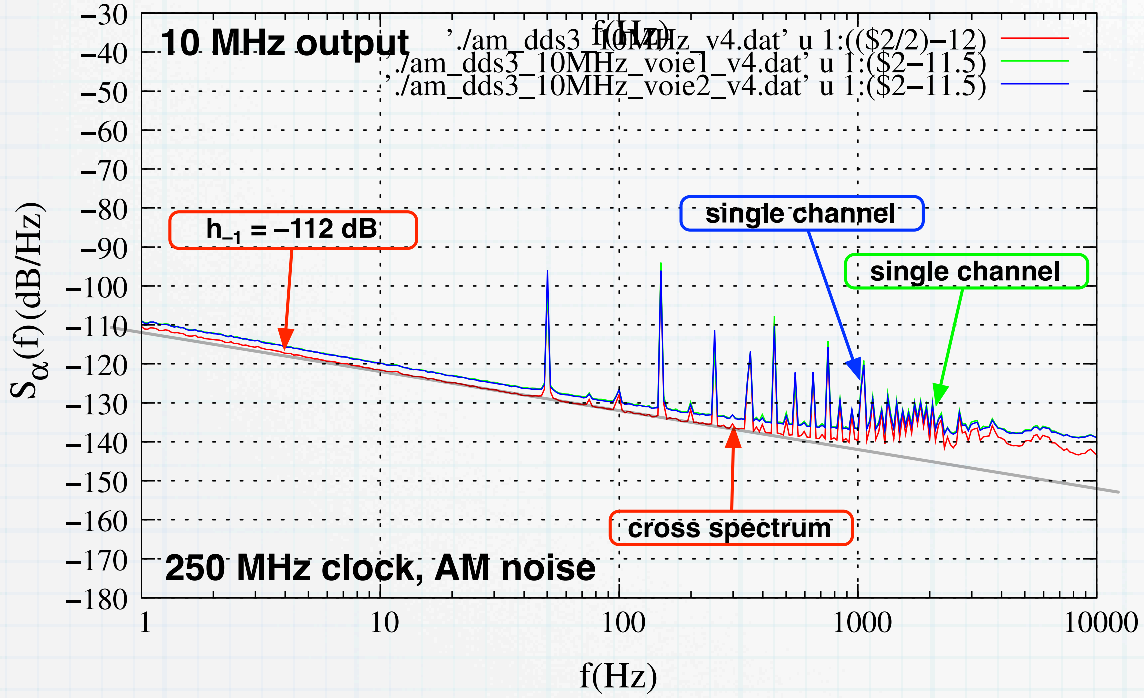
E. Rubiola, The measurement of AM noise of oscillators, arXiv:physics/0512082, Dec. 2005
E. Rubiola, F. Vernotte, The cross-spectrum experimental method, arXiv:1003.0113v1 [physics.ins-det], Feb. 2010

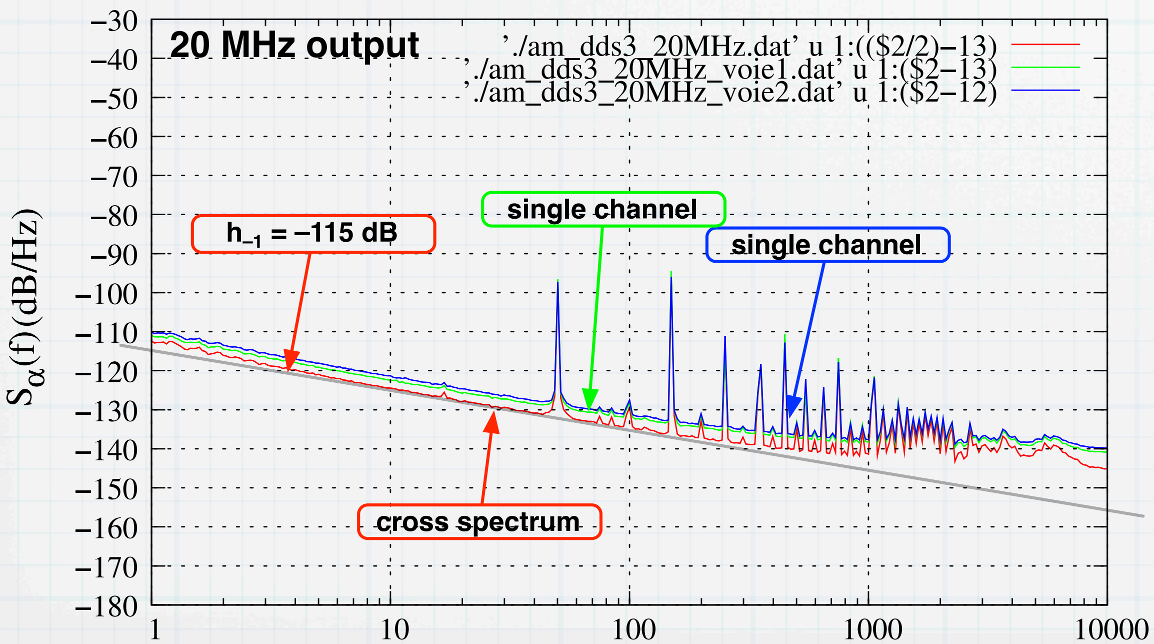
AM noise (1)

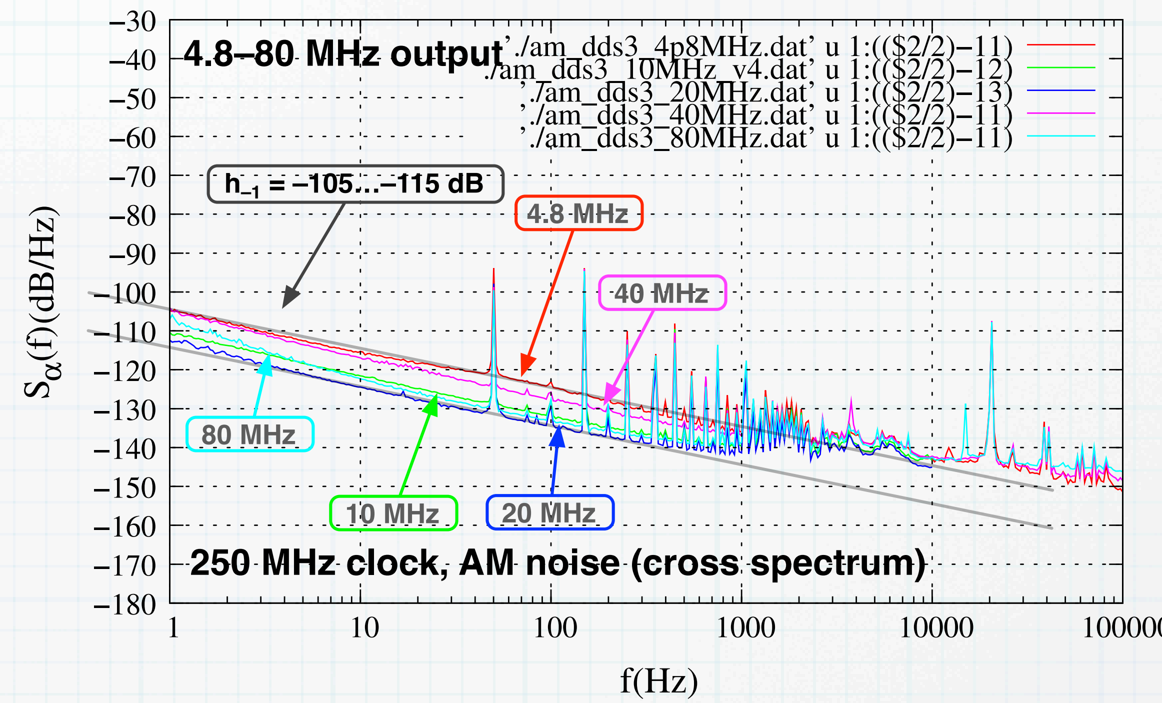

AD9854
4.8–80 MHz output
'./am_dds3_4p8MHz.dat' u 1:(($2/2)−11)
'./am_dds3_10MHz_v4.dat' u 1:(($2/2)−12)
'./am_dds3_20MHz.dat' u 1:(($2/2)−13)
'./am_dds3_40MHz.dat' u 1:(($2/2)−11)
'./am_dds3_80MHz.dat' u 1:(($2/2)−11)
h_-1 = −105…−115 dB
4.8 MHz
40 MHz
80 MHz
10 MHz
20 MHz
250 MHz clock, AM noise (cross spectrum)
Sα(f)(dB/Hz)
f(Hz)
−30
−40
−50
−60
−70
−80
−90
−100
−110
−120
−130
−140
−150
−160
−170
−180
1
10
100
1000
10000
100000

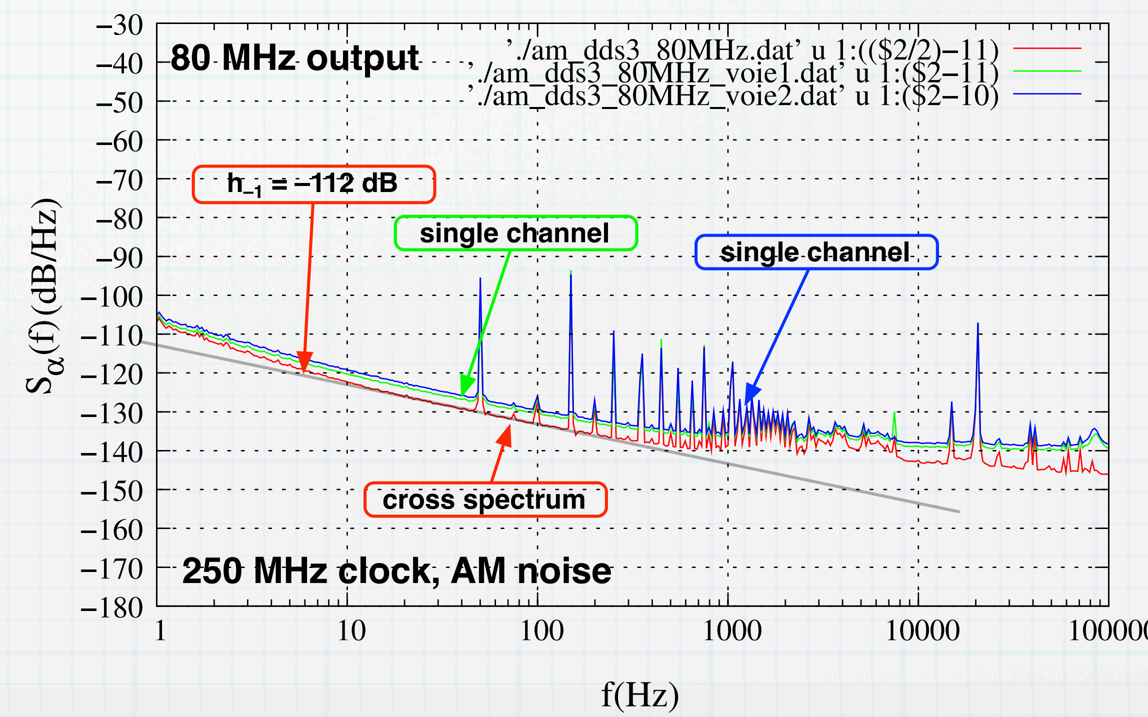
AM noise (2)


4.8 MHz output
'./am_dds3_4p8MHz.dat' u 1:(($2/2)−11)
'./am_dds3_4p8MHz_voie1.dat' u 1:($2−11)
'./am_dds3_4p8MHz_voie2.dat' u 1:($2−11)
h_-1 = −105 dB
single channel
single channel
cross spectrum
250 MHz clock, AM noise
Sα(f) (dB/Hz)
f(Hz)
−30 −40 −50 −60 −70 −80 −90 −100 −110 −120 −130 −140 −150 −160 −170 −180
1 10 100 1000 10000 100000


10 MHz output
'./am_dds3_10MHz_v4.dat' u 1:(($2/2)−12)
'./am_dds3_10MHz_voie1_v4.dat' u 1:($2−11.5)
'./am_dds3_10MHz_voie2_v4.dat' u 1:($2−11.5)
h_-1 = −112 dB
single channel
single channel
cross spectrum
250 MHz clock, AM noise
Sα(f) (dB/Hz)
f(Hz)
−30 −40 −50 −60 −70 −80 −90 −100 −110 −120 −130 −140 −150 −160 −170 −180
1 10 100 1000 10000


20 MHz output
'./am_dds3_20MHz.dat' u 1:(($2/2)−13)
'./am_dds3_20MHz_voie1.dat' u 1:($2−13)
'./am_dds3_20MHz_voie2.dat' u 1:($2−12)
h_-1 = −115 dB
single channel
single channel
cross spectrum
Sα(f) (dB/Hz)
−30 −40 −50 −60 −70 −80 −90 −100 −110 −120 −130 −140 −150 −160 −170 −180
1 10 100 1000 10000


4.8–80 MHz output
'./am_dds3_4p8MHz.dat' u 1:(($2/2)−11)
'./am_dds3_10MHz_v4.dat' u 1:(($2/2)−12)
'./am_dds3_20MHz.dat' u 1:(($2/2)−13)
'./am_dds3_40MHz.dat' u 1:(($2/2)−11)
'./am_dds3_80MHz.dat' u 1:(($2/2)−11)
h_-1 = −105...−115 dB
4.8 MHz
40 MHz
80 MHz
10 MHz
20 MHz
250 MHz clock, AM noise (cross spectrum)
Sα(f) (dB/Hz)
f(Hz)
−30 −40 −50 −60 −70 −80 −90 −100 −110 −120 −130 −140 −150 −160 −170 −180
1 10 100 1000 10000 100000


80 MHz output
'./am_dds3_80MHz.dat' u 1:(($2/2)−11)
'./am_dds3_80MHz_voie1.dat' u 1:($2−11)
'./am_dds3_80MHz_voie2.dat' u 1:($2−10)
h_-1 = −112 dB
single channel
single channel
cross spectrum
250 MHz clock, AM noise
Sα(f) (dB/Hz)
f(Hz)
−30 −40 −50 −60 −70 −80 −90 −100 −110 −120 −130 −140 −150 −160 −170 −180
1 10 100 1000 10000 100000

Conclusions

- Noise theory and model for the DDS
- A lot of still-not-published experimental data
  - Phase noise
  - Allan deviation
  - Amplitude noise
- Experiments done at INRIM and at FEMTO-ST
- Model and experimental data are in fair agreement

http://rubiola.org