A Fully-Digital Realtime SoC FPGA based Phase Noise Analyzer with Cross-Correlation

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***Abstract*—We report on a fully-digital and realtime operation of a phase noise analyzer using modern digital techniques with cross-correlation. With the advent of system on chip field-programmable gate arrays (SoC FPGAs) embedding hard core central processing unit, coprocessor and FPGA onto a single integrated circuit, the building of sensitive analysis devices for Time & Frequency research is made accessible at virtually no cost and benefits from reconfigurability. Used with high-speed digitizers we have successfully implemented a four-channel system whose preliminary results at 10 MHz shows a residual white noise floor $<$ -185 dBrad^2/Hz up to 5 MHz off the carrier, and flicker $<$ -127 dBrad^2/Hz using cross-correlation.**

I. Introduction

In the field of Time and Frequency metrology, precise phase estimation is essential for the building and qualification of ultrastable clocks and oscillators with low-jitter. [1].

For more than a decade, with the democratization of Field-Progammable Gate Arrays (FPGAs) used with high-speed digitizers, digital signal processing techniques inherited from telecommunication systems and Software Defined Radio (SDR) [2]–[7] enable to rethink spectral measurements with higher dynamic ranges than traditional coherent demodulation techniques using saturated mixers. Eventually cross-correlation techniques push these limits downwards at a rate of $1/\sqrt{m}$ with m the number of realizations [8], only limited by the storage area and processing power. Also, such digital devices can be useful in understanding collapse effects on cross-spectral estimations [9].

After a short insight on noise spectrum analysis based on digital down conversion and on design workflow, we describe some preliminary measurements on two different platforms.

II. DDC-based noise spectrum analysis

A. Principle of operation

A typical digital down-converter (DDC) based noise analyzer is sketched in Figure 1.

The phase modulated noise degrading a perfect sinusoid is downconverted to DC after sampling thanks to a numerically controlled oscillator (NCO) set up at the carrier frequency. Successive filtering/decimation stages allow to focus on lower decades off the carrier or examine the spectral measure at lower sampling rates by filtering out aliased noise while reducing the measurement bandwidth. Phase estimation is done by calculating the arctangent function of the in-phase and quadrature components of the demodulated and filtered signal. Eventually the amplitude is also estimated. From the phase time series (amplitude time series), the Fourier transform is computed after proper windowing. Ultimately the cross-spectrum is returned.

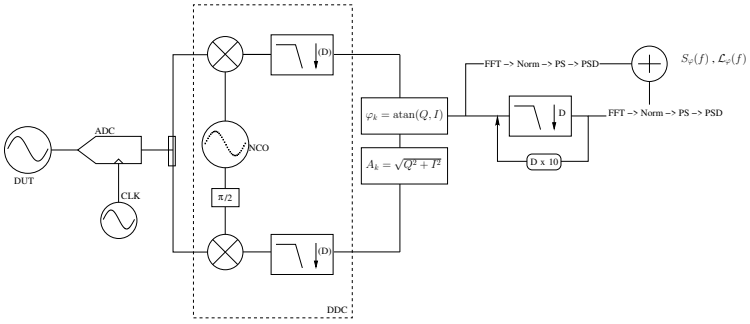

Fig. 1. Principle of a digital phase noise measurement system

B. Design workflow

As we target profound knowledge of digital techniques for metrology, all algorithms and building blocks (except some First In First Out (FIFO) structures) have been developped from scratch at FEMTO-ST. Therefore we have developped a complete EcoSystem from front-end (digitizers) to user space (final user) in order to guarantee code sanity and circular design workflow. C-C++-based libraries enable digital blocks to either match the performances and requirements of the hardware implementation or to be used as threaded double-precision blocks when used at low data rates within the CPU or deported CPU-side. All data transfers from FPGA to CPU or deported host are managed using multi-threaded direct memory access DMA (or ethernet sockets) techniques. Additionally, a Qt-based graphical user interface allows realtime evaluation of the embedded solution with saving features for data inspection.

Experimentations have been mainly performed on Xilinx Zynq-ZC706 coupled to 2 pairs of AD9652 RF digitizers, 16 bits, 250 Msps, under full control. We have also investigated on "out-of-the-box" SDR platform from Ettus Research

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(USRP X310). Concerning the latter, the provided DDC and first filtering/decimation stage was used as it.

III. Measurement chain

Some key elements of the signal path according to Fig. 1 are resumed in this section.

A. Offset compensation

The collected samples usually suffer from remaining offsets of the A/D converters leading to gain mismatch in the spectrum that is sometimes observed in analyzers (Fig. 2).

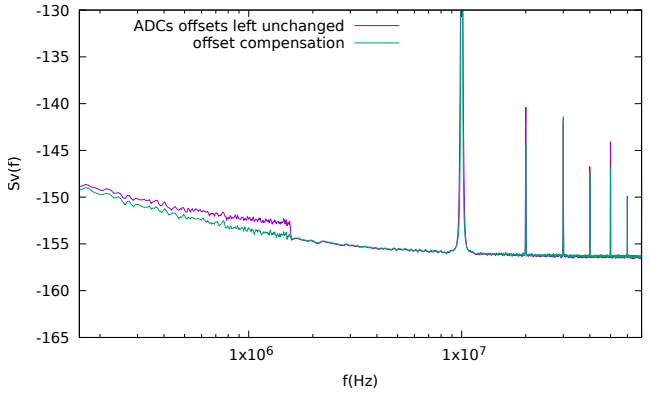

Fig. 2. Distorded spectrum in presence of gain mismatch.

B. NCO

The numerically controlled oscillator is designed with a 32 bit accumulator and lookup table (LUT) size of 2^{12} addresses. It is cadenced to the operating ADC clock (250 Msps) and provides two 16-bits synthetized frequencies in quadrature. No extra algorithm or weighting function such as Taylor series correction were employed and lead to matching results of the Xilinx IP core.

Both NCO output are mixed with the A/D data to provide in-phase and quadrature (IQ) components of the demodulated signal.

C. Filtering/decimation

An FIR (finite impulse response) filter with 128 coefficients acts as a sinc filter. Such a situation may quickly end up consuming a lot of ressources (namely DSP48, highly efficient Multiply-Accumulate slices). As decimation is usually desirable, the required ressources are then lowered as number of operations are useless. They are even lowered for the lower stages, where the data rate becomes decimated compared to the system clock, through judicious reuse of idle slices. It is embedded in a complex form to ensure providing the required filtered I/Q components.

While the full bit width remains unchanged for the first stage, no extra quantization noise is induced by the chain: all the operations that where performed in fixed point thus produce matching results when casted to double precision.

D. Phase extraction

The arctangent function is implemented using a CORDIC (COordinate Rotation Digital Computer) algorithm known to be robust and efficient to quickly converge to the desired angle. Thanks to a 25 iterations process, the phase resolution is in principle $r = \tan^{-1}(2^{-24}) \sim 6 \cdot 10^{-8}$ radians. It is designed to provide a 4-quadrant as would provide the `atan2` function.

The output phase flow is constrained within $\pm\pi$ rotations. An additional block to unwrap phases enable to reconstruct the linear progression of the phase. At high speed, side effects may lead to wrong interpretation of the phase series and produce jumps that need to be detected and circumvent.

Also the linear slope is coupled to the detuning of the analyzed frequency, the NCO frequency, and clock or reference frequency. In order to recover the true phase fluctuations, a linear regression algorithm is thus necessary [10].

Unlike several implementations where linear slopes are removed over long data sets (e.g. [2]), it has been chosen to extract the phase after the I/Q filtering/decimation processes.

The phase time series are windowed (Hanning) and finally processed through a standard radix-2 FFT algorithm to qualify the noise power spectral densities.

IV. Fully digital realtime ADC characterization

In order to qualify the high-speed digitizers, we reproduced the technique developped in [6]. Two pairs of ADCs are analyzed simultaneously in realtime (Figure 3).

The four upper decades are fully performed within the FPGA. Data are transfered to CPU for averaging and display. The I/Q data stream of the fourth filtering stage is directly transfered to CPU at a rate of 25 ksps per channel where spectrum estimation is done continuously for lower decades.

For the AD9652 characterized in this measurement, we deduce from the white voltage noise of -153 dBV^2 an equivalent number of bits (ENOB) of 11.3, in perfect agreement with the datasheet.

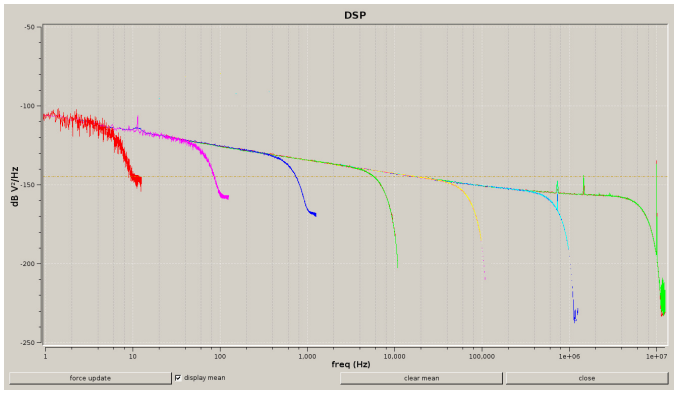

Fig. 3. Snapshot of a user interface with simultaneous measurement of 2 pairs of ADCs (in dBV^2/Hz), 4 min. of averaging

V. Fully digital realtime 4-channel noise floor

A four-channel system has been developped enabling suppression of ADC noises and clocks noise while cross-correlation is operating.

The noise floor was measured by feeding the same synthesizer 10 MHz, 12 dBm signal into the four ADCs.

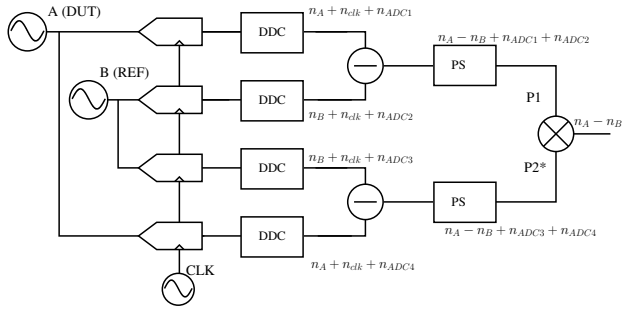

Fig. 4. Principle of a 4-channels phase noise analyzer with cross-correlation.

A. Noise rejection capability

The correct operation of the cross-correlations may be checked by performing the first decade (DDC + phase recovery) within the FPGA. The 25 Msps 4 complex channels are transfered to the CPU via DMA, where the windowing, and cross-spectrum are calculated. Eventually all spectrums (frames) are stored into an external hard drive for data inspection.

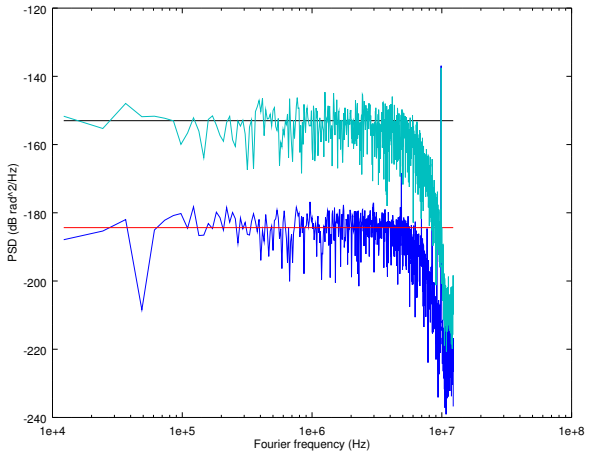

Fig. 5. Straight line (up) : ADC noise fit. Spectrum (up) : First frame (m=1) showing the ADC noise limit. Straight line (down) : Estimated spectrum for 1,863,000 averages. Spectrum (down) : Measured spectrum @frame 1,863,000

The first frame corresponds to a cross-correlation factor (m=1) and is reprensented on Fig. 5. A straight line fit gives the limitation of the measurement (~ -153 dBrad^2/Hz, white) due to the ADC noise. As one selects the frame number 1,863,000, the expected noise rejection would be represented by the estimated line down on the graph, hence $5{\cdot}\log_{10}(m) \simeq 31.3$ dB lower. The corresponding spectrum is also represented. The overall process took $\sim$ 130 min to accomplish (stotage takes time).

B. Noise floor evaluation

Preliminary results of a fully digital realtime implementation are presented in Figure 6. In these proceedings but also to prove the reconfiguration ability, we have chosen to glue two different runs done independently. The two higher decades (10 kHz – 1 MHz) have been computed while the lower decades analysis was disabled in order to gain data transfer bandwidth. This enables a much faster convergence of the noise floor in several hours (43,918.976 averages). The four lower decades were obtained by running the phasemeter continuously for approximately three days (2,859 averages for the 1 Hz – 10 Hz decade).

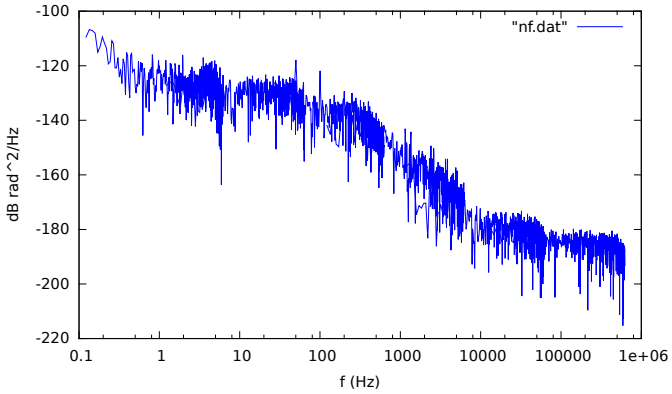

Fig. 6. Fully digital realtime 4-channel noise floor measurement with reconfiguration

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C. Issues

During our experiments we have observed that from time to time the 2 pairs of A/D converters could experience synchronization problems when a measurement process starts (otherwise when the samples are aligned, they keep their alignment during the whole measure). A 1-sample misalignement lead to dramatic results and spectral measure cannot be trusted. Indeed, an extra-rejection of flicker noise is expected. We also experience problems with commercial devices for which we report here an erratum (Fig. 9 in [6]). A detector of misalignment can be implemented to restart the measurement in case of failure. These kind of issues are known and new techniques based on the JESD protocol should avoid this. This situation is mainly encouraged by the use of developpment platforms where the signal lengths are hardly matched (we have for example observed such effects when 2 different signals clocks are not synchronized at the ns level).

D. SDR equipment as an alternative study

Modern Software Defined Radio equipment embed high-speed digitizers suitable to the development of sensitive phase measurement systems. The tested platform concerns specifically here the Ettus Research USRP X310, an attractive

solution for T&F research also because they are open-source / open-hardware solutions. Other groups like [7] have presented interesting results for time deviation purpuses. Eventually such a system was tested "out of the box" providing its dedicated Digital Down Converter.

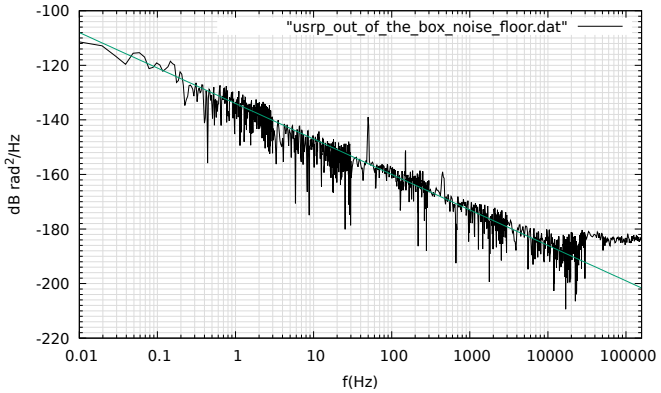

Fig. 7. usrp noise floor.

The white noise floor clearly shows some extra quantization noise due to the DDC we have no control of yet. A significant amount of this noise is folded back to lower frequencies leading to the presented uncommon spectrum.

VI. Application to the measurement of low noise RF synthesizer

The SDR solution has been tested to the measurement of a low noise RF synthesizer (R&S SMA100A used in our experiments) and compared to a commercial high-end 90 k$ instrument (Fig. 8).

For the short term, the limitation is probably due to the SDR device, although we should have observed the spikes revealed by the commercial analyzer. Indeed in [6] we observed similar behaviour.

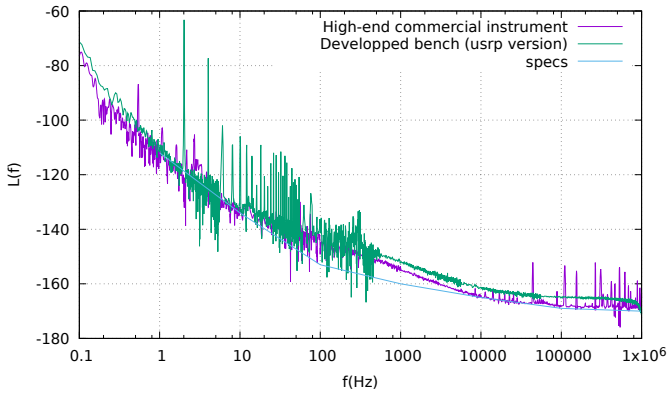

Fig. 8. Measurement of a low noise synthesizer : comparison between High-end instrument and SDR platform @ 10 MHz, 10 dBm.

From 1 Hz – 1kHz, we observe a dense area of spikes, regularly spaced and folded by the main 2 Hz spike. Interestingly, for this frequency, the commercial analyzer shows anti-correlation.

A close up of the 10 Hz – 100 Hz area is analyzed in the following figure. Although not recommended, we removed the 'outliers', and both curves look similar, with a bit more resolution as compared to the smoothed version of the high-end analyzer.

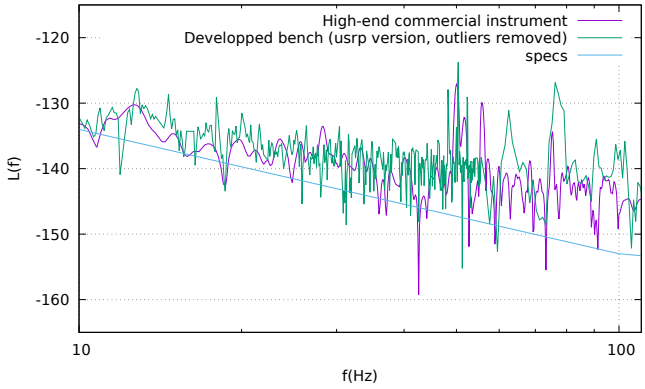

Fig. 9. close up of the Fig.8, with removed outliers

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VII. Conclusion

We have successfully developped a reconfigurable fully-digital phase noise analyzer with realtime operation. White noise floor of $<$ -185 dbrad^2/Hz and flicker $<$ -127 dBrad^2/Hz in a preliminary experiment have been measured.

Acknowledgment

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