Phase noise and jitter in digital electronic components

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I. Introduction

We tested a few digital integrated circuits of different technology and families with the ultimate target of understanding low phase noise frequency synthesis. Digital electronics is appealing for its simplicity, reproducibility and cost, in applications where the lower noise of analog circuits is not mandatory.

Our work is partially driven by the attempt of reducing the phase noise in two ways. First, by paralleling numerous gates, as in microwave and RF amplifiers. Secondly, to dealias the output as we did in the Λ divider [1], yet with the largest pipeline made possible by the high toggling frequency of the newest FPGAs (≈1 GHz).

II. Noise Model

We have identified two classes of phase noise behavior affecting complex digital devices, as suggested by Fig. 1. Some of the key concepts expanded underneath are already present in early articles, chiefly [2] and [3]. Yet, the available literature is anterior to the devices we are interested in, and fits only partially.

The φ-type noise shows up as a random phase φ(t) not affected by the carrier frequency ν_0. This behavior can be understood as a random voltage (threshold) fluctuation v(t) in the presence of a sinusoidal signal of peak amplitude V_p. There follows $\varphi(t) = v(t)/V_p$. However, v(t) is not accessible, and even V_p may differ from the amplitude measured at the input pin. Anyway the signature of the pure φ-type noise is that the power spectral density $S\varphi(f)$ is independent of ν_0. For the sake of clarity we stress that $S\varphi(f)$ can be described by the usual polynomial law, while φ-type just means that $S\varphi(f)$ does not scale up/down with ν_0.

The x-type noise is a fluctuation of the delay, independent of ν_0. This may be called jitter, or more appropriately phase time, defined as $x(t) = \varphi(t)/2\pi\nu_0$. See [4] for further detail on x(t) and the other less-usual noise parameters. The x-type noise can be interpreted as a signal propagating along the complex path of the clock-distribution subsystem. Albeit the actual topology is often inaccessible to the designer, slew rate and noise bandwidth are an outcome of the internal structure, and independent of ν_0. The signature of the pure x-type noise is that the power spectral density $Sx(f)$ is independent of ν_0, thus $S\varphi(f)$ is proportional to ν_0^2.

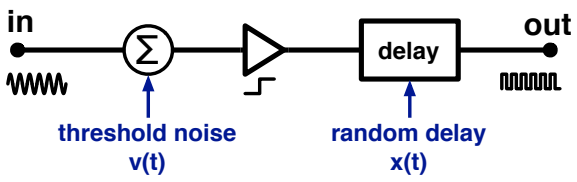

Fig. 1: block diagram describing the two basic phase-noise types.

The phase noise of a digital signal is sampled at each rising and falling edge, thus at the sampling frequency $2\nu_0$. This sets the phase-noise bandwidth B_φ equal to ν_0, usually referred to as the Nyquist frequency, equal to half the sampling frequency. Since it always holds that $\nu_0 < B_N$ (noise bandwidth of the circuit), aliasing folds B_N to B_φ, and increases the phase noise. High B_N/B_φ ratio (example, work at 5 MHz on 1-GHz device) results in unexpectedly high phase noise.

Anyhow, for a given technology (given B_N), aliasing introduces a proportionality factor $1/\nu_0$ to both $Sx(f)$ and $S\varphi(f)$. In turn, the two noise types split into four sub-types listed in Table I. The question of aliasing in the presence of non-white phase noise is kept for later.

III. Experimental Method

Checking on the noise model, we measured the devices listed in Table II with a Symmetricom 5125A test set [5]. Both device-under-test and test set are driven by the same synthesizer. The noise of such synthesizer is common mode, and therefore rejected. Nonetheless we used a high purity synthesizer. We collected noise data scanning the input frequency and changing the internal configuration (HDL program).

After some experiments, we came to the conclusion that frequency changes result in a thermal transient that results from a significant change in the dynamical power consumption. A moderate thermal insulation was used to prevent the

Tab I: Basic noise types

Noise type	Dependence on ν_0	
	$S\varphi(f)$	$Sx(f)$
Pure x-type	ν_0^2	C vs. ν_0
Aliased x-type	ν_0	$1/\nu_0$
Pure φ-type	C vs. ν_0	$1/\nu_0^2$
Aliased φ-type	$1/\nu_0$	$1/\nu_0^3$

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fluctuations of the air flow from spoiling the measured $S\varphi(f)$ at low Fourier frequencies, and a delay of 1 hour after each frequency change proved to be useful.

TAB II: DIGITAL CIRCUITS UNDER TEST

Device	Node size	Type	Brand
MAX 3000	300 nm	CPLD	Altera
MAX V	180 nm	CPLD	Altera
Cyclone II	90 nm	FPGA	Altera
Cyclone III	65 nm	FPGA	Altera
Zynq	28 nm	FPGA / ARM	Xilinx

IV. SOME RESULTS

A. Cyclone III FPGA

Figure 1 shows an example of phase noise measured on an Altera Cyclone III FPGA programmed to replicate the clock to the output (buffer). Thus, the input is a 10 dBm sinusoidal signal, and the output is a square wave at the same frequency.

In the 10–100 Hz decade, the noise fits well the $1/f$ law at all carrier frequencies. So, this region tells us about flicker. Starting from 50 MHz, with smooth transition from 25 MHz, $S\varphi(f)$ follows precisely the ν_0^2 law (+6 dB per factor-of-2). This is the signature of the pure x-type noise. Not a surprise, the input slew rate is high enough to null the effect of the threshold noise, which is of the φ type. The x-type noise of the clock distribution prevails.

For $\nu_0 \leq 25$ MHz, and still in the flicker region, $S\varphi(f)$ tends to the ν_0 law (+3 dB per factor-of-2). In principle, this would be the signature of aliasing in the x-type noise. However, this conclusion conflicts with the rule that aliasing has a negligible effect on flicker. We still not know the explanation, but we are investigating on an alias-like phenomenon where the noise sidebands of the numerous harmonics $n\nu_0$ are folded down to ν_0. Another unexplained effect is the bump at low Fourier frequency, between 0.1 Hz and 10 Hz, which shows up only at the lowest carrier frequencies ($\nu_0 \leq 12.5$ MHz).

At low ν_0 (3.125…12.5 MHz), white noise shows up on the bottom right hand of Fig. 1, with $1/\nu_0$ law (–3 dB per factor-of-2). Since the noise integrated over the bandwidth does not change, decreasing the sampling frequency ν_0 results in higher $S\varphi(f)$. From a different standpoint, this is an outcome of the Parseval theorem, which states that the power can be obtained bi integrating the spectrum, or from the time domain, and the result is the same. This is the signature of φ-type noise, due to the low slew rate at the input, in the presence of aliasing.

This experiment enables to describe a simple description of the noise of the Cyclone III (configured as clock buffer), using only two parameters. First, this device exhibits pure x-type noise in the flicker region for a wide range of carrier frequency and a few decades of Fourier frequency. The flicker component of $Sx(f)$ is of 22 fs/√Hz at 1 Hz, and describes most of the behavior of Figure 1. Then, at low carrier frequency alias results in φ-type noise. Described by $S\varphi(f)=k^2_{A\varphi}/\nu_0$. The parameter $k_{A\varphi}$ can be extracted from Fig. 1. For example, at 12.5 MHz, the white phase noise is of 3.2×10^{-14} rad^2/Hz, thus $k_{A\varphi} = 630$ µrad. Assuming that the noise bandwidth is of 2 GHz (a rough estimate is twice the maximum toggle frequency), and a peak input voltage of 1 V, after Section II we get a threshold fluctuation of 14 nV/√Hz.

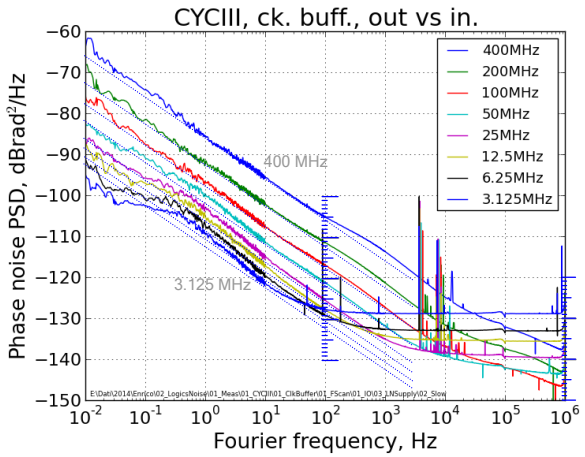

Fig. 1: Residual phase noise of the Cyclon III FPGA programmed to replicate the clock to one output.

B. Preliminary conclusions from the work in progress

Numerous measurements have been done shortly summarized underneath. Others are in progress. The lowest phase noise is observed in elderly CPLDs based on 300-nm technology. Oppositely, the highest phase noise is observed in the highest-density device we tested (28-nm, the FPGA inside a Zynq). This rather general behavior is only partially a surprise because the node size is clearly related to the volume of the active region, where gain and threshold decision take place. In microwave and RF amplifiers, it is well known that lower phase noise is achieved with larger size or by paralleling several devices [6-7]. On the other hand, the short gate delay associated with high density and high speed does not go with proportionally small jitter. Connecting in parallel numerous small-size gates works fairly with white noise, less with flicker. Similarly, the larger pipeline in the Λ scheme could not improve on a smaller pipeline with larger-size gates. In the end, the phase noise of our 300-nm Λ divider [1] is still unsurpassed.

V. FINAL REMARKS

High-density electronics deserves to be studied now because

it is inevitable in future design. Miniaturization and low power are per se interesting features. High speed enables to process high frequencies, while lower dissipation may help in achieving high stability and small interference to other parts of the system. The comparatively small complexity of frequency synthesis may even fit in the unused space of a complex system.

Our work is still in progress, and we will release more at the meeting.

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